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Maikel Fernando Menke

CONTRIBUTION TO THE MODELING, ANALYSIS, DESIGN, AND CONTROL OF THE LLC RESONANT LED DRIVER

Santa Maria, RS
2021

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Thesis presented to the Doctoral Course of the Electrical Engineering Graduate Program, in the Energy Processing Area, of the Federal University of Santa Maria (UFSM-RS), in partial fulfillment of the requirements for the degree of **Doctor in Electrical Engineering**.

Advisor: Dr. Eng. Álysson Raniere Seidel
Co-advisor: Dr. Eng. Rodrigo Varella Tambara

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2021

DEDICATION

To my father, Ernildo Menke, my mother Loraini Braun Menke, and my wife Daniele de Oliveira Freitas.

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First of all, I would like to thank God for everything in my life.

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“I didn’t always stick with Him (God) but he always stuck with me.”
[Eu nem sempre fiquei com ele (Deus), mas ele sempre ficou comigo.]

Denzel Washington, in "Put God First Speech".

RESUMO

CONTRIBUIÇÕES PARA A MODELAGEM, ANÁLISE, PROJETO E CONTROLE DO CONVERSOR RESSONANTE LLC DRIVER DE LED

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ORIENTADOR : Álysson Raniere Seidel Dr. Eng.
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Este trabalho apresenta várias contribuições para a modelagem, análise, projeto e controle do conversor ressonante LLC driver de LED. Inicialmente, a exatidão do modelo dinâmico do conversor é melhorada levando-se em consideração na modelagem o comportamento elétrico não linear do LED ao invés da sua resistência equivalente. Na modelagem emprega-se a função descritiva estendida. Resultados de simulação mostram que o modelo proposto prevê o real comportamento dinâmico do conversor ressonante LLC driver de LED quando a operação se dá em torno da frequência de ressonância. Quando a frequência de comutação (f_{sw}) é diferente da ressonância, o comportamento previsto apresenta erros. Posteriormente, a contribuição para a análise do LLC é dada pela solução no domínio do tempo (DT), onde a solução direta da representação do sistema no espaço de estado é empregada. A análise do LLC no DT supera o problema da abordagem clássica de análise baseada na aproximação pela harmônica fundamental, a qual apresenta erros quando a f_{sw} é diferente da frequência de ressonância do LLC. Em comparação com os procedimentos de análise no DT apresentados na literatura, a metodologia proposta apresenta um número reduzido de aproximações, garantindo assim melhor exatidão. Resultados experimentais mostram uma excelente exatidão do método proposto, independentemente da condição de operação (filtro, carga, entrada, etc.). Empregando a solução no DT proposta, um novo procedimento de projeto para o conversor ressonante LLC driver de LED é proposto. Este projeto baseia-se no conceito da eficiência média ponderada. Além disso, diferentes restrições são avaliadas para garantir comutação em zero de tensão (ZVS), comutação em zero de corrente (ZCS), ganho de potência suficiente e uma faixa de f_{sw} adequada para toda a faixa de operação do conversor. Resultados experimentais mostram que o conversor projetado apresenta alta eficiência, ZVS, ZCS e a uma variação de f_{sw} adequada. A eficiência máxima de 96,44% foi obtida. Em comparação com o projeto clássico, observa-se ganhos de eficiência de até 4,3%. Em relação ao sistema de controle, a contribuição é dada pela proposta de um novo controlador híbrido para o conversor ressonante LLC implementando o estágio DC/DC de um driver de LED conectado à rede elétrica. O controlador proposto é dado por um subsistema PI e um subsistema com rejeição adaptativa de perturbações periódicas, dando origem ao controlador PI&APDR. Resultados experimentais e análises de simulação mostram o excelente desempenho do controlador proposto em comparação com os controladores proporcionais-ressonantes. Empregando o controlador PI&APDR, a referência CC da corrente no LED é rastreada em uma ampla faixa de operação, mesmo sob variações paramétricas, como tensão média de barramento, elementos do filtro ressonante e módulo de LED. Além disso, um desempenho aprimorado é obtido na redução da ondulação da corrente de saída, mesmo quando diferentes frequências e amplitudes na ondulação da tensão do barramento são consideradas. Além disso, embora seja empregado um controlador adaptativo, o PI&APDR preserva a característica de ter um projeto e uma implementação simples.

Palavras chave: Driver de LED. Conversor ressonante LLC. Análise e projeto do LLC. Modelagem e controle do LLC.

ABSTRACT

CONTRIBUTION TO THE MODELING, ANALYSIS, DESIGN, AND CONTROL OF THE LLC RESONANT LED DRIVER

AUTHOR : Maikel Fernando Menke
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This work presents several contributions to the modeling, analysis, design, and control of the LLC resonant LED driver. Initially, the LLC resonant LED driver dynamic model accuracy is improved by taking into account under the modeling the LED non-linear electrical behavior instead of its equivalent load resistance. The extended describing function approach is employed. Simulation results show the feasibility of the proposed model, which predicts the real dynamic behavior of the LLC resonant LED driver when it operates around the main resonance. For the operation beyond the main resonance, the predicted behavior deviates from the real response. Afterward, the contribution to the LLC analysis is given by the proposed time-domain (TD) analysis, where the direct TD solution from the state-space representation is employed. The TD solution overcomes the classical first harmonic approximation (FHA) problem, which presents errors when the switching frequency (f_{sw}) is beyond the LLC series resonance. Compared to the TD procedure reported in the literature, the developed methodology presents a reduced number of assumptions, ensuring leading accuracy. Experimental results show an outstanding accuracy of the proposed method regardless of the operating condition (filter, load, input, etc.). Following, employing the proposed TD solution, a new design procedure for the LLC resonant LED driver is derived. This design procedure relies on the weighted-average-efficiency concept. Besides, different constraints are assessed to ensure zero voltage switching (ZVS), zero current switching (ZCS), enough power gain, and a practical f_{sw} range over a wide operating window. Experimental results show the feasibility of the proposed design procedure, achieving high efficiency, ZVS, ZCS, and feasible f_{sw} range over the whole operating range. The peak efficiency of 96.44% is achieved. In comparison to the classical design, the efficiency is improved up to 4.3%. Regarding the control system, the contribution is given by the proposal of a new hybrid dual-loop controller for the LLC resonant converter implementing the downstream DC/DC stage in an offline two-stage electrolytic-capacitor-free and flicker-free LED driver. The proposed controller is given by a PI subsystem and an adaptive periodic disturbance rejection subsystem, comprehending the proposed PI&APDR controller. Experimental results and simulation analysis show the outstanding performance of the proposed controller in comparison to conventional counterpart resonant-based controllers. Employing the PI&APDR controller the LED current DC reference is tracked over a wide operating range, even under parametric variations such as average bus voltage, resonant tank elements, and LED module. Besides, enhanced performance is achieved in reducing the output current ripple raised from the bus voltage ripple, where different bus voltage ripple frequencies are also considered. Furthermore, even employing non-linear adaptive controllers, the PI&APDR preserves the feature of having a simple design and implementation.

Keywords: LED driver. LLC resonant converter. LLC analysis and design. LLC modeling and control.

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1 INTRODUCTION

Artificial lighting systems (ALS) are essential to human being development. From fire to nowadays state-of-the-art Light-Emitting-Diode (LED), as important as the own produced light, the ability to control its position in space, availability, luminous flux intensity, color, and color temperature, changes the way that world progress. Today, artificial light production comes mainly from an electrical lamp, where input electrical energy is converted into light at the output. Consequently, a significant amount of electrical power is spent worldwide to produce light. Scientific and engineering contributions to diminish this amount of energy are appreciated and have been persuading researchers worldwide. Beyond energy savings gains, considerable attention has been given to ALS based on LEDs because of the LED flexibility. This flexibility allows creating a well-being environment through light intensity control, temperature color control, own color control, and human-centric lighting. In addition to lighting purposes, LEDs have been used to transmit data wireless. However, from energy-saving to human-centric lighting and data transmission, the electronic circuit responsible to correctly power the LED lamp compose the backbone for any modern ALS. Therefore, due to the LED driver importance in the ALS and the constant need to improve their performance and add functionalities, this thesis aims to contribute to development of a high-performance LED driver based on the DC/DC LLC resonant converter.

1.1 MOTIVATION AND BRIEF BACKGROUND

1.1.1 Artificial lighting systems

Artificial lighting systems (ALS) have been widely discussed in the literature, where light-emitting diodes (LED) are nowadays accepted as the most efficient, robust, compact, flexible, and reliable electric light source (lamp) (BRANAS ET AL., 2013), (ALMEIDA, CAMPONOGARA ET AL., 2015), (CHO ET AL., 2017), (Y. WANG, ALONSO ET AL., 2017). However, owing to the LED output light direct relationship with its forward current and the LED voltage source electrical behavior, to adequately supply an LED, a current-controlled

driver must be designed (SCHRATZ ET AL., 2016). Moreover, to outcome in an ALS with the same prominent characteristics of the LED device, the LED driver characteristics have to match the LED ones. This means that the LED driver has to present high efficiency, high reliability and implement advanced functionalities to delight the LED device flexibility.

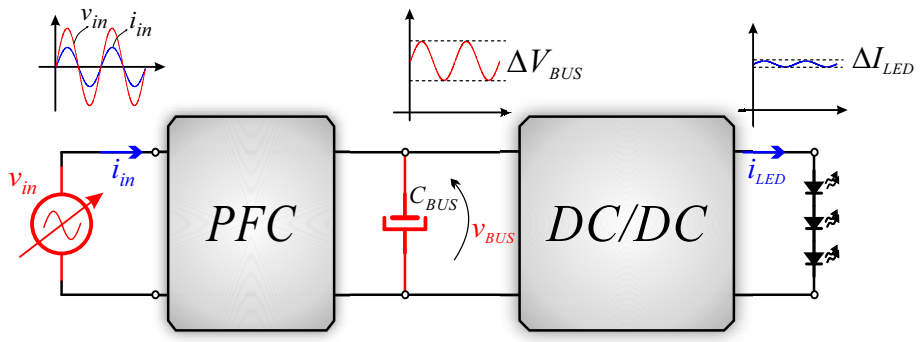
1.1.2 Offline LED driver structure

From the electronic point of view, Fig. 1 shows the usually employed structure for an LED current-controlled driver fed from the local AC line for medium-to-high power (>70 W) ALS applications. As can be seen, two power stages compose the LED driver. The power factor correction (PFC) stage converts the AC input voltage v_{in} to a DC output v_{BUS}, and the DC/DC stage adapts v_{BUS} to suitable levels for the LED device. The PFC stage is responsible for providing a high power factor (PF) and reducing the current harmonic injection into the AC line. For universal input voltage systems ($85-265\ V_{RMS}$; $50-60\ Hz$), the PFC stage regulates the average bus voltage (V_{BUS}) in a fixed value or within a predefined range.

The DC/DC stage is strictly responsible for regulating the LED current (i_{LED}). The average LED current (I_{LED}) reference value is defined by the required dimming level. To modify I_{LED}, amplitude and/or pulse width modulation (PWM) dimming techniques can be employed (LUN ET AL., 2009). On the other hand, due to the straight relationship between LED current and its luminous output flux over a wide bandwidth, i_{LED} has to present a reduced ripple (ΔI_{LED}) in order to avoid output light modulation (flicker). In this way, intended to mitigate health risk to viewers caused by the flicker, recommended practices for modulating LED current presented in (IEEE STD 1789, 2015) should be considered during the LED driver design.

In the last years, several approaches have been proposed in the literature to match the LED device and the driving converter features (ALMEIDA, CAMPONOGARA ET AL., 2015).

Figure 1 – Off-line two stage LED driver structure diagram.



Source: Author.

Among these solutions, to achieve higher power densities and high efficiency in the power processing throughout the LED driver stages, resonant power converters (RPC), instead of hard-switching pulse width modulated (PWM) converters are employed in the DC/DC stage (Y. WANG, GUAN ET AL., 2015B). On the other hand, to enhance the LED driver reliability and lifespan, special attention has been given to the DC-link capacitor (C_{BUS}), where electrolytic capacitors (E-Cap) are being substituted by film capacitors (F-Cap), which presents a longer lifetime with the drawback of a lower energy density (ALMEIDA, CAMPONOGARA ET AL., 2015), (H. MA, W. YU ET AL., 2011).

1.1.3 Flicker-free E-Cap less LED drivers

To avoid the LED driver volume and cost increase due to the F-Cap low energy density compared to E-Cap, several approaches in the literature proposed the employment of reduced DC-link capacitance (W. CHEN ET AL., 2012), (CAMPONOGARA ET AL., 2015), (SOARES, ALMEIDA, ALONSO ET AL., 2017), (LAM ET AL., 2017), (SOARES, ALONSO ET AL., 2018), (KOMSARI ET AL., 2018), (SOARES, ALMEIDA, DE OLIVEIRA ET AL., 2018). Nevertheless, reduced DC-link capacitance values result in an unavoidable higher bus voltage ripple (ΔV_{BUS}). Consequently, ΔV_{BUS} can provoke throughout the DC/DC stage a low frequency (LF) ΔI_{LED}, and so deteriorating the ALS functioning due to the resultant flicker. Hence, the merit of these studies mentioned above is that even employing reduced capacitance values, the driver performance has not deteriorated, being noticed a high power factor, controlled current harmonic injection into the AC line, and low ΔI_{LED}. Furthermore, most of these studies focus on LED driver control system design, which seems to be the most suitable approach since no significant hardware change is necessary to reduce F-Cap capacitance without deteriorating the ALS performance. The ΔI_{LED} attenuation through the control system action is known in the literature as active ripple compensation (ARC) technique (SOARES, ALMEIDA, ALONSO ET AL., 2017). Notwithstanding, these solutions are committed to single-stage or integrated single-stage (ISS) structures, so they can not be directly addressed into two independent stages (2IS) structures such as the one shown in Fig. 1.

1.1.4 LLC resonant power converter

Resonant power converters (RPC) have been employed to implement the DC/DC stage to achieve high efficiency in the power processing throughout the offline LED driver stages. Among several RPC topologies, the LLC configuration has drawn considerable attention due to its capability to reach a wide operation range with high efficiency, low level of electromagnetic emission, high power density, and isolated output (SIMONE ET AL., 2006). Therefore, the LLC resonant converter has been widely employed in diverse applications, such as in battery chargers

(SHAFIEI ET AL., 2017), photovoltaic converters (Q. ZHANG ET AL., 2014), and LED drivers (C. A. CHENG, C. H. CHANG ET AL., 2015), (FENG ET AL., 2014), (DONG ET AL., 2020). Thereby, in a general way, RPC are becoming increasingly popular in industrial applications (R. YU ET AL., 2012) and also become the focus of several studies, where analysis and design procedures have been enhanced.

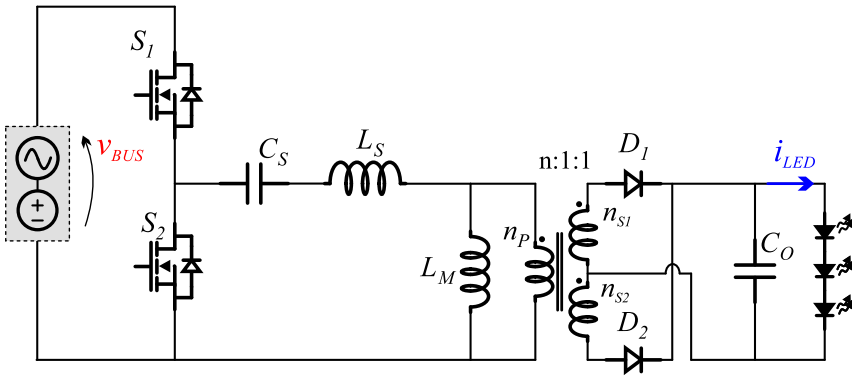
The LLC resonant converter supplying an LED load from the bus voltage provided by a PFC stage is sketched in Fig. 2. Compose the LLC converter structure: the half-bridge (HB) inverter implemented by switches S_1 and S_2; LLC resonant circuit given by the series resonant capacitor C_S, series inductor L_S, and magnetizing inductance L_M of the transformer; Output rectifier implemented by D_1 and D_2; and, output filter given by C_O.

1.1.4.1 LLC resonant LED driver analysis and design

Regarding RPC analysis, the fundamental harmonic approximation (FHA) has become the standard method due to its simplicity, seeing that the system is originally nonlinear. Throughout the FHA analysis, voltages and currents in the resonant circuit are assumed to be sinusoidal. Besides, the output rectifier, output filter, and load in DC/DC applications are modeled as an equivalent AC resistance (R_{ac}), which allows employing the classic AC circuits analysis technique (STEIGERWALD, 1988).

When a RPC converter is subjected to a wide operating range, as it is in the DC/DC stage of an offline LED driver, the switching frequency (f_{sw}), which is modulated to regulate the converter output, moves away from the main resonance (f_o). Nevertheless, especially for the LLC converter operating beyond f_o (L_S and C_S series resonance), the FHA method becomes less accurate (SIMONE ET AL., 2006), (X. FANG, HU, Z. J. SHEN ET AL., 2012), (R. YU

Figure 2 – Circuit diagram of the LLC resonant converter implementing the DC/DC stage of an offline LED driver.



Source: Author.

ET AL., 2012) and (DENG ET AL., 2015). Besides, due to the multi-resonance behavior of the LLC, many aspects of the circuit operation in the time-domain (TD) will be lost in the FHA analysis (X. FANG, HU, Z. J. SHEN ET AL., 2012). These aspects are critical to define and evaluate the converter losses scenario and obtain further insights into the converter behavior, such as the zero voltage switching (ZVS) and zero current switching (ZCS) condition. In this way, to overcome these issues, it is noticed in the literature an effort to employ TD methods when dealing with the LLC resonant converter analysis. However, the analyses presented in the literature that deal with the TD analysis for the LLC converter supplying an LED load are limited, where usually several assumptions are made that impairs the analysis accuracy.

Similarly, when it goes to the LLC resonant LED driver design for a wide operating range, the FHA approach is usually employed to analyze the converter and define its components. Unfortunately, in this case, a poor design is achieved due to the FHA lack of accuracy. The FHA lack of accuracy impairs the accurate prediction of the converter peak gain, switching frequency range, and the zero-voltage switching (ZVS) condition. Hence, to sidesteps these shortcomings, TD analysis has been used to guide the converter design (R. YU ET AL., 2012), (X. FANG, HU, Z. J. SHEN ET AL., 2012), (Z. FANG, CAI ET AL., 2015), (DENG ET AL., 2015), (AWASTHI ET AL., 2018).

1.1.4.2 LLC resonant LED driver control system

The DC/DC stage of the offline LED driver has to regulate I_{LED} over a wide range to perform dimming and reduce LF ripple to avoid flicker. Focusing in control systems that are designed to reduce output current ripple (ARC), studies are mainly found in offline LED drivers and battery charger applications. In these applications, linear and nonlinear controllers have been employed (C. LIU ET AL., 2015), (Z. ZHANG ET AL., 2018), (H. MA, Q. LIU ET AL., 2012), (ZHIYUAN HU ET AL., 2015), (NISHIMURA ET AL., 2012).

It is well known that linear controllers, analyzed by the classical control theory, are simple to design and implement, being so feasible for LED drivers. However, due to the inherent dynamic variation of RPC under amplitude dimming and or parametric variations, the performance of linear controllers becomes deteriorated. Linear controllers are valid only around the nominal operating conditions. Alternatively, nonlinear controllers present strong robustness against disturbances, parameters uncertainties, parametric variation, unmodelled dynamics, and load variations. Nevertheless, nonlinear controllers are usually more complex to design and require high-performance digital systems to be implemented, increasing the cost considerably and rendering it impracticable for LED drivers where simple implementations are desired.

At this point, it can be seen that the main challenge in a current-controlled LED driver conception is the design of a stable control system capable of regulating I_{LED} over a wide

dimming range, attenuate LF ΔI_{LED} excited by ΔV_{BUS}, and hand over a suitable dynamic performance preserving overall a simple implementation fashion. In this perspective, a model that predicts the converter dynamic behavior with high accuracy contributes to the design of a control systems that is less sensitive to present a deteriorated performance when subjected to a wide operating range. Alternatively, a solution for this challenge would be the development of a new control systems structure, where the advantages of classical and nonlinear controllers are gathered without impairing the system simplicity. Nevertheless, few studies reported in the literature directly deal with the LLC resonant LED driver dynamic model and its control system design.

1.1.5 Thesis central focus

Based on the preceding discussion, it can be seen that there are several challenges in the high-performance offline LED driver analysis, design, and control, mainly related to the DC/DC stage implemented by LLC resonant converter. To solve these problems, a trustful analysis and design procedure should be developed employing the TD analysis, which considers the converter's whole operating range and load non-linearity. Besides, a control system capable of maintaining I_{LED} controlled, attenuate LF current ripple, and hand over a satisfactory dynamic performance for the driver simultaneously without compromising the control system simplicity should be proposed. However, to design a stable control system utilizing linear or nonlinear controllers, it is necessary to know in advance the LED driver dynamic behavior as accurately as possible. Usually, the system dynamic behavior is given by the small-signal model of the power electronics converters that composes the driver, mathematically represented as a transfer function (TF). Therefore, an improved small-signal model for the LLC resonant LED driver should also be proposed. In this way, the development of all these solutions is the central focus of this thesis.

Regarding the issues mentioned above, it should be noticed that they are related to the DC/DC stage of an offline two stages LED driver, which is implemented by the LLC resonant converter. Therefore, to limit the main topic discussed in this thesis to the DC/DC stage, the PFC stage is omitted being v_{BUS} emulated by a voltage source.

1.2 OBJECTIVE AND CONTRIBUTIONS

The LLC resonant converter employment in LED drivers has drawn the attention of scientific research and industrial applications. However, to obtain a high-performance LLC resonant LED driver, several issues and challenges are not adequately addressed in the literature, which becomes the focus of this thesis.

1.2.1 Objective

This study aims to propose original solutions for the problems that impair the conception of a high-performance LLC resonant LED driver. Thus, seeking to contribute to the modeling, analysis, design, and control of the LLC resonant LED driver. The specific objectives are highlighted as follows.

1.2.1.1 LLC resonant LED driver small-signal modeling

To properly feed the LED device, a current-controlled driver has to be designed. Therefore, a feedback loop is incorporated into the control system of the LED driver to regulate the output current. However, to design a stable control system with satisfactory performance, it is essential to know the LED driver dynamic behavior with high accuracy. Nevertheless, several issues arise when the dynamic behavior of the LLC converter is going to be modeled. Initially, classical modeling procedures can not be directly applied to RPC. Therefore, the extended describing function method has been employed. Besides, the LED non-linearity also affects the dynamic behavior of the converter. Thus, it should be included in the modeling approach.

With these issues in mind, the LLC resonant LED driver dynamic behavior is carefully analyzed to derive an improved modeling procedure. Hence, the proposal of a trustworthy modeling procedure for the LLC resonant LED driver dynamic behavior is a specific objective of this thesis.

1.2.1.2 LLC resonant LED driver time-domain solution

To overcome the FHA lack of accuracy and disclose further insights for the LLC resonant LED driver, an alternative solution is systematically presented to analyze the converter in the TD. In this way, considering the LLC as a piece-wise linear system, the state-space representation direct TD solution is employed. So, the TD solution of the LLC resonant LED driver figures as a specific objective of this study.

1.2.1.3 LLC resonant LED driver design

Classical design procedures rely on the converter analysis carried out by the FHA. Consequently, for the LLC resonant converter operating over a wide range, classical design approaches does not lead to a reliable design. In this perspective, a new design procedure is necessary, which should be indispensable based on the TD analysis. TD-based procedures

outcome in a reliable design since the predicted converter behavior presents enhanced accuracy. Therefore, one particular objective of this thesis is the development of a new LLC resonant LED driver design, strictly derived from the converter TD analysis. In addition, this design procedure should consider the wide operating range of the converter, assess its power density, and pursue a general high-performance.

1.2.1.4 Enhanced control system for offline LED drivers

As aforementioned, the main challenge for a current-controlled LED driver conception is the design of a stable control system that presents a suitable performance while preserving overall a simple implementation fashion. Therefore, linear and nonlinear control systems are evaluated to propose a new control system with enhanced performance. In this way, the proposal of a new control system for the LLC resonant LED driver is one specific objective of this thesis.

1.2.2 Thesis Contribution

The following developments are claimed as this thesis proposal:

1. Proposal of an improved LLC resonant LED driver small-signal model. So, solving the problem given by LED device non-linearity influence in the dynamic response.
2. Proposal of a new procedure to analyze the LLC resonant LED driver in the TD. Thus, solving the problem related to the lack of accuracy in predicting the behavior of the LLC convert with the classical FHA approach.
3. Proposal of an improved design procedure for LLC converter supplying an LED load under a wide operating range. Thus, solving this gap in the literature.
4. Proposal of an new hybrid controller for the LLC resonant LED driver. Thus, solving the problems related to the LED current ripple attenuation and robust DC current reference tracking under a wide operating window.

1.3 THESIS OUTLINE

To organize the contents, this thesis is arranged in chapters that develop each claimed contribution.

Chapter 2 presents the LLC resonant converter literature review, enclosing its modeling, analysis, design, and control, continually establishing a link with the LLC resonant LED driver. This chapter is not intended to exhaust the literature review but discuss the latest developments in state-of-the-art technology.

Chapter 3 deals with the LLC resonant LED driver small-signal modeling. The extended describing function approach is employed. Wherein, to achieve a trustworthy model, the LED non-linearity modeled by its piece-wise linear circuit is taken into account throughout the modeling procedure.

Chapter 4 presents the proposed TD solution for the LLC resonant LED driver, which is based on the state-space representation direct TD solution adapted to a non-linear system. Besides, the proposed mode solver and proposed operating mode map are also discussed.

Chapter 5 deals with the proposed design procedure for the LLC resonant LED driver. The proposed design is based on TD analysis, predicted average efficiency, and additional constraints that ensure enough current gain, soft switching, and improved efficiency over a wide operating range.

Chapter 6 proposes a new hybrid controller, which presents enhanced performance in tracking the LED current DC reference, reject input and output step disturbance, and periodic disturbance rejection from the bus voltage ripple. The essence of this control is given by a PI plus an adaptive periodic disturbance rejection subsystem.

Chapter 7 summarizes this thesis, presenting final remarks, suggestion for future works, and related publications.

2 LLC RESONANT LED DRIVER REVIEW

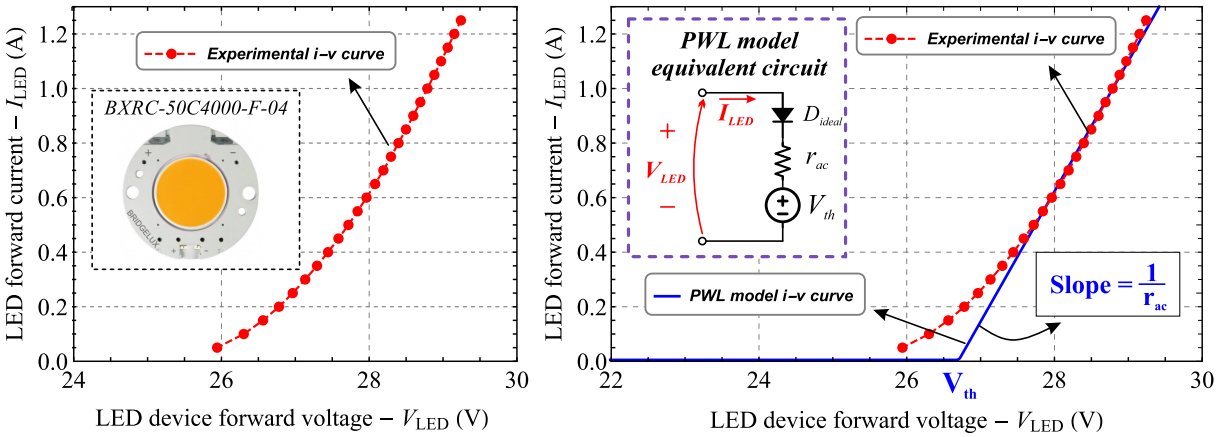
This chapter presents the state-of-the-art technology review of the LLC resonant LED driver modeling, analysis, design, and control to situate the reader in the thesis subject and provide the initial understanding of this research topic. To highlight the research gap, studies that are similar to the current work are critically analyzed.

2.1 LED DEVICE ELECTRICAL BEHAVIOR

To analyze and design an LED driver, it is essential to known the LED electrical behavior, given by the forward current and voltage relationship (*i-v curve*). Fig. 3(left) shows the measured *i-v curve* for the chip-on-board (COB) device, model BXRC-50C4000-F-04 (BRIDGELUX, 2014) employed in this thesis.

To characterize the LED device *i-v curve* mathematically, the modified Shockley equation is employed in (SCHUBERT, 2006), (ALMEIDA, NOGUEIRA ET AL., 2011). To simplify the analysis of the *i-v curve*, this exponential function is expressed by the Taylor series in (R. L. LIN, S. Y. LIU ET AL., 2013). Alternatively, piece-wise linear (PWL) models have been widely employed due to their simplicity and feasibility (R. L. LIN E Y. F. CHEN, 2009). In the PWL model, a simple equivalent circuit can emulate the LED *i-v curve*, which

Figure 3 – LED *i-v curve*; Left: Experimental *i-v* characteristic of the BXRC-50C4000-F-04 LED device; Right: LED PWL model equivalent circuit *i-v curve*.



Source: Author.

describes the LED in terms of an ideal diode D_{ideal}, its forward diode voltage drop V_{th}, and the internal series resistance r_{ac} (or r_d).

Considering the linear region in the BXRC-50C4000-F-04 LED *i-v curve* ($0.45\ A < I_{LED} < 1.15\ A$), and employing least square fitting, the obtained equivalent PWL model parameters are $r_d = 2.094\ \Omega$ and $V_{th} = 26.696\ V$. This equivalent circuit *i-v curve* response is plotted in Fig. 3(right) and compared to the measured curve. From the comparison, it can be noticed that the PWL model behaves similarly to the measured *i-v curve* only when $0.45\ A < I_{LED} < 1.15\ A$. For $I_{LED} < 0.45\ A$, the modeled *i-v curve* deviates from the measured one, impairing the LED driver theoretical analysis, especially for applications where the LED current amplitude is modulated to achieve dimming. To illustrate how the LED current amplitude modulation (AM) outcomes in dimming, Fig. 4 shows the LED relative luminous flux intensity as a function of I_{LED} for the BXRC-50C4000-F-04 device.

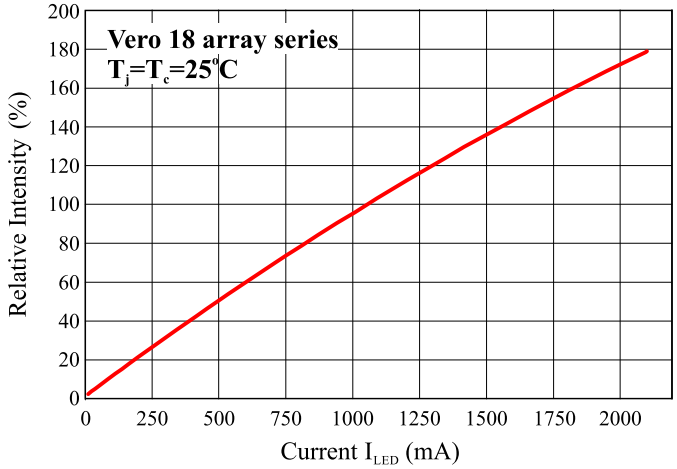
To enhance LED PWL model accuracy, the superposition concept of the multi-branch PWL (MBPWL) circuit is proposed by (R. L. LIN E Y. F. CHEN, 2009). This approach splits the *i-v curve* into several PWL parts. To elucidate the MBPWL LED equivalent circuit model, Fig. 5(left) shows the LED equivalent circuit employing two branches and the yielding theoretical *i-v curve*. The MBPWL equivalent circuit parameters V_{F1} and V_{F2} are selected LED forward voltage levels, and the internal series resistances (r_1 and r_2) are defined by (2.1).

$$r_1 = \frac{V_{F2} - V_{F1}}{I_{F2}} \tag{2.1a}$$

$$r_2 = \frac{V_{F3} - V_{F2}}{I_{F3} - \frac{V_{F3} - V_{F1}}{r_1}} \tag{2.1b}$$

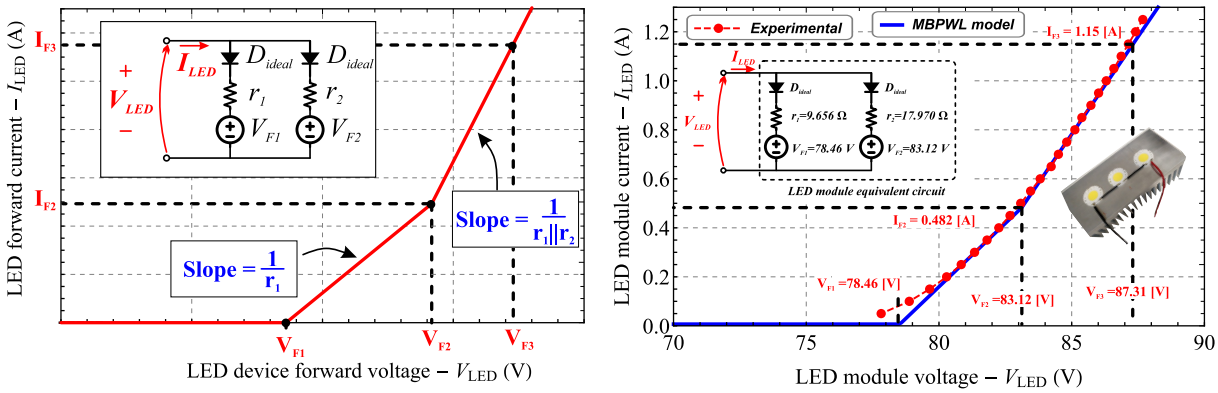
To compose the LED module employed in this thesis, three BXRC-50C4000-F-04

Figure 4 – Typical relative luminous flux as a function of the LED current.



Source: Adapted from (BRIDGELUX, 2014)

Figure 5 – MBPWL model analysis: (a) Two-branch PWL LED equivalent circuit and *i-v curve*; (b) LED module measured *i-v curve* in comparison to the MBPWL *i-v curve*; and, LED module MBWPL model equivalent circuit.

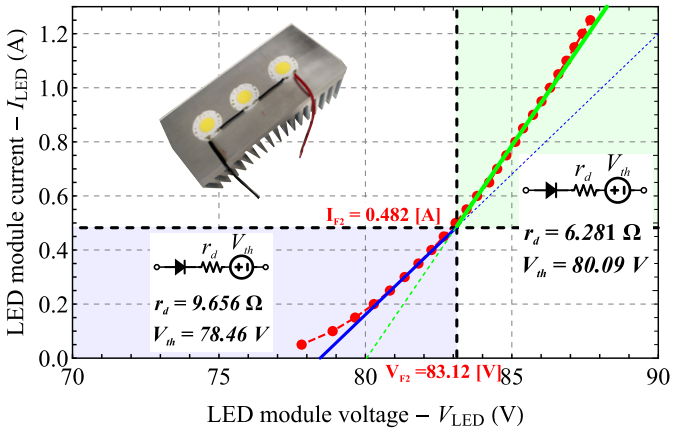


Source: Author.

devices are connected in series. The series connection is adopted to avoid the current balancing issue. Besides, due to the low voltage and high current COB device characteristics, the LED module voltage is not excessive. Finally, to achieve the required 100 W for the rated output power, the LED module nominal forward current has to be 1.15 A. Fig. 5(right) shows the measured *i-v curve* in comparison to the predicted value by the MBPWL circuit for the LED module (three LED in series). As can be seen now, compared to a single PWL model, the MBPWL model matches the measured *i-v curve* over a broader range.

Alternatively, the LED module behavior can be emulated by two single PWL circuits as shown in Fig. 6. Where $I_{LED} = 0.482\ A$ and $V_{LED} = 83.12\ V$ correspond to the boundary condition that defines which PWL model to use. This approach simplify the mathematical analysis since a piece-wise-defined function can be employed. On the other hand, under simulation the equivalent circuit shown in Fig. 5 has to be employed.

Figure 6 – LED module electrical behavior emulated by two piece-wise-defined PWL model.



Source: Author.

2.2 OFFLINE LED DRIVER STRUCTURE OVERVIEW

Fig. 1 shows the usually employed structure for a medium-to-high power (>70 W) offline LED driver when the module is composed by a single string[1]. In this case, the LED driver is conceived by a two-stage structure, given by the AC/DC front-end power factor correction (PFC) stage followed by a DC/DC current-controlled converter, where the DC-link bus capacitor decouples both stages (C_{BUS}) (S. LI ET AL., 2016), (STMICROELECTRONICS, S.D.). A comprehensive LED driver structure review, here omitted, can be seen in (Y. WANG, ALONSO ET AL., 2017), (ARIAS ET AL., 2012), and (S. LI ET AL., 2016).

Assuming that the PFC stage is implemented by the boost converter operating with universal input voltage (85–265 V_{RMS}, 50/60 Hz), which is the usual solution in this application (C. A. CHENG, H. L. CHENG ET AL., 2014), the nominal average bus voltage V_{BUS} has to be greater than 375 V, being natural choice 380 V or 400 V. Meantime, the LED driver output voltage is a function of the employed LED technology and its array configuration (series and/or parallel connection). However, in new medium-to-high power ALS designs, the COB LED technology has usually been chosen due to their small optical source, compact device, and low cost (BRODRICK, 2016). Thus, due to the COB LEDs low voltage and high current characteristics (BRIDGELUX, 2014), the DC/DC stage supplying a COB LED-based load has to present a high voltage gain; otherwise, the LED cannot be appropriately powered. Furthermore, implementing the dimming by the I_{LED} amplitude modulation (AM) (LUN ET AL., 2009), will demand from the DC/DC stage the ability to operate under a wide range. Besides, it should be carried in mind that the bus voltage v_{BUS} is not constant but presents periodic oscillations due to the inherent power imbalance between input and output. v_{BUS} also shows some DC fluctuation due to the PFC stage transient behavior during load and AC line variation. Consequently, this v_{BUS} variation ($AC + DC$) will increase even more the DC/DC stage operating window.

In these circumstances, among different resonant tanks, the LLC configuration leads to an optimal solution to implement the DC/DC stage for an offline LED driver. The LLC resonant converter can reach a wide operation range with high efficiency due to its soft-switching characteristics, together with a low level of EMI emission, and the ability to achieve high power density (B. YANG ET AL., 2002), (SIMONE ET AL., 2006). These LLC features also meet the pursued features for the LED driver, which are high efficiency and consequently high reliability, high power density, and high flexibility. It is important to highlight that for an ALS that employs LEDs, the driver must match the LED device's characteristics.

As aforementioned, to enhance the offline LED driver reliability, E-Cap that are usually employed as the DC-link capacitor (C_{BUS}), are being substituted by F-Cap. F-Cap presents a

[1] Multi-string applications employ a post-regulator for each string.

longer lifetime with the drawback of a lower energy density (ALMEIDA, CAMPONOGARA ET AL., 2015), (H. MA, W. YU ET AL., 2011). However, to avoid the LED driver volume and cost increases due to the F-Cap low energy density compared to E-Cap, several approaches in the literature proposed the employment of reduced DC-link capacitance. Nevertheless, reduced DC-link capacitance values result in an unavoidable higher ΔV_{BUS}. So, in a two-stage offline LED driver, the DC/DC stage has to handle this excessive ΔV_{BUS}, mainly by avoiding its transmission to the LED current. Low-frequency (LF) high ΔI_{LED} must be avoided since it will give rise to flicker (LEHMAN ET AL., 2014).

Therefore, to get the design specifications for the LLC resonant converter implementing the downstream DC/DC stage in a two-stage offline LED driver structure, the following assumptions are taken for v_{BUS}: (i) its is assumed that the nominal average bus voltage is 400 V; (ii) due to the use of F-Cap with reduced capacitance, the bus voltage contains a 40 V peak-to-peak periodic ripple at twice the input grid frequency ($100-120\ Hz$); (iii) the DC/DC stage must be able to supply the load with its nominal power over a $380-410\ V_{DC}$ input voltage range, so providing constant light intensity under the event of a line dropout. (iv) PFC over-voltage protection is activate when $v_{BUS} > 420\ V$.

Now, gathering the bus voltage and output current variation, Table 1 presents the LLC resonant LED driver design specifications. Analyzing Table 1, it has to be noticed that the LLC converter is designed to operate over a wide range, presenting a V_{BUS} variation between 360 V and 420 V, and a variable output current to perform dimming between 100% and 20%, which correspond to the reference dimming range for outdoor applications established in (ENERGY STAR, 2019). The AM dimming method is employed due to its simplicity compared to the pulse-width modulation (PWM) dimming method.

It is important to mention that usually LED drivers are not designed to accomplish with hold-up time specifications. However, with the fast digitalization of ALS, the hold-up time specification trend to be incorporated into new designs. Although, in this thesis, the hold-up time is not taken into account.

Table 1 – LLC resonant LED driver specifications

Parameter	**Designator**	**Nom**	**Min**	**Max**
Half-bridge input voltage	V_{IN} or V_{BUS}	400 V	360 V	420 V
Bus voltage ripple frequency range	$f_{\Delta V}$	–	100 Hz	120 Hz
Average output current	I_O	1.15 A	0.20 A	1.15 A
Outcome power	P_O	100 W	16 W	100 W
Outcome output voltage	V_O	87.31 V	80.39 V	87.31 V

Source: Author.

2.3 DC-LINK CAPACITANCE REDUCTION

The LED device presents outstanding features that made it the mainstream electrical light source in any new ALS. However, to extract from the LED device all its potentialities, it is indispensable that the LED driver performs as well as the own LED device. Regarding the reliability of power electronics systems and LED drivers, several works have stated that the E-Cap employed in the DC-link corresponds to the weakest link in the electronic system, so becoming one of the lifetime bottleneck (H. WANG, H. WANG ET AL., 2020), (H. LI, S. LI ET AL., 2021). To overcome this drawback, several approaches have been proposed E-Cap-less LED drivers. In these E-Cap-less LED drivers, the metalized F-Cap are employed, whose lifetime can achieve more than 100000 hours. Besides, because of the F-Cap self-healing capability, they rarely fail catastrophically (ALMEIDA, CAMPONOGARA ET AL., 2015). However, unfortunately, F-Cap presents reduced energy-density compared to E-cap (H. WANG E BLAABJERG, 2014). In this way, to avoid LED driver volume and cost increases, several works in the literature have proposed different techniques to reduce the required capacitance in the DC-Link (CAMPONOGARA ET AL., 2015), (SOARES, ALONSO ET AL., 2018), (H. LI E XIAO, 2020). Hence, the converter power density does not deteriorate, and the lifetime is increased. However, reduced DC-link capacitance values result in an unavoidable higher bus voltage ripple (ΔV_{BUS}), giving rise to the output flicker if this ripple is not handled correctly. Therefore, a hot research topic corresponds to the development of flicker-free E-Cap-less LED drivers.

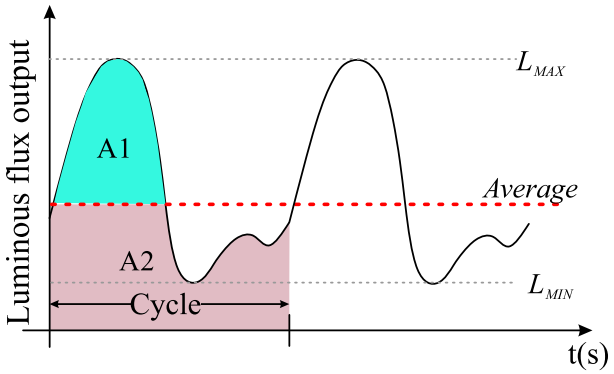
2.3.1 Flicker

The flicker can be defined as a change in the luminous flux of a lamp due to power fluctuations of the power supply (IEEE STD 1789, 2015). In LED-based artificial lighting systems, the flicker occurs due to the current variations. In this way, the harmonic content of the current flowing across the LED translates into light output modulated by those components (CASTRO ET AL., 2019).

To evaluate the flicker, two metrics were defined in order to measure the flicker (LEHMAN ET AL., 2014). Fig. 7 shows the luminous flux variation about time to elucidate the flicker metric definitions. The Flicker Index is defined as the area above ($A1$) the line of the average luminance divided by the total area ($A1+A2$) of the light output curve during a cycle, given by (2.2). The percent flicker, also defined as $Modulation(\%)$ or $Mod.(\%)$ is computed by (2.3).

$$Flicker\ Index = \frac{A1}{A1+A2} \tag{2.2}$$

Figure 7 – Flicker index and Percent flicker definition.



Source: Adapted from (IEEE STD 1789, 2015)

$$Modulation(\%) = \frac{L_{MAX} - L_{MIN}}{L_{MAX} + L_{MIN}} \tag{2.3}$$

where L_{MAX} and L_{MIN} are respectively the maximum and minimum output luminance.

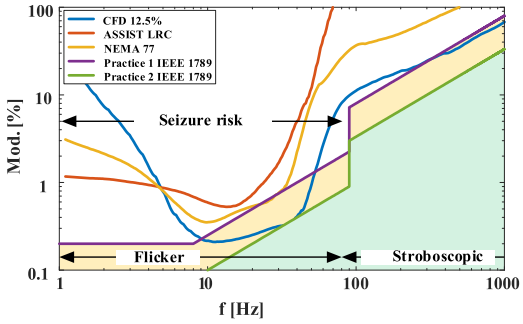
Although the flicker refers to modulation of luminous intensity, for lighting systems based on LED, it is usually assumed that the LED current is approximately proportional to the luminous flux output of the LED (see Fig. 4). This linear response can be assumed up to 1 MHz. Consequently, the LED current ripple can be employed to estimate the luminous intensity variation. However, in LED driver specifications, the LED current ripple is defined as the peak-to-peak ripple ($\Delta I_{LED} = I_{max} - I_{min}$). Thus, the percent LED current ripple is given by $\Delta I\% = 100\ \Delta I_{LED}/I_{LED}$. For the special cases where $I_{LED} = 0.5(I_{max} - I_{min})$, then the $\Delta I\%$ is equal to twice the $Mod.(\%)$ (IEEE STD 1789, 2015). In other words, the $Mod.(\%)$ can be estimated by $Mod(\%) = \Delta I\%/2$.

Considering the LED current direct relationship with the luminous output, both Flicker index and $Mod.(\%)$ can be easily computed by manipulating experimental LED current measurements. Nevertheless, these two defined metrics present the issue of being independent of the flicker frequency and the lack of a relationship with human eye perception (CASTRO ET AL., 2019). Therefore, other metrics have been proposed in the last decade, which consider flicker frequency and the human eye-sensitive curve. Nevertheless, in a general way, these different metrics have in common the fact that they set specific reference values to the admissible fluctuations of the light at specific frequencies, which can be translated to the permissible current ripple in the case of LEDs.

Fig. 8(a) shows a comparison among different flicker metrics in terms of the allowed $Mod.(\%)$ at each frequency. As can be seen, Practice 2 of the IEEE 1789-2015 is the most restrictive of all the discussed flicker metrics (IEEE STD 1789, 2015). In this way, whenever an LED driver is conceived without E-Cap, the most rigorous regulation set by Practices 2 should be respected for a conservative design. In other words, all the harmonic components of the measured LED current should lie within limits given by Practice 2, specified in Fig. 8(b).

Figure 8 – (a) Comparison of different flicker metrics in terms of the allowed Mod.(%); (b) Recommended practices in accordance to (IEEE STD 1789, 2015).

(a) –



(b) –

Practice 1	If it is desired to limit the possible adverse biological effects of flicker, then flicker Mod. (%) should satisfy the following goals: • Below 90 Hz, Mod. (%) is less than 0.025×frequency. • Between 90 Hz and 1250 Hz, Mod. (%) is below 0.08×frequency. • Above 1250 Hz, there is no restriction on Mod. (%).
Practice 2	If it is desired to operate within the recommended NOEL of flicker, then flicker Mod. (%) should be reduced by 2.5 times below the limited biological effect level given in Recommended Practice 1: • Below 90 Hz, Mod. (%) is less than 0.01×frequency. • Between 90 Hz and 3000 Hz, Mod. (%) is below 0.0333×frequency. • Above 3000 Hz, there is no restriction on Mod. (%).

Source: Adapted from (CASTRO ET AL., 2019).

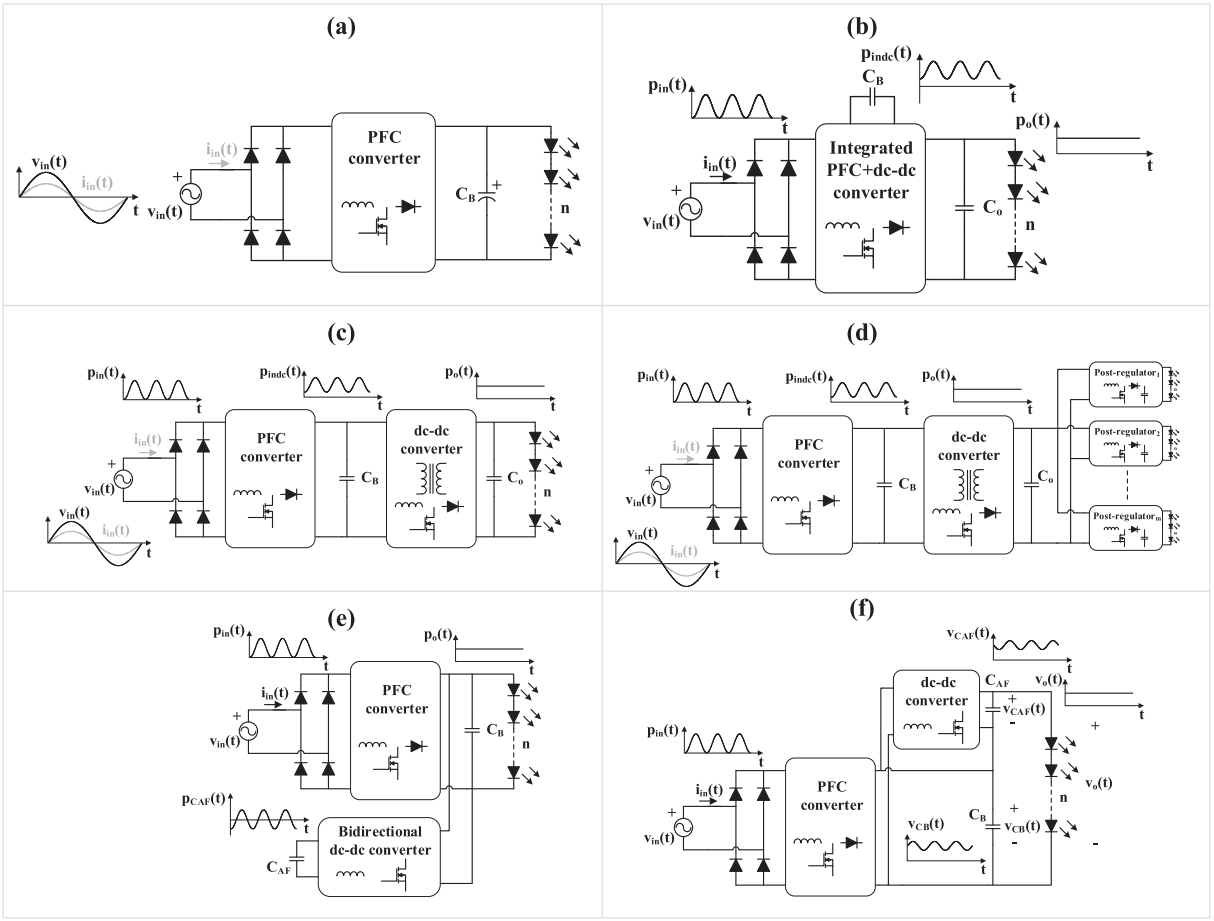
2.3.2 Flicker-free E-Cap-less Offline LED drivers

The DC-link in offline LED drivers is necessary to handle the power imbalance between AC input and DC output. Thus, reduced C_{BUS} capacitances unavoidable give rise to higher ΔV_{BUS}, whose frequency $f_{\Delta V}$ is double the AC line frequency. Thus, if the LED driver does not present any resource to counterbalance this ripple, the LED driver will present the flicker phenomenon. In this way, several works have been reported proposing solutions to outcomes with an LED driver free of E-Cap and flicker-free. Subjected to this scenario, a review of the state-of-the-art strategies to drive LEDs from ac power with a flicker-free feature is reported in (CASTRO ET AL., 2019).

Considering active solutions for single-phase systems that perform high power-factor, the offline LED driver structure can be classified as following: single-stage; integrated single-stage (ISS); multi-stage; multi-stage with reduced redundant power processing; multi-stage with active DC-link filter; and modular solutions. From a macro point of view, this classification is related to the number of power conversion stages in the LED driver. Except for the modular solutions that are rarely employed, Fig. 9 sketched the schematic of the mentioned structures.

The single-stage solution shown in Fig. 9(a) present as features the low-cost and simplified implementation. On the other hand, this structure presents difficulties in achieve simultaneously high power factor, dimming, and E-Cap-less. Besides, the universal input voltage is also rarely employed in this topology. Isolated output is also complicated to implement with reduced capacitances. This structure also presents voltage conversion ratio issues and is not suitable for medium-to-high power applications. Nevertheless, one way to realize a single-stage Flicker-free E-Cap-less LED driver is by distorting the input current up to the limits defined by IEC-61000-3-2, Class C standard (LAMAR ET AL., 2012), (W. CHEN

Figure 9 – Common Off-line LED driver strucures. (a) Single-stage; (b) Integrated single-stage; (c) Multi-stage: Two-stages; (d) Multi-stage: Three-stages; (e) Multi-stage, or pseudo single-stge, with active DC-link filter; (f) Multi-stage with reduced redundant power processing.



Source: (CASTRO ET AL., 2019).

ET AL., 2012). Thus, reduced capacitances can be employed without provoking an excessive bus voltage ripple.

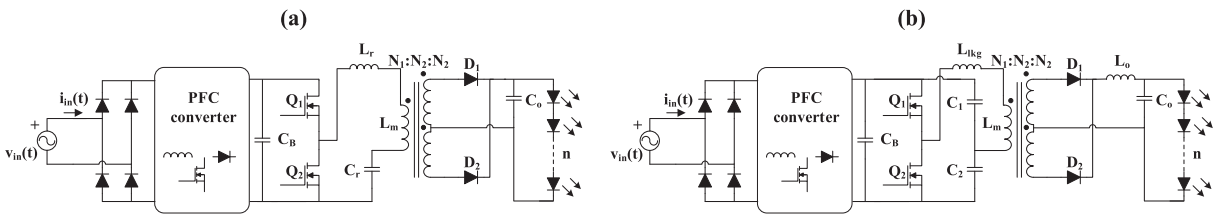
On the other hand, the integrated single-stage (ISS) shown in Fig. 9(b) is the most used method to achieve a single-stage that can remove E-cap without incurring into flicker. This solution combines the PFC and DC/DC stage by sharing the active switches. Consequently, a single control loop is responsible for regulating the output current while maintaining the high power factor at the input. To conceive the Fricker-free E-Cap-less offline LED driver with the ISS structure, different approaches have been reported in the literature. Initially, the DC/DC stage should be carefully analyzed to select the converter that presents reduced voltage ripple transformation (BRAND ET AL., 2020). On the other hand, the bus voltage ripple can be canceled at the converter's output with the help of the control loop, usually by distorting the input current. In general, this solution is not as efficient as the two-stage due to stress happening on the shared switches. Besides, ISS structure is not recommended for universal

input voltage applications that demand dimming. Regarding the isolated output, it can be achieved by properly selecting the DC/DC stage. ISS offline LED drivers employing reduced capacitances, while achieving low LED current ripple and high power factor, have been reported in (ALONSO ET AL., 2012), (DA FONSECA ET AL., 2017), (SOARES, ALMEIDA, ALONSO ET AL., 2017), (SOARES, ALMEIDA, DE OLIVEIRA ET AL., 2018), (SOARES, ALONSO ET AL., 2018), (LUZ ET AL., 2018), (LAM ET AL., 2017).

Regarding the multi-stage structure, several variations have been reported in the literature. Fig. 9(c) shows the two-stage structure, where the PFC stage converts the AC input voltage v_{in} to a regulated DC output V_{BUS}, simultaneously providing a high power factor (PF) and reducing the current harmonic injection into the AC line. The second stage (DC/DC converter) is strictly dedicated to supplying the LED load with adequate voltage and current levels. The control loop of the DC/DC stage can be effectively designed to attenuate the ΔV_{BUS} avoiding its transmission to the LED current. Besides, in this structure both PFC and DC/DC stages are decoupled due to the DC-link. Thus, each stage can be optimized without impairing the adjacent converter. In a general way, the two-stage structure corresponds to the optimal solution in terms of efficiency, reliability, and flexibility. This structure is commonly employed in high-performance LED drivers, addressing Flicker-free, E-Cap-less, universal input voltage, and full dimming (MENKE, TAMBARA, BISOGNO ET AL., 2016B), (MENKE, TAMBARA, BISOGNO ET AL., 2016A). Cost and complexity are the most limiting factor, so this structure is employed in applications wherein reliability and efficiency are of most importance. With regard to the DC/DC stage, two solutions are gaining attention: the LLC resonant converter and the asymmetrical Half-Bridge (AHB), shown in Fig. 10. In the case of the AHB, this topology can provide high reliability and high efficiency by reaching zero voltage switching (ZVS) in the primary switches. The LLC resonant converter has been widely used for LED driving due to its high efficiency over a wide operating range. In the LLC, ZVS can be achieved on the primary side as well as ZCS on the secondary side.

For high-performance multi-string applications, the three-stage solution shown in Fig. 9(d) is employed. In this system, a post-regulator is added to control the LED current of each string. Multi-stage, or quasi-single-stages, structures that do not process all the power as

Figure 10 – Preferred solutions for high performance medium-to-high power two-stage Offline LED driver. (a) Half-bridge LLC resonant; (b) Asymmetrical half-bridge converter.



Source: (CASTRO ET AL., 2019).

in the full cascade solution are classified in multi-stage with auxiliary active DC-link filtering or multi-stage with reduced redundant power processing. Fig. 9(e) shows the structure for the case where the active DC-link filter is employed. This configuration comprises an E-Cap-less PFC converter and a bidirectional converter, which serves to absorb the AC component of the pulsating current of the PFC converter, leaving only a DC component to drive the LEDs (S. WANG ET AL., 2012).

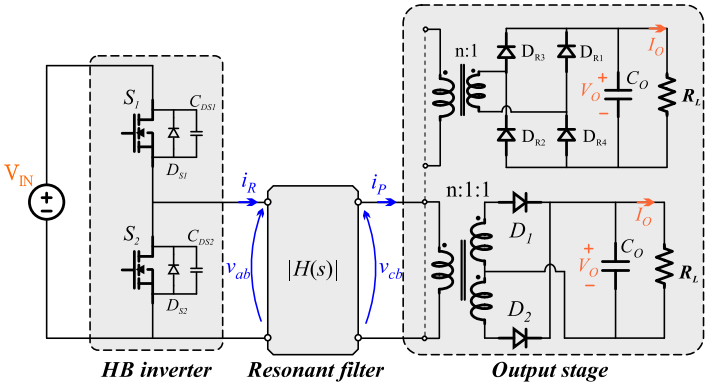
For the multi-stage with reduced redundant power processing (R2P2) shown in Fig. 9(f), the output of DC/DC converter will be a voltage waveform with its phase inverted from the output voltage of PFC. Employing this structure, high efficiency can be achieved at the expense of a complex control system. It is worthy of mentioning that analog control is preferred in offline LED drivers. Flicker-free E-Cap-less LED driver employing multi-stage R2P2 structure are detailed in (CAMPONOGARA ET AL., 2015), (VALIPOUR ET AL., 2016),(BEKOSKI ET AL., 2019), (H. LI E XIAO, 2020), and (H. LI, S. LI ET AL., 2021).

Finally, it is worthy of mentioning that alternative solutions have been proposed by merging the presented structures. For instance, in (H. MA, LAI ET AL., 2016), the PFC and DC/DC stage are integrated, and a post regulator controls the LED current. In (H. MA, W. YU ET AL., 2011) a single stage with post-regulator is proposed.

2.4 LLC RESONANT POWER CONVERTER ANALYSIS

In a general way, the resonant power converter (RPC) structure is given by an inverter, a resonant filter, and an output rectifier. Easily the output can be isolated by employing high-frequency transformers. For the mentioned inverter, between Full-bridge (FB) and Half-bridge (HB) inverters, the HB configuration is commonly employed for medium-to-low power step-down applications. Regarding the output rectifier, the FB or then FW rectifier can be employed. Fig. 11 elucidates the RPC converter structure employing an asymmetrical HB inverter.

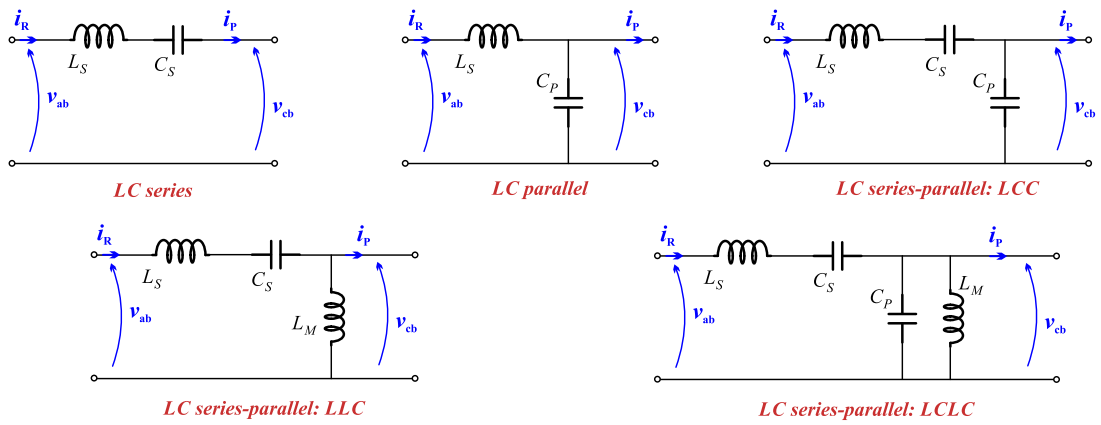
Figure 11 – Half-bridge resonant power converter structure with isolated output.



Source: Author.

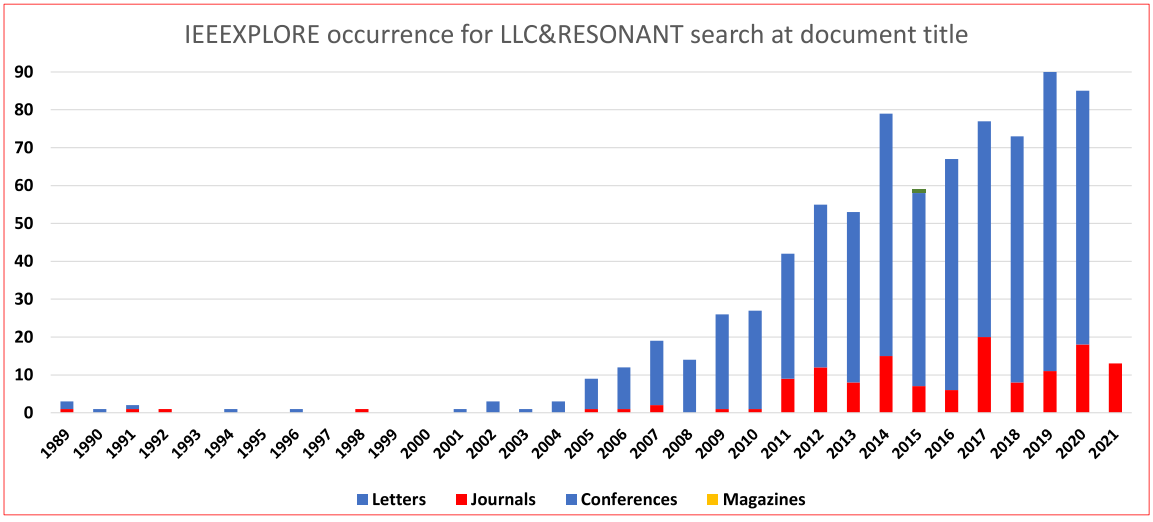
The resonant filter is responsible for the RPC voltage and current gain, HB switching condition, switching-frequency range, and the converter power efficiency conversion and density. Fig. 12 shows the most popular configurations for the resonant filter. Each topology presents its advantages, disadvantages, features, and optimal application. Nevertheless, among these filter configurations, the series-parallel LLC has received considerable attention in the last decade due to its high performance over a wide operating range. To exemplify the attention that LLC resonant power converters are receiving, Fig. 13 shows the occurrence sorted by year for the search in the IEEEXplore platform delimited to the occurrence of "LLC"and "Resonant"at the document title. As can be seen, there is a continuous increase in the number of publications in the last decade, which also stamps the LLC resonant converter as a hot research topic in the power electronics field.

Figure 12 – Classical resonant filters.



Source: Author.

Figure 13 – IEEEXplore occurrence of LLC&RESONANT search at document title. Search on 04/04/2021.



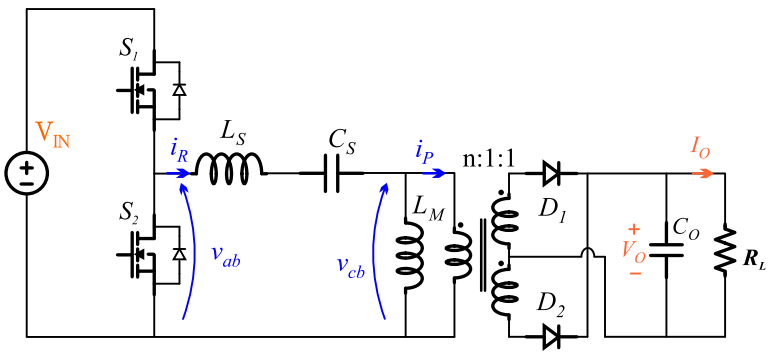
Source: Author

Fig. 14 shows the schematic diagram for the HB LLC resonant converter employing the FW rectifier with capacitive output filter and resistive load. As can be seen in Fig. 14, the LLC topology is the LC series where the magnetizing inductance is incorporated into the resonant filter. By utilizing the transformer magnetizing inductance L_M, the LLC converter modifies the gain characteristic of the series resonant converter (LC series). Compared with the LC series, the LLC converter can achieve both buck and boost mode. Besides, it considerably improves the light-load efficiency. However, its multiple resonant stages and various operation modes make it difficult to analyze and design accurately (DENG ET AL., 2015).

Regarding RPC analysis techniques, there are several possible approaches: First Harmonic Approximation (FHA) or frequency domain; Time domain or operation mode analysis (TD); State-plane analysis (SPA); Laplace based theorem (LBT); Discrete based analysis (DBA); Hybrid analysis: Frequency domain with partial TD correction (HFTD1), and Frequency domain with complete TD correction (HFTD2). A comparison among different analysis methodologies for LLC resonant converter is presented in (WEI, LUO, S. CHEN ET AL., 2019). As stated, each analysis presents its accuracy and complexity features. It is worth mentioning that the accuracy of the LLC analysis can directly influence the converter parameter's design and performance. Besides, the way that the electrical behavior of the load is considered also affects the analysis accuracy, mainly for the nonlinear load as LED.

The RPC analysis is essential for the complete system insight and design. For a given modulation strategy, the analysis aims to predict the converter behavior as a function of the changed parameter. Among several modulation strategies for RPC, pulse frequency modulation (PFM) is the most employed modulation in the industry. In this strategy, the inverter switches are controlled in a complementary fashion, with 50% duty, and by a variable switching frequency (f_{sw}), the output voltage and current can be changed. A comprehensive review of the LLC converter modulation techniques is presented in (WEI, LUO E MANTOOTH, 2020B). With the RPC adequately analyzed, the design methodologies are derived.

Figure 14 – Half-bridge LLC resonant converter.



Source: Author.

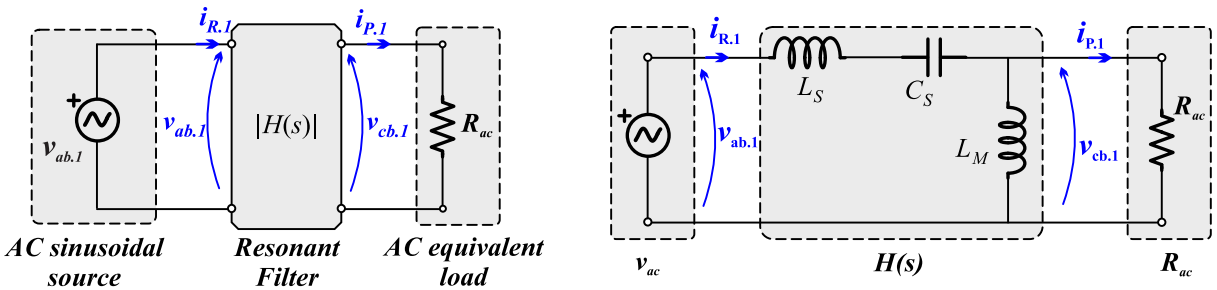
2.4.1 First Harmonic Approximation - FHA

To analyze the RPC, the FHA approach, based on classical AC complex analysis, is introduced in (STEIGERWALD, 1988). The FHA has become the standard method to analyze RPC due to its simplicity, seeing that the system is originally nonlinear. Throughout the FHA analysis, all voltages and currents in the resonant circuit are assumed to be sinusoidal, and output rectifier, filter, and load are modeled as an equivalent AC resistance (R_{ac}) reflected to the primary side. These assumptions allow employing the classic AC circuits analysis technique (STEIGERWALD, 1988). In other words, the FHA is based on the assumption that input-to-output power transfer is essentially due to the fundamental component of the Fourier series of currents and voltages. Fig. 15 shows the equivalent AC circuit for a generic RPC as well as the AC equivalent circuit for the LLC filter.

Focusing on the LLC resonant converter, several studies reported in the literature present a detailed qualitative analysis of the steady-state operation employing FHA (SIMONE ET AL., 2006), (HUANG, 2010), (ADRAGNA ET AL., 2009). Fig. 16(a) shows the LLC resonant converter main waveforms for the operation at the series resonance, also referred to as the main resonance (f_o). As it can be seen, the resonant current i_R is quite similar to a sinusoidal waveform. On the other hand, the HB inverter output voltage v_{ab} correspond to a square waveform, which amplitude is given by the input voltage V_{IN}, and frequency is defined by the HB f_{sw}. The voltage at the primary side of the transformer v_{cb} corresponds to a symmetrical square waveform, whose amplitude is given by the output voltage reflected to the primary side nV_O, where n is the transformer turn ratio.

To obtain the parameters for the equivalent AC circuit of the LLC resonant converter shown in Fig. 15, initially the voltage v_{ab} is decomposed in Fourier series, and its fundamental value $v_{ab.1}$ is isolated, given by (2.4) and shown in Fig. 16(b). Similarly, the v_{cb} fundamental $v_{cb.1}$ value is defined by (2.5). The resonant tank parameters are not modified in the classical FHA.

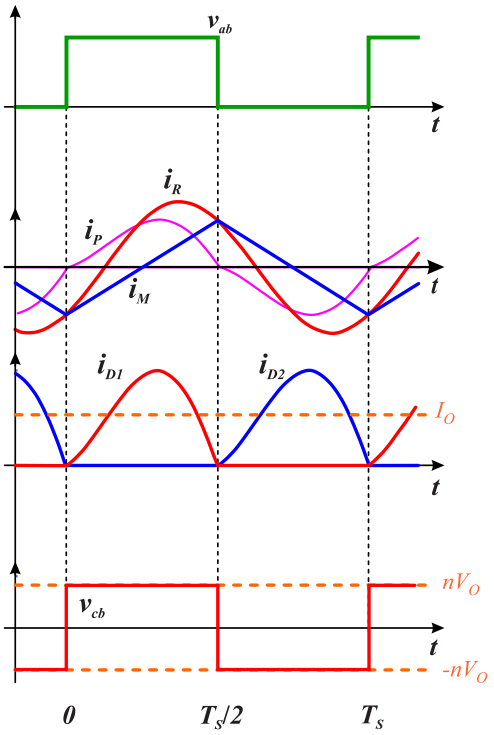
Figure 15 – AC equivalent circuit. Left-trace: Equivalent AC circuit for a generic RPC; Right-trace: Equivalent AC circuit for the LLC resonant converter.



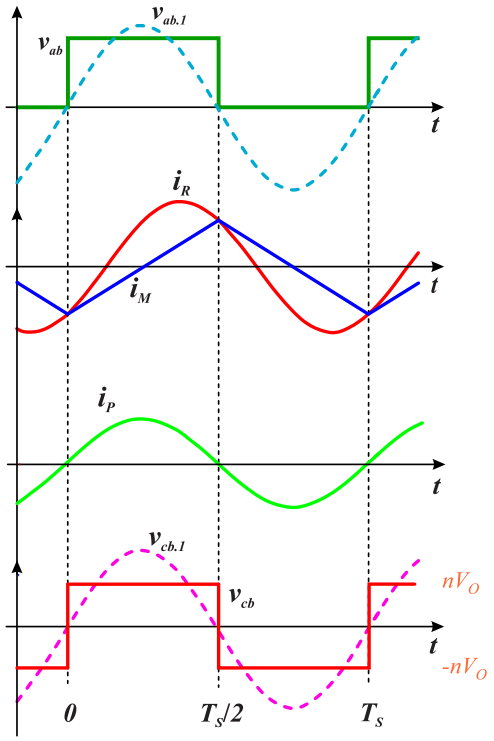
Source: Author.

Figure 16 – Half-bridge LLC resonant converter main waveforms when operating at the series resonance.

(a) – Nonlinear waveforms.



(b) – FHA approximation.



Source: Author.

$$v_{ab.1} = \frac{2}{\pi} V_{IN} sin(\omega t) \tag{2.4}$$

$$v_{cb.1} = \frac{4n}{\pi} V_O sin(\omega t) \tag{2.5}$$

Analyzing Fig. 15 and main waveforms in Fig. 16, it it should be noticed that the current flowing into transformer primary winding i_P correspond to the current that flows throughout the AC equivalent load R_{ac} (see Fig. 15), consequently $i_P = i_{Rac}$. With little effort, it can also be noticed that i_P is in phase with v_{cb}. In this way, based on the energy equivalence point of view, the load can be modeled as an AC equivalent resistor, defined by (2.6).

$$R_{ac} = \frac{v_{cb.1}}{i_{Rac}} \tag{2.6}$$

Since the output capacitor only absorbs AC current, the DC average value of rectified

sinusoidal wave current i_{Rac} is equal to the load current I_O. Thus the amplitude of i_{Rac} is computed by (2.7).

$$i_{Rac} = \frac{\pi}{2n} I_O sin(\omega t) \tag{2.7}$$

Finally, substituting (2.5) and (2.7) into (2.6), and after some calculations yields in

$$R_{ac} = \frac{8n^2}{\pi} R_L \tag{2.8}$$

where, $R_L = V_O/I_O$.

By solving the simplified AC equivalent circuit obtained by FHA, the DC voltage gain characteristic is derived. Analyzing Fig. 15, the LLC filter output to input voltage transfer function (voltage DC gain) can be defined by (2.9). Where $|H(s)|$ is given by (2.10).

$$\frac{v_{cb.1}}{v_{ab.1}} = \frac{\frac{4n}{\pi} V_O}{\frac{2}{\pi} V_{IN}} = \frac{2nV_O}{V_{IN}} = |H(s)| \tag{2.9}$$

$$|H(s)| = \frac{V_O}{V_{IN}/2n} = \frac{1}{\sqrt{\left(1 + \frac{1}{L_n}\left(1 - \frac{1}{f_n^2}\right)\right)^2 + Q^2\left(f_n - \frac{1}{f_n}\right)^2}} \tag{2.10}$$

Where $L_n = L_M/L_s$ is the inductance ratio, $f_n = f_{sw}/f_o$ is the normalized switching frequency, being f_o given by (2.11); and Q is the quality factor of the filter defined by (2.12).

$$f_o = \frac{1}{2\pi\sqrt{L_S C_S}} \tag{2.11}$$

$$Q = \frac{\sqrt{\frac{L_S}{C_S}}}{\frac{8n^2}{\pi^2} R_L} \tag{2.12}$$

Alternatively, the LLC resonant filter gain can be computed by (2.13). Where the resonant factor A and load factor B are defined by (2.14) and (2.15), respectively.

$$|H(s)| = \frac{1}{\sqrt{A^2 + B^2}} \tag{2.13}$$

$$A = \left(1 + \frac{1}{L_n}\left(1 - \frac{1}{f_n^2}\right)\right) \tag{2.14}$$

$$B = Q\left(f_n - \frac{1}{f_n}\right) \tag{2.15}$$

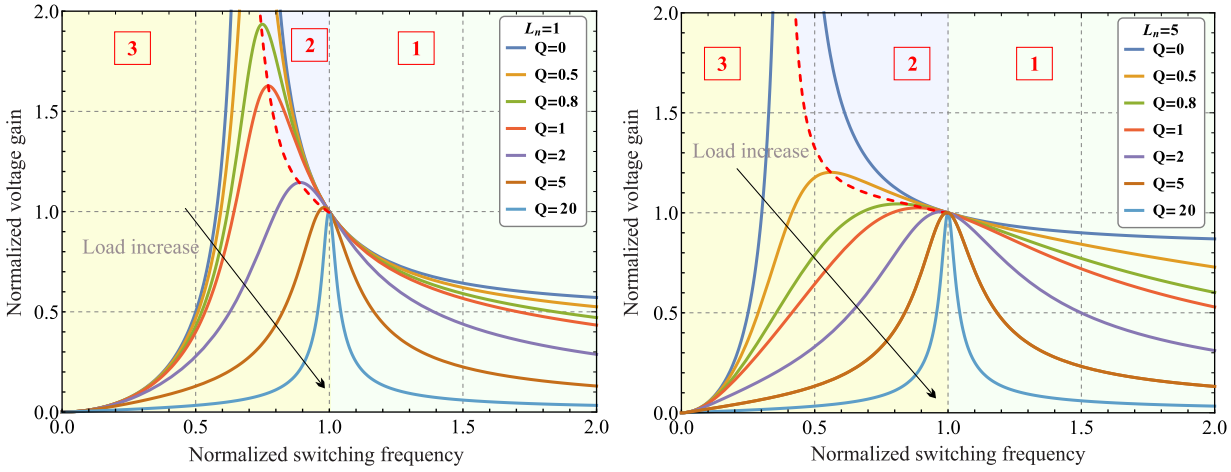
With the LLC gain mathematically defined, several analyses can be carried out assessing the effect of the main parameters in the converter gain. For instance, Fig. 17 shows the LLC normalized gain for different Q and L_n, as a function of the normalized f_{sw}.

Basically, three regions characterize the LLC operation under FHA analysis. In Region 1, since the $f_{sw} > f_o$, the LLC operates in the buck mode, and ZVS condition can be noticed for the HB switches. Region 2 is delimited by $f_{zvs/zcs} < f_{sw} < f_o$, where $f_{zvs/zcs}$ is the ZVS/ZCS boundary condition, highlighted by the red dotted line in the curve gains. In Region 2, the HB can work under ZVS, and the output rectifier can work with ZCS. Region 3 should be avoided since, in this region, the HB switches lose the ZVS condition. Furthermore, it can be seen that when $f_{sw} = f_o$, the LLC resonant circuit operates as a voltage source, regardless of the load. It is worth mentioning that Region 1 and Region 2 outcome in as inductive operation. Below f_o, the L_M participates in the resonance, thus for no-load condition, the peak gain frequency f_p is computed by (2.16). This second resonant frequency characterizes the LLC as a multi-resonant converter.

Figure 17 – Voltage gain characteristic of the LLC resonant converter supplying an resistive load.

(a) – DC gain for different Q values as a function f_n, being $L_n = 1$;

(b) – DC gain for different Q values as a function f_n, being $L_n = 5$.



Source: Author.

$$f_p = \frac{1}{2\pi\sqrt{(L_S + L_M)C_S}} \tag{2.16}$$

2.4.1.1 FHA for the LLC resonant LED driver

Fig. 18 shows the LLC resonant converter supplying an LED load. As can be seen, the LED electrical behavior is emulated by its PWL circuit (see section 2.1), which has an entirely different electrical behavior compared to the LED equivalent resistance $R_{eq} = V_{LED}/I_{LED}$. Therefore, to obtain trustfully FHA analysis results, the LED nonlinear behavior needs to be considered under the equivalent AC load definition (WU, 2011A), (WU ET AL., 2011B).

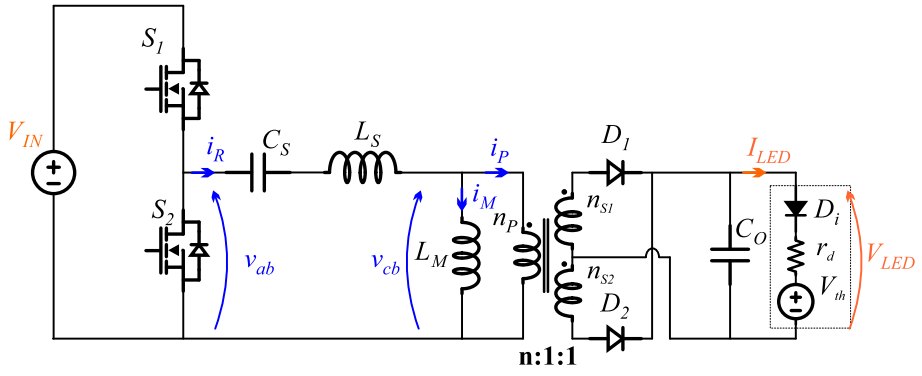
To mathematically describe the LED electrical behavior by the single PWL model, the relationship between I_{LED} and V_{LED} can be rewritten by

$$I_{LED} = \begin{cases} \frac{V_{LED} - V_{th}}{r_d} & \text{if} \quad V_{LED} > V_{th}, \\ 0 & \text{if} \quad V_{LED} \leq V_{th} \end{cases} \tag{2.17}$$

In order to simplify the analysis, it is assumed that the output LED current and voltage ripple is negligible. In this way, considering the operation at f_o with $V_{LED} > V_{th}$, the main waveforms of the LLC resonant LED are the same as the LLC resonant converter previously presented in Fig. 16. Then, combining (2.17) in the definition of R_{ac}, the value of R_{ac} for the LLC converter supplying an LED load is derived, given by (2.18).

$$R_{ac} = \frac{v_{ab1}}{i_{Rac}} = \begin{cases} \frac{8n^2 r_d}{\pi^2} \frac{V_{LED}}{V_{LED} - V_{th}} & \text{if} \quad V_{LED} > V_{th}, \\ \infty & \text{if} \quad V_{LED} \leq V_{th} \end{cases} \tag{2.18}$$

Figure 18 – LLC resonant LED driver circuit.



Source: Author.

Finally, Fig. 19 shows the equivalent AC circuit for the LLC resonant LED driver. In this circuit, the value of R_{ac} is no longer a function of the constant resistor (R_{eq}), but reflects the nonlinear behavior of the LED. Defined the equivalent AC circuit of the LLC resonant LED driver, its voltage and current characteristics can be derived. However, it should be carried in mind that because of the LED load nonlinear electrical behavior, two different AC equivalent circuits should be analyzed independently to reflect LED non-linearity. When $V_{LED} > Vth$, LED is in on state and R_{ac} is a finite value and follows LED *i-v* relationship. When $V_{LED} \leq Vth$, LED is in off state, and forward current is zero, the circuit operates as in no-load condition. In addition, especially for LED drivers, the LED forward current instead of voltage needs to be controlled. Thus, the LLC current gain is derived.

For the LLC resonant LED driver, the quality factor Q is defined by (2.19). Then, employing the resonant factor A and load factor B previously defined, the normalized current gain for the LLC resonant LED driver is obtained given by (2.20) (WU ET AL., 2011B). Wherein K is given by (2.21); and, the current normalization factor I_n is given by (2.22). It should be noticed that I_n is the output current at $f_{sw} = f_o$ under nominal input condition.

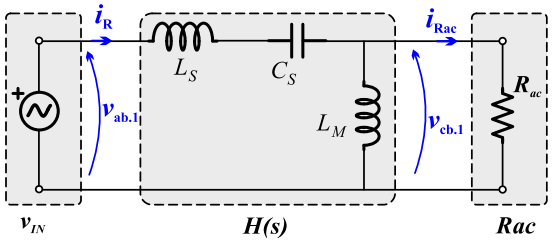
$$Q = \frac{\sqrt{\frac{L_S}{C_S}}}{\frac{8n^2}{\pi^2} r_d} \tag{2.19}$$

$$H_i(s) = \frac{I_{LED}}{I_n} = \begin{cases} \frac{1}{K-1} \frac{-A^2 + \sqrt{A^4 - (A^2+B^2)(A^2-K^2)}}{A^2+B^2} & \text{if} \quad V_{LED} > V_{th}, \\ 0 & \text{if} \quad V_{LED} \leq V_{th} \end{cases} \tag{2.20}$$

$$K = \frac{V_{IN}/2n}{V_{th}} \tag{2.21}$$

$$I_n = \frac{V_{IN}/2n - V_{th}}{r_d} \tag{2.22}$$

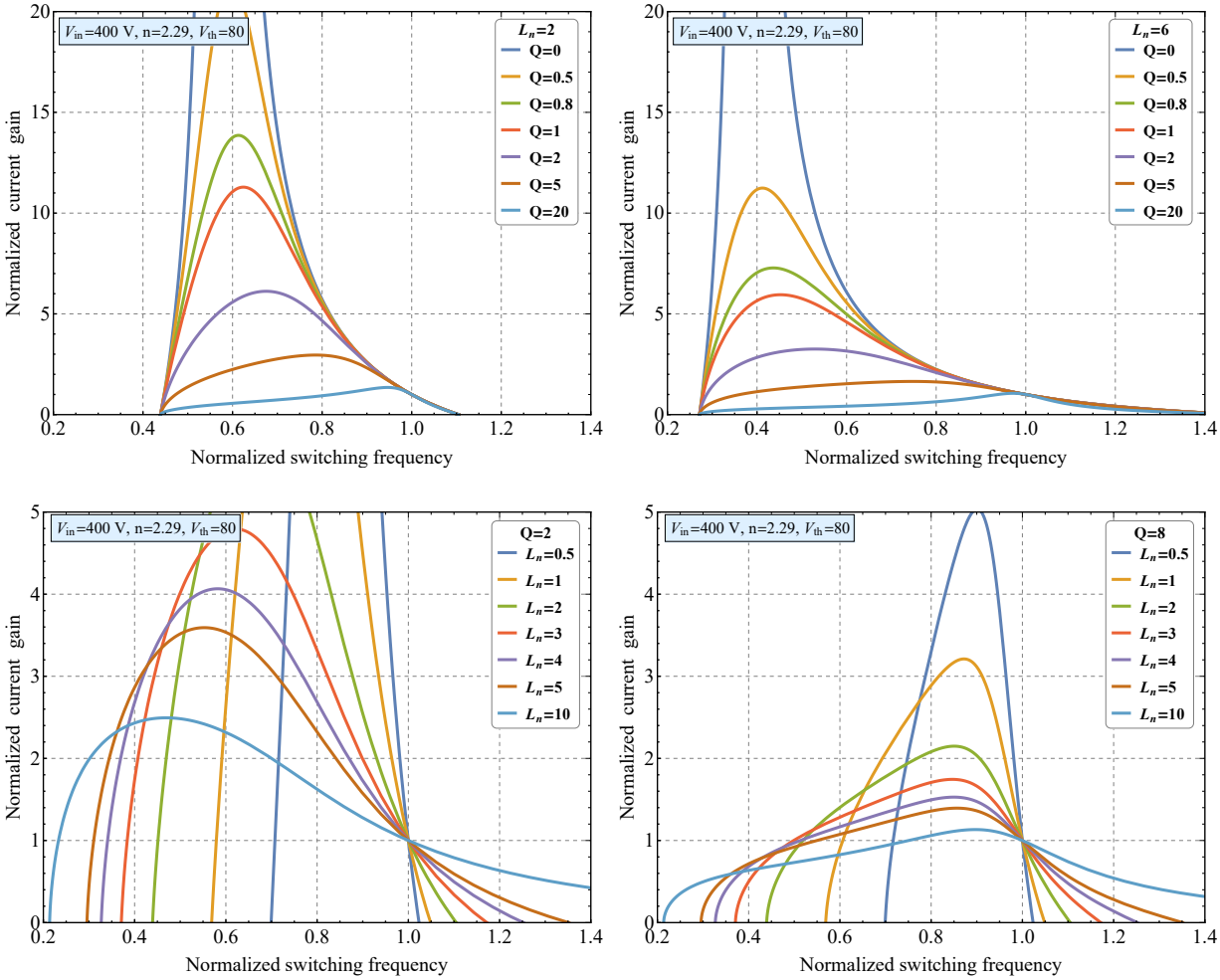
Figure 19 – LLC resonant LED driver equivalent AC circuit.



Source: Author.

In the conclusion, Fig. 20 shows the current gain for the LLC resonant LED driver when different L_n and Q are considered. As can be seen, for certain values of the normalized frequency, the current gain becomes zero, which means that $V_{LED} = V_{th}$ and LED is in off state.

Figure 20 – Current gain characteristic for the LLC resonant converter supplying an LED load.



Source: Author.

2.4.1.2 LLC resonant converter with parasitic components

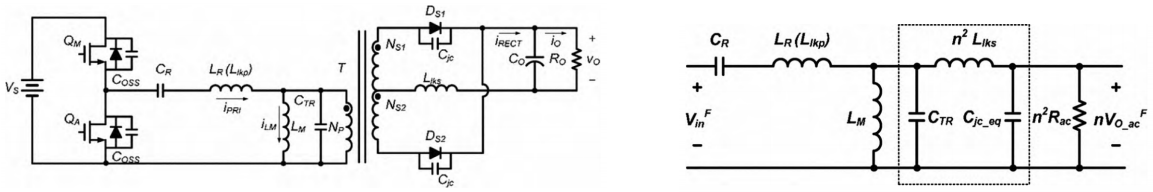
Based on the analysis presented in the last sections, the output voltage and current can be regulated by increasing the LLC f_{sw}. In this analysis, all the elements are considered ideal. However, under some specific scenarios employing experimental results, the conversion ratio increases as f_{sw} increases. To explain this behavior, the LLC resonant converter is analyzed in (B. H. LEE ET AL., 2009) including the main parasitic components. Fig. 21 shows the LLC resonant converter circuit diagram and the AC equivalent circuit when the parasitic components are included in the FHA analysis. In these circuits, C_{oss} is the output capacitance

of the MOSFETs, C_{TR} is the transformer wiring capacitance, L_{lks} is the leakage inductance at the transformer secondary side, and C_{jc} is the junction capacitance of the rectifier diode. Analyzing the effect of each parasitic component, the authors in (B. H. LEE ET AL., 2009) found out that C_{jc} is the main element that contributes to the increase of the LLC gain when f_{sw} increases. This effect increases even more as load decreases.

Figure 21 – Analysis of the LLC resonant converter including parasitic components.

(a) – Circuit diagram of LLC.

(b) – AC equivalent circuit.



Source: (B. H. LEE ET AL., 2009)

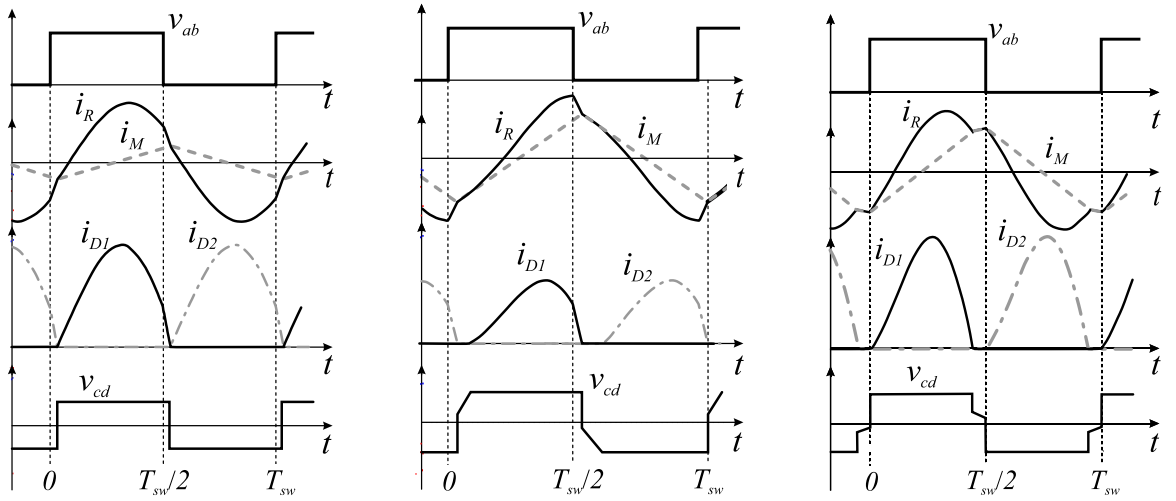
2.4.1.3 Final remarks on FHA

During PFM, the LLC resonant converter f_{sw} is changed to regulate the output voltage and current. For applications that demand a wide operating range, the f_{sw} moves away from f_o. Under this condition, the FHA method becomes less accurate (SIMONE ET AL., 2006), (X. FANG, HU, Z. J. SHEN ET AL., 2012), (R. YU ET AL., 2012) and (DENG ET AL., 2015). Operating beyond f_o, the resonant tank current and voltages present high-order-harmonic components, which also transfer power. Remember that in the FHA, only the fundamental components are considered. Fig. 22 shows the LLC resonant converter main waveforms for different operating points, above and below f_o. As can be seen, these waveforms are substantially different from sinusoidal ones, which explains the FHA error in predicting the converter behavior for operations beyond the series resonance.

Due to inaccuracy of the FHA approach, it may outcome in an inferior analysis, also leading to a poor design, which may present ZVS failure, low efficiency, magnetic saturation risk, insufficient peak gain, and unpractical f_{sw} range. Besides, many details of the circuit operation in the TD will be lost in the FHA analysis (X. FANG, HU, Z. J. SHEN ET AL., 2012), which are critical to define and evaluate the converter power loss and obtain further insights into the converter behavior. Therefore, to overcome some of these issues, hybrid analysis has been proposed in the literature. For instance, in (IVENSKY ET AL., 2011) adjustments in the load factor (see equation (2.14)) have been proposed after partially analyzing the circuit in the TD. So, this method is named as Frequency domain with partial TD correction (HFTD1). The Frequency domain with complete TD correction (HFTD2) is presented in (J. LIU ET AL.,

Figure 22 – LLC resonant converter main waveforms operating away from the main resonance.

(a) – $f_{sw} > f_o$ at heavy loads. (b) – $f_{sw} > f_o$ at light loads. (c) – $f_{sw} < f_o$ at moderate loads.



Source: Author.

2017), where both resonant and load factors are adjusted. Both HFTD1 and HFTD2 increase the FHA accuracy; even so, some operation modes can not be predicted, which can not be neglected in the accurate analysis.

Finally, to overcome these issues, it is noticed in the literature a current effort in dealing with the LLC resonant converter TD analysis, which allows an accurate analyses of the LLC resonant converter regardless of its operating condition.

2.4.2 Time-domain or operation modes analysis

In the last years, several studies have been proposed the analysis of resonant converters in the TD. Because of the reduced number of assumptions in TD analysis, an outstanding accuracy is achieved regardless of the resonant filter parameters and operating conditions. For the sake of clarity, it is important to say that in the TD analysis of power electronics converters, the converter current and voltages are derived in reference to time considering the steady-state operation.

As stated by (GLITZ ET AL., 2019), the TD analysis allows for the behavior of converters to be studied under different design parameters and operating conditions without employing simulation software. While FHA is the traditional method for predicting the converter's behavior, it simplifies the obtained waveforms to the degree that they are not useful for enhanced analysis and design procedures.

Regarding the LLC resonant converter steady-state TD analysis, several studies have

been originated from the methodology proposed in (LAZAR ET AL., 2001). The state-of-the-art technology of the TD analysis of the LLC can be summarized by (LAZAR ET AL., 2001), (T. LIU ET AL., 2006), (X. FANG, HU, Z. J. SHEN ET AL., 2012), (R. YU ET AL., 2012), (H. WANG E BLAABJERG, 2014), (DENG ET AL., 2015), (Z. FANG, CAI ET AL., 2015), (SHAFIEI ET AL., 2017), (MUMTAHINA ET AL., 2018). In these studies, the following common approach is noticed: (**i**) All the LLC resonant stages are presented, and for each stage, the differential equations that rule the evolve of a partial number of the system states are shown; (**ii**) Differential equations for each resonant stage are solved analytically; (**iii**) The different operation modes[2] of the converter are presented with the respective main waveforms; (**iv**) For each operation mode, the constraint conditions that defines the operation mode boundaries are presented; (**v**) After these sections, each work follows the own focus, usually proposing a new design procedure.

2.4.2.1 LLC resonant converter steady-state time-domain analysis

In this section, the TD analysis of the LLC resonant converter is described step-by-step.

Resonant stages

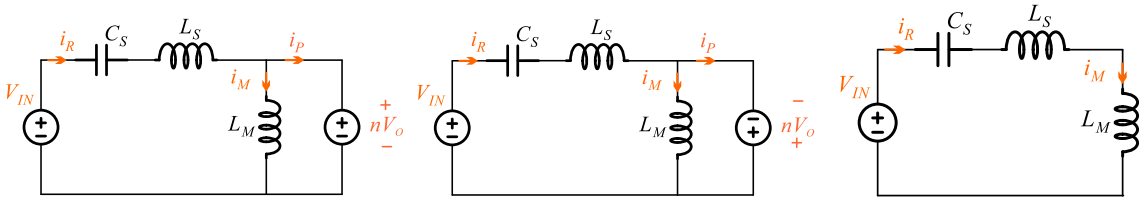
Analyzing one switching cycle ($T_{sw} = 1/f_{sw}$) of the ideal LLC converter in the steady-state operation, six possible resonant stages for the HB resonant filter are identified. This resonant stages are classified as a function of L_M voltage (v_{LM}) and HB switches S_1 and S_2 state. However, assuming that the LLC converter uses PFM with 50% duty-cycle, the resonant tank current and voltage waveforms are symmetrical to the other half-switching-cycle (X. FANG, HU, Z. J. SHEN ET AL., 2012). Thus, it is possible to simplify the LLC examination focusing the analysis in the resonant stages that occurs during the first half-switching-cycle, defined when S_1 is ON and S_2 is OFF (See Fig. 14).

Fig. 23 shows the LLC converter equivalent circuit for each resonant stage. The stage characterized by L_M positive clamped $v_{Lm} = nV_O$, is named Stage P, where V_O is the output average voltage, and n the transformer turns ratio. In the same way, for L_M negative clamped $v_{Lm} = -nV_O$, the stage is named N. Finally, the stage where $|v_{Lm}| \leq nV_O$ is named O.

[2] An operation mode is defined as a single sequential of the different resonant stages

Figure 23 – Equivalent circuit for each resonant stage of the LLC resonant converter.

(a) – Stage P. (b) – Stage N. (c) – Stage O.



Source: Author.

Stage P

During stage P, HB switch S1 is ON, and diode D1 conducts. The output voltage reflected to the primary side is applied across L_M. Consequently, the magnetizing inductance current i_M increases linearly. The resonant filter current i_R is a function of the resonance between L_S and C_S. Since D_1 is on, it means that $i_P = i_R - i_M > 0$, and consequently, the primary energy is transferred to the output side.

Analyzing the equivalent circuit of stage P in Fig. 23(a), the following can be obtained:

$$L_S \frac{di_R(t)}{dt} + v_{Cs}(t) = V_{IN} - nV_O \tag{2.23a}$$

$$i_R(t) = i_{Cs}(t) = C_S \frac{dv_{Cs}(t)}{dt} \tag{2.23b}$$

$$v_{Lm}(t) = nV_O = L_M \frac{di_M(t)}{dt} \tag{2.23c}$$

Applying Laplace transformation in (2.23), the following solutions are obtained:

$$I_R(s)sL_S + V_{Cs}(s) = V_{IN} - nV_O + L_S I_{R0} \tag{2.24a}$$

$$I_R(s)\frac{1}{sC_S} - V_{Cs}(s) = -\frac{V_{Cs0}}{s} \tag{2.24b}$$

$$I_M(s)sL_M = nV_O + L_M I_{M0} \tag{2.24c}$$

Where I_{R0}, V_{Cs0}, and I_{M0} are the initial conditions for the resonant tank current (i_R), series resonant capacitor voltage (v_{Cs}), and magnetizing inductance current (i_M), respectively. The angular resonant frequency is given by $\omega_o = 2\pi f_o$.

Applying the inverse Laplace to 2.24, the TD solution for each state-variable is obtained, given by (2.25). It should be noticed that these equations determine the evolve of each state-variable solely during stage P.

$$i_R(t) = \frac{I_R(0)L_S + V_{IN} - nV_O}{L_S}\cos(\omega_o t) - \frac{V_{Cs}(0)}{L_S\omega_o}\sin(\omega_o t) \tag{2.25a}$$

$$v_{Cs}(t) = V_{Cs}(0)\cos(\omega_o t) + (I_R(0)L_S + V_{IN} - nV_O)\omega_o \sin(\omega_o t) \tag{2.25b}$$

$$i_M(t) = I_M(0) + \frac{nV_O}{L_M}t \tag{2.25c}$$

Stage N

During stage N, HB switch S1 is ON, and diode D2 conducts. Thus, the output is reflected to the primary side in negative polarity. Consequently, i_M decreases linearly. Similarly, as in stage P, i_R is essentially determined by the resonance between L_S and C_S. In stage N, the primary energy continues to be transferred to the output side, however $i_P < 0$. To obtain the TD equation for each state-variable during stage N, the equivalent circuit shown in Fig. 23(b) must be analyzed. This solution is omitted here since it can be found in mentioned studies that analyze the LLC in the TD.

Stage O

Fig. 23(c) shows the equivalent circuit for the resonant stage O. During this stage, HB switch S1 is on, and D_1 and D_2 are off, and consequently, no energy is transferred to the output. In this stage, there is a resonance among L_S, L_M and C_S. Furthermore, in stage O, the $i_R = i_M$, and the voltage across L_M is lower than $|nV_O|$. The TD solution is obtained following the same procedure employed in stage P and stage N.

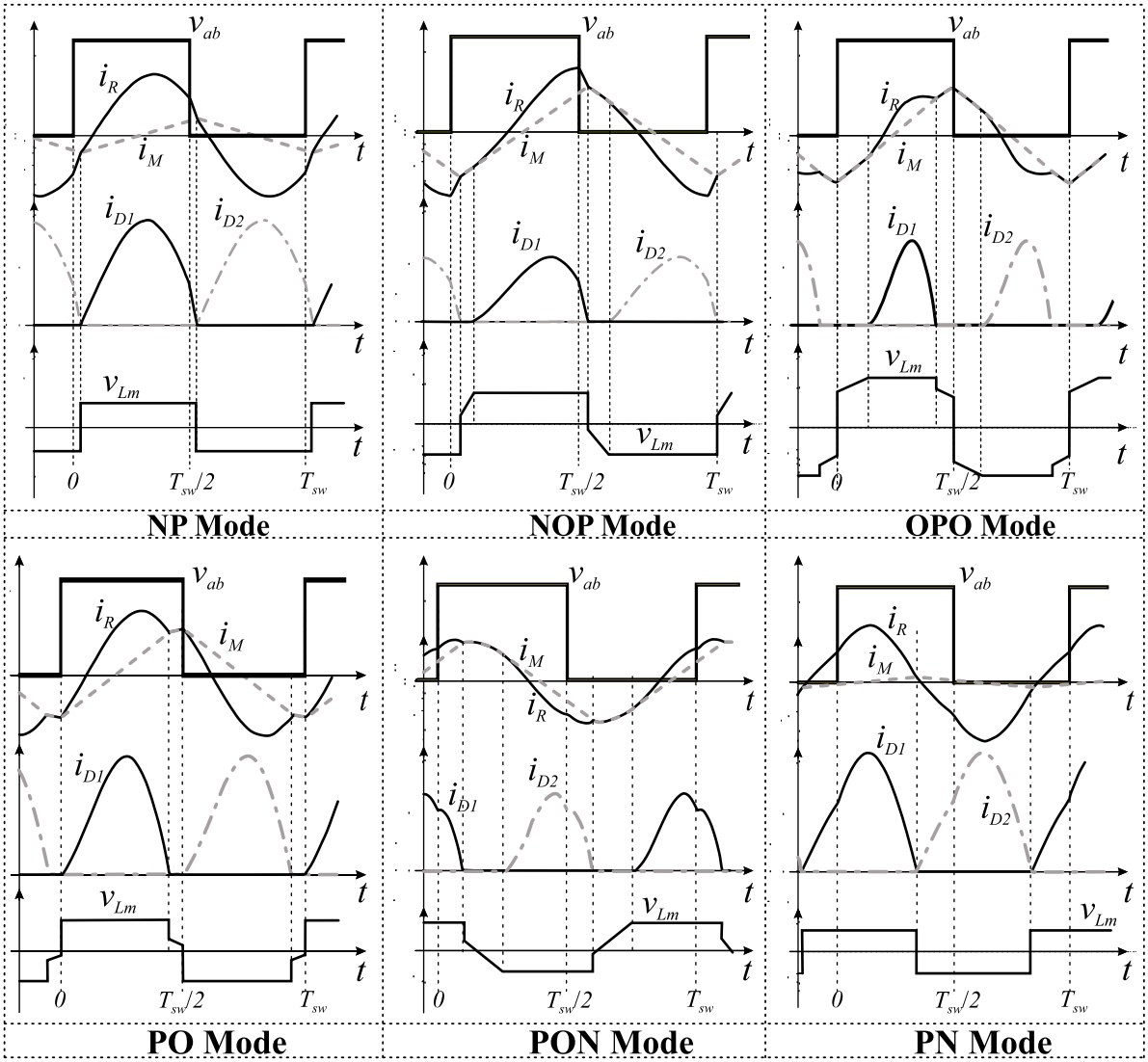
Operation modes

Different successive combinations of the resonant stages (P, N, and O) in the first half-switching-cycle (S1 on, and S2 off) define the LLC converter operation modes. For instance, PO mode indicates that in the first step, the resonant tank operates at stage P and then enters to stage O (second step), which is finished at $T_{sw}/2$. It should be noticed that due to the aforementioned symmetrically behavior of a resonant converter with a constant 50% duty-cycle operation, only the stages in the first half-switching-cycle are used to define and analyze each operation mode of the LLC converter.

For the ideal LLC resonant converter supplying a resistive load, there are six[3] main operation modes: PO, PON, PN, NP, NOP, and OPO also previously identified in (LAZAR ET AL., 2001), (X. FANG, HU, Z. J. SHEN ET AL., 2012), (Z. FANG, CAI ET AL., 2015) and (DENG ET AL., 2015). Fig. 24 shows the LLC resonant converter main waveforms for the main different operation modes, where t_0 refers to the time 0, which is in phase with the switch S_1 gate signal v_{GS1}, and T_{sw} is the switching period. As it can be seen, each mode has the own voltage and current behavior. Besides, each operation mode is constrained by the boundary

[3]Some other modes exist in a low-frequency region, which might have more than three stages in half-switching-cycle. These modes are usually neglected since they occur in the ZCS region. Commonly, the LLC converter is designed to operate in the ZVS region for power efficiency considerations.

Figure 24 – LLC resonant converter main waveforms for the typical operation modes.



Source: Author.

conditions at the joints of adjacent stages and at the switching instants (X. FANG, HU, Z. J. SHEN ET AL., 2012). The incidence of each mode for a given LLC resonant converter is a function of the resonant filter, switching frequency, load condition, and input voltage. Thus, all these variables have to be taken into account under the steady-state TD solution and analysis of the converter.

Considering the symmetrical behavior of the LLC converter, the end value of the states should be opposite to their initial values (X. FANG, HU, Z. J. SHEN ET AL., 2012). This condition, given by (2.26), can be easily noticed in the waveforms presented in Fig. 24.

$$i_R(0) = -i_R(T_{sw}/2) \tag{2.26a}$$
$$v_{Cs}(0) = V_{IN} - v_{Cs}(T_{sw}/2) \tag{2.26b}$$
$$i_M(0) = -i_M(T_{sw}/2) \tag{2.26c}$$

Finally, it is necessary to set up a system of equations to obtain the TD solution for each operation mode. Then, this system of equations must be solved to find the unknown parameters: initial conditions for each state-variable; time instant where two adjacent stages meet; and the output voltage. The arrangement of this system of equations is well-defined for each operation mode.

2.4.2.2 Mode solver and operation mode distribution

Employing the FHA approach, the LLC gain curve is divided into three regions. The knowledge of the characteristics of each region allows one to design and assess the converter in terms of the gain (buck or boost) and switching conditions (ZVS and ZCS). In the TD, each operation mode boundary will define a specific region. It means that in the frequency-gain plot, one specific mode occurs for a certain frequency range and gain. Thus, the characteristics of each mode must be investigated.

Therefore, the LLC operation modes occurrence is evaluated by carefully analyzing the discussion reported in the literature (X. FANG, HU, Z. J. SHEN ET AL., 2012), (DENG ET AL., 2015), (R. YU ET AL., 2012). The NP operation mode occurs solely above the LLC main resonance f_o for the heaviest load. If the load is decreased, the converter enters the NOP mode, which also occurs only above the resonance. During NP and NOP mode, the HB switches operates under ZVS condition. On the other hand, the output rectifier does not present ZCS. For the operation above the resonance with light loads, the converter will run into the OPO mode. In OPO mode, ZVS is achieved on the primary side as well as ZCS is noticed on the secondary side. Regarding the normalized unit gain, operating above the resonance, the LLC behaves as a step-down converter (buck). Besides, the operation modes where the stage O is present are also named as DCM due to the discontinuity in delivering the power to the output, otherwise, the operation mode is defined as CCM.

For the operation below f_o, the OPO mode is also noticed for light load conditions. Increasing the load, the LLC enters into PO mode. Both PO and OPO modes can realize ZVS on the primary side and ZCS on the secondary side. Besides, in these two modes, the LLC behaves as a step-up converter (boost). For the operation below the resonance with heavy loads, the converter can run in PON or PN mode. In fact, PN occurs for the heaviest load. These two modes meet the peak gain and the boundary of ZVS/ZCS condition for HB switches. In

addition, as a function of the f_{sw}, operating at PON or PN mode, the LLC can behave as a step-down or step-up converter.

Finally, it is important to mention that for NP, NOP, OPO, and PO mode, the voltage gain increases monotonically with the decrease of f_{sw}, ensuring closed-loop stability. Table 2 summarize the main observations from the above discussion. Besides, this table presents the alternative names for each LLC operation mode, also found in the literature.

Table 2 – LLC resonant converter operation modes names and occurrence

Operation	**Mode**		**Occurrence**	**Behavior**
CCM above f_o	CCMA	NP	Above f_o for heavy loads	buck
CCM below f_o	CCMB	PN	Below f_o for heavy loads	buck and boost
DCM above f_o	DCMA	NOP	Above f_o for moderate loads	buck
DCM above and below f_o	DCMAB	OPO	Above and below f_o for light loads	buck and boost
DCM below f_o 1	DCM1	PON	Below f_o for moderate loads	buck and boost
DCM below f_o 2	DCM2	PO	Below f_o for moderate loads	boost

Source: Author.

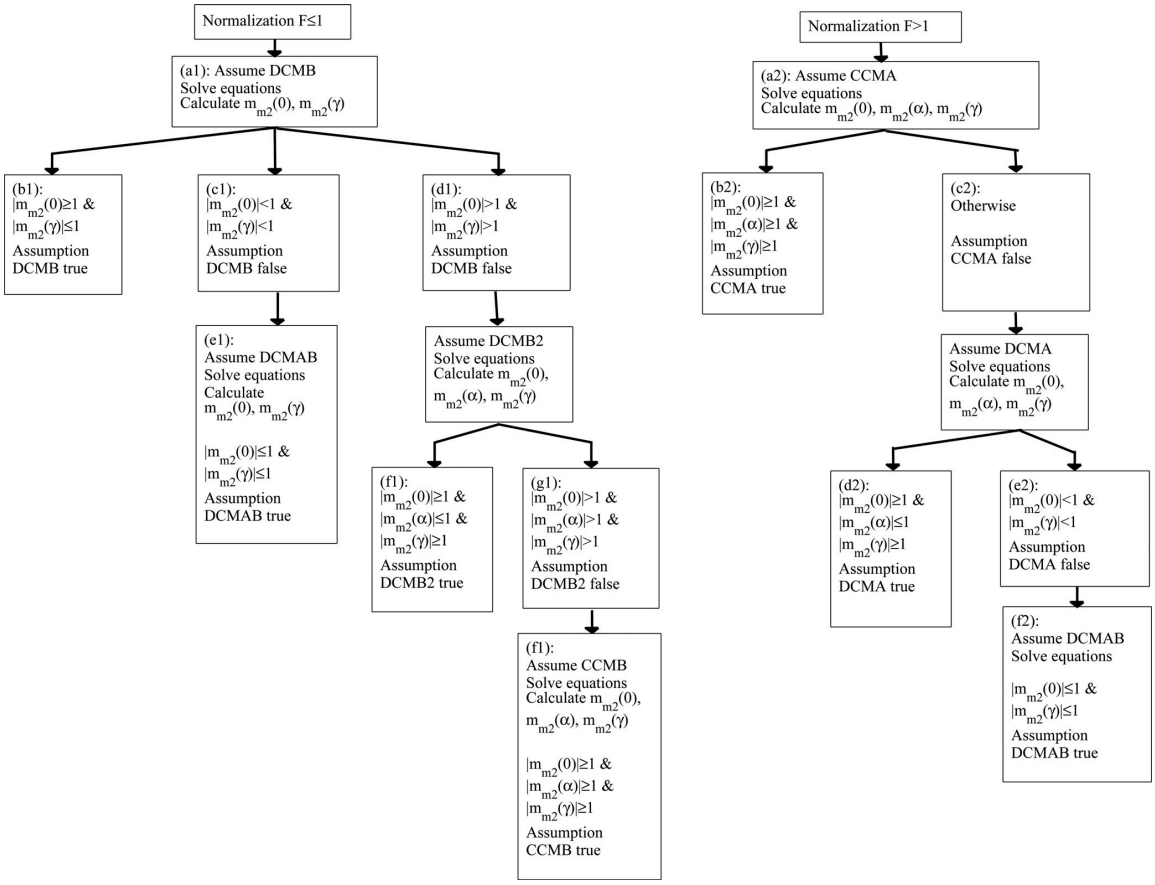
For the LLC resonant converter TD solution at a specific operation point, it is necessary to know the related operation mode, allowing one to employ the correct system of equations. Thus, to automatically define the LLC operation mode, different algorithms have been proposed in the literature (R. YU ET AL., 2012), (Z. FANG, CAI ET AL., 2015), (MUMTAHINA ET AL., 2018). To illustrate the mode solver algorithm, Fig. 25 shows the mode solver proposed by (R. YU ET AL., 2012). As can be seen, in this sort of algorithms, based on initial analysis, one specific operation mode is assumed. Then additional mode indicators are computed to validate the assumed mode or not.

Finally, an exciting tool to analyze the LLC resonant converter is developed by evaluating the operation modes boundary conditions. This analysis outcome in the so-called operation mode map. Therefore, the boundary condition between two adjacent modes must be assessed. For instance, the boundary between NP and NOP mode can be defined by assessing the magnetizing inductance voltage (v_{Lm}) at the transition time (t_{Z1}) between N and P stages. If $v_{Lm}(t_{Z1}) < nVo$, the output rectifier can not be polarized, and the stage O occurs, and so consequently NOP operation mode occurs. Extending this analysis for the different adjacent modes, the LLC operation mode map can be plotted, as shown in Fig. 26.

2.4.2.3 LLC time-domain analysis including parasitic components

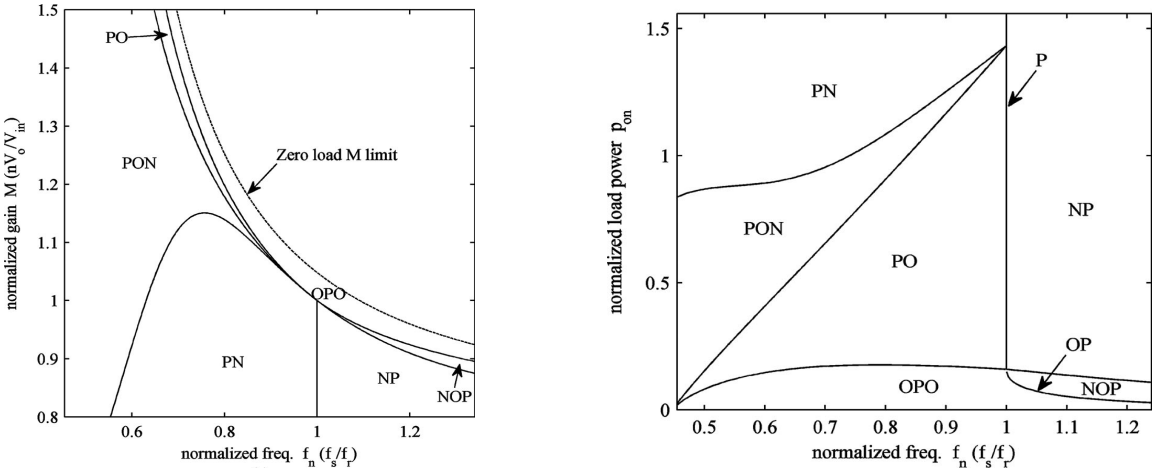
As aforementioned, due to the parasitic components, the LLC has a critical problem for light load conditions operating above the resonance. In this case, the output cannot be regulated at very light load conditions, although the f_{sw} is widely changed. Employing a simplified TD analysis, the output capacitance of the MOSFET, and capacitance of the diode are considered

Figure 25 – LLC Mode solver flowchart.



Source: (R. YU ET AL., 2012).

Figure 26 – LLC resonant converter operation mode map.



Source: (X. FANG, HU, Z. J. SHEN ET AL., 2012).

in (J. H. KIM ET AL., 2011). This article demonstrates that the voltage gain at very light load conditions is reduced due to the effect of C_{oss}. Thus, if C_{oss} is large enough, the voltage gain decreases as f_{sw} increases so that output voltage can be regulated. However, adding extra

capacitance to the HB output will impair the ZVS condition. In (F. LI ET AL., 2019) the LLC resonant converter including additional parasitic components is analyzed for the operation at PO mode. Nevertheless, the TD analysis of the LLC resonant converter, including parasitic components, is not covered adequately in the literature due to the high order of the system and additional resonant stages.

2.4.2.4 LLC resonant LED driver analysis employing TD approach

The TD analysis is the most accurate procedure to analyze the LLC converter. However, TD analyses considering the LED electrical behavior are not yet presented in the literature. For accurate steady-state analysis, it is essential to consider the LED non-linear behavior. Thus, the PWL equivalent circuit should be considered under the TD analysis. For amplitude modulation dimming methods, proper analysis procedures must be employed.

2.4.2.5 Final remarks on time-domain analysis

Considering the literature that deals with LLC converter TD analysis, even that accurate results are obtained in predicting the LLC converter behavior in the TD, there are common approximations that do not allow a general and theoretically exact solution. The main approximations that simplify the analysis but avoid further insights of the converter are: (**i**) Converter output voltage is considered as a constant voltage source (V_O), which does not allow enhance the output filter design and evaluate the output voltage and current ripple, crucial in application such as LED drivers and battery chargers; (**ii**) Voltage and current analysis in all the converter elements is avoided, being analyzed only a partial number of the system states variables; (**iii**) The operation of the LLC converter is given for a 50% duty-cycle with pulse-frequency-modulation (PFM); (**iv**) All elements are considered ideal; (**v**) Load is treated as purely resistive.

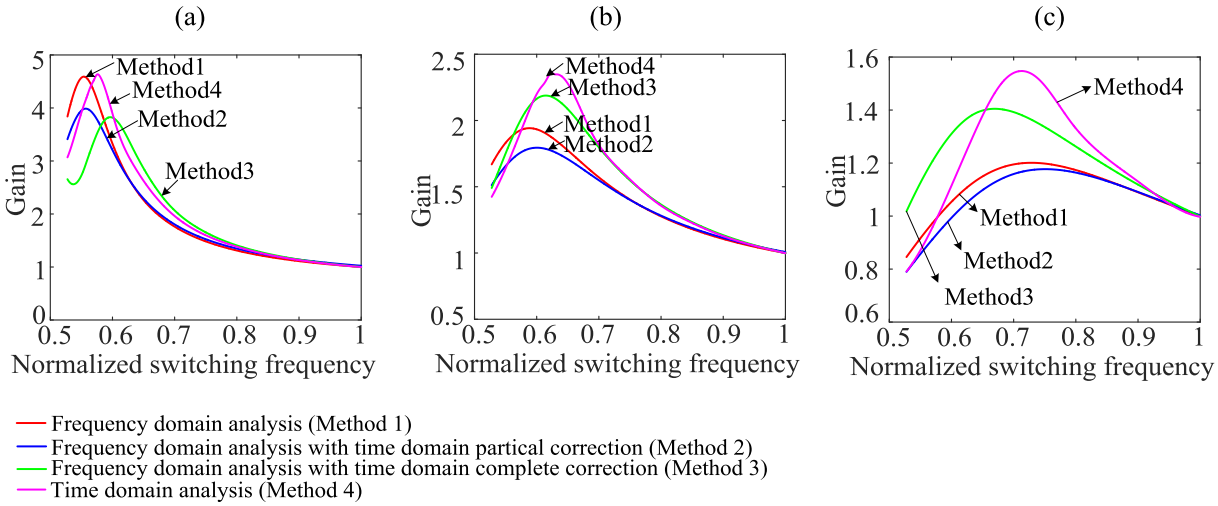
2.4.3 Final remarks on RPC analysis

The main goal in LLC resonant converter analysis is to obtain the gain curve as a function of modulated parameter. In the sequence, it is unquestionable that several analyses can be carried out. Among different modulation strategies, the PFM method is the most commonly employed. Thus, the discussion presented above focused on this method. Similar reviews dealing with LLC modulation and analysis methodologies have been reported in the literature, as can be seen in (WEI, LUO, S. CHEN ET AL., 2019), and (WEI, LUO E MANTOOTH, 2020A).

Fig. 27 shows the comparison for the four main methodologies employed in the LLC resonant converter analysis. Considering that the TD analysis has the same results as the simulation, it is selected as the real behavior of the converter to make the comparison between these different analysis methodologies. Thus, analyzing Fig. 27 it can be seen that for the other three analysis methodologies, errors exist during the whole range, especially when the f_{sw} is away from the main resonant frequency f_o. Specifically, the peak voltage gains of the frequency-domain (FHA) analysis methodologies are smaller than the practical results, which means that the LLC resonant tank potentials are not fully utilized.

As a conclusion of the LLC resonant converter analysis review, it can be noticed that the TD procedure is the most accurate methodology. However, although it has been the focus of numerous analyses, the LLC general TD solution is not completely enclosed due to its complexity given by the multiple resonance nature and its variable structure behavior (resonant stages).

Figure 27 – Accuracy comparison between different analysis methodologies for an LLC resonant converter with $L_M/L_S = 5$ and different Q values: (a) $Q = 0.2$; (b) $Q = 0.5$; (c) $Q = 0.85$.



Source: (WEI, LUO, Z. WANG ET AL., 2021).

2.5 LLC RESONANT POWER CONVERTER DESIGN

A well-designed LLC resonant converter, regardless of its application, has to present over the whole operation window: ZVS operation, enough gain peak, high efficiency, feasible switching frequency range, reduced EMI, and high power density. This section presents the main insights of several design procedures found in the literature. Since the design procedure is closely related to the employed analysis procedure, the design procedures are classified as a function of the analysis methodology.

The converter operation window ranges from the minimum to maximum load over the

minimum and maximum input voltage. The application specifications also define some important conditions that impact the design of the LLC converter. Considering voltage fed LLC converter, the design will be characterized by one of the following scenarios: Constant or Variable average input voltage, with output at: (i) Constant voltage; (ii) Constant current; (iii) Variable voltage; (iv) Variable current; and (v) Variable voltage and current.

Usually, in offline applications, the bus voltage presents some operation range, either given by the bus voltage ripple or variable DC due to the PFC operation. The application strictly defines the output. Battery chargers and LED drivers will present a variable output voltage and variable current. Several other applications require a constant voltage controlled regardless of the load (laptop adapters).

2.5.1 FHA based design procedures

Employing FHA analysis, well-known design procedures are formed for the DC/DC LLC resonant converter (LU ET AL., 2006), (BEIRANVAND ET AL., 2012), (SIMONE ET AL., 2006). FHA-based design procedures are given by few simple equations, which is their main advantage. Design procedures based on FHA analysis are good solutions for simple applications. In this case, the converter usually operates only at nominal conditions or runs around main resonance when submitted to tiny variations at input and output. Specifically, in (LU ET AL., 2006) an optimal design methodology for the LLC operating at f_o is presented. L_M is optimized to reduce conduction losses and ensure ZVS by limiting the HB switches minimum turn-off current. In the sequence, L_n and Q are selected based on the gain curves, where the peak gain and f_{sw} range are assessed.

Employing FHA, a comprehensive analysis and design of the LLC is carried out in (SIMONE ET AL., 2006). The general design criteria are: (i) The converter is designed to work at f_o at nominal input voltage (defines the transformer turns ratio). (ii) The converter must be able to regulate down to zero load at maximum input voltage. (iii) The converter will always work in ZVS in the whole operating range. Then, to accomplish this task, a ten step design procedure is presented. Unfortunately, no experimental results are shown to assess the feasibility of the proposed procedure. The work proposed by (BEIRANVAND ET AL., 2012) deals with LLC design for a wide output voltage ($35-165\ V$) under different load ($0-3\ A$) and input voltages ($320-370\ V$). To enhance the FHA analysis accuracy, for no-load operation, higher-order harmonics are considered. In this procedure, an analysis is carried out examining the output voltage adjustable range as a function of normalized f_{sw}, inductance ratio (L_S/L_M), and quality factor (Q). Power MOSFET peak current and conduction losses under full-load conditions are also evaluated employing the normalized parameters. Similarly, the maximum voltage of the resonant capacitor is also assessed. To improve performance under light load, the input impedance under no load is maximized.

A variable DC-link control approach based on the maximum efficiency point tracking technique has been proposed for an LLC-based battery charger (H. WANG E BLAABJERG, 2014). With this proposed technique, the DC-link voltage always follows the variation of the battery pack voltage, which ensures that the LLC converter is always operating at f_o. Detailed modeling and power loss analysis are provided for the LLC converter operating at f_o. A guideline is detailed to design such an LLC converter operating at maximum efficiency point with the minimum circulating current in the resonant tank while still achieving ZVS. The effectiveness of the designed LLC converter with variable DC-link control is experimentally compared to adopting a fixed DC-link voltage. The experimental results show that the efficiency of the LLC converter can be improved by 2.1% at the heaviest load condition and 9.1% at the lightest load condition.

2.5.1.1 LLC resonant LED driver design based on FHA

The optimal design procedure proposed by (LU ET AL., 2006) is adapted for the LLC resonant LED driver in (WU, 2011A), (WU ET AL., 2011B). To achieve a reliable design, the LED electrical behavior is taken into account during the converter analysis. In (WU, 2011A), the design target is to provide 100% constant current during the whole input and output ranges. The input voltage is given by the bus voltage variation. The output current is regulated in different levels to perform dimming. This input and output variation imposes some difficulties on the design. In order to exemplify this design procedure, Appendix A presents the LLC resonant LED driver analysis and design based on the FHA approach, which follows the procedure proposed by (WU, 2011A), (WU ET AL., 2011B).

The LLC resonant LED driver is reported in several studies, to cite some of them (FENG ET AL., 2014), (ZHAO ET AL., 2014), (C. A. CHENG, H. L. CHENG ET AL., 2014). However, in these studies, the design is usually carried out approximating the LED electrical behavior by a fixed resistor value R_{eq}, defined by the nominal output voltage and current. For the LLC LED driver operating at f_o with a constant input voltage and fixed output current (without dimming), the FHA approach considering the LED as a resistive load presented good accuracy. However, when the f_{sw} moves away from f_o to perform dimming or compensate input voltage disturbances, the behavior predicted by the FHA deviates from the experimentally observed. Thus, the FHA approach becomes unreliable for improved analysis and design methodologies.

For LLC resonant converter design, it is worth mentioning that a resistive load can be employed to approximate the LED electrical behavior. However, this resistance value changes as a function of the LED current and voltage. It means that for each output current, a specific resistance value must be employed.

2.5.2 Time-domain based design procedures

Due to the FHA limited accuracy, design procedures based on the TD analysis have been reported in the literature. In (T. LIU ET AL., 2006), based on the TD analysis, the LLC DC gain curve is derived and analyzed. To evaluate the converter efficiency, primary and secondary switches RMS current are evaluated in a normalized way to infer the conduction losses. However, only the nominal operation condition is evaluated in the design. Primary switches turn-off current and secondary switches turn-off voltage are assessed to evaluate the switching losses. All this evaluation is done for different Q values, assuming constant gain $1,05$ and as a function of $L_n = L_M/L_S$. Finally, the transformer turns ratio is defined taken into account nominal load and middle DC gain. Q and L_n are selected to address the start-up requirements and DC gain range. Furthermore, L_n selection is also supported by the analysis of the resonant tank current, where the L_n that outcome is smaller current for nominal load condition is selected. It is worthy of mentioning that since the TD is employed, a reliable design is achieved.

In (ADRAGNA ET AL., 2009), a novel design methodology for the tank circuit has been proposed that minimizes its reactive energy, still keeping soft-switching all over the specified input voltage and output load ranges. The operation below f_o at the minimum input voltage is pushed considerably close to the boundary with the capacitive-mode operation (ZVS/ZCS boundary) to reduce the reactive energy. In this study, a simplified TD analysis is employed to develop the design procedure. Detailed modeling of the converter and an analysis of the soft-switching condition is addressed by employing simplified TD analysis. Then, the magnetizing inductance value is carefully analyzed to provide enough current gain and ZVS at the most critical point.

A computer-aided design procedure is proposed in (R. YU ET AL., 2012). In this work, a systematic optimization procedure is proposed to optimize the LLC converter efficiency at full-load conditions. The calculated efficiency (at full-load) serves as the objective function to optimize the converter efficiency. The TD analysis of the LLC is employed to compute the converter efficiency. Thus, a mode solver technique is proposed to handle the LLC steady-state solution. The details of design variables, boundaries, equality/inequality constraints, and loss distributions are given. Measured full-load efficiency of 97.07% is achieved compared to the calculated 97.4%. Finally, it can be seen that the proposed optimization procedure is an effective way to design high-efficiency LLC converters.

Employing the TD analysis and dealing with the peak gain, an optimal design procedure for the LLC resonant converter is presented in (X. FANG, HU, F. CHEN ET AL., 2013). As stated by the authors, the optimal resonant tank design can be achieved by appropriately setting the peak gain in the way that the LLC reaches its peak gain under the full-load and minimum f_{sw} condition. Actually, this specific point optimizes the trade-off between minimizing the

conduction loss and maintaining the desired gain range. Besides, to culminate with the filter design, the authors evaluated the influence of varying the resonant circuit parameters on the RMS currents in the resonant tank.

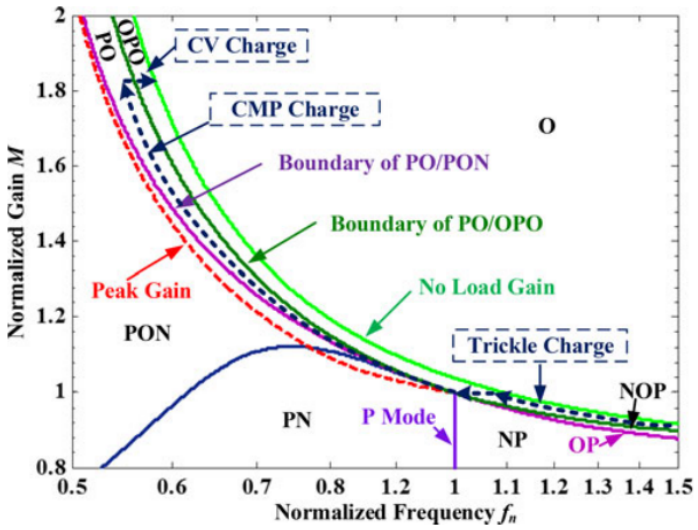
Focusing on the battery charging applications, an interesting design procedure is described in (Z. FANG, CAI ET AL., 2015). In this procedure, a time-weighted average efficiency (TWAE) index is proposed, representing the average weight of conversion efficiency during the battery charging period. This TWAE index is then employed as the objective function to optimize the converter parameters. This means that the whole operating window is taking into account and not only one specific point at rated conditions. To compute the converter power loss and consequently the TWAE, the voltage and current information are derived from the LLC time-domain analysis.

For battery charger applications, the full-load operation is required in a wide output voltage range, which differs from a resistive load with a single nominal condition. Thus, a procedure based on a trajectory design target rather than a single point design target is presented in (DENG ET AL., 2015) for an LLC resonant-based plug-in hybrid electric vehicle (PHEV) battery charger. This design method focuses on restricting the whole charging trajectory within the preferable operation modes that offer the converter soft-switching capability and minimize the circulating energy. The mode boundaries and distribution are obtained from the precise TD model. Then, the LLC converter's operation modes boundaries and mode distribution are discussed to locate the operation trace to the preferable region. The key parameters that affect the designed operating trajectory are identified as the inductance ratio and characteristic impedance. Finally, all the discussion has led to the design of a 6.6 kW, 390 V input, and $250-450$ V output LLC converter that presents soft-switching under all operating conditions achieving 97.96% peak efficiency. Fig. 28 illustrates the charging trajectory within the preferable modes. The charging trajectory includes the trickle charge, constant maximum power (CMP) charge, and constant voltage charge. Also, dealing with LLC-based PHEV battery charger, in (C. SHEN ET AL., 2020), a new design procedure is proposed that restrain the LLC operation only in the PO mode, so achieving soft switching on both primary and secondary sides.

Employing optimization tools, in (MUMTAHINA ET AL., 2018) a design procedure that minimizes the LLC power loss at full load is proposed. The major contribution of this paper is the development of a cost function that incorporates a mode solver for the phase-shifted LLC state equations. The method features automatic detection of the preferred operational mode. Besides, it simultaneously determines the values of the resonant elements and transformer turns ratio for a given power level and voltage transformation ratio.

Taking several conditions into account during the design of the LLC, a complete step-by-step design procedure based on TD analysis is proposed in (WEI, LUO, Z. WANG ET AL., 2021). Restringing the operation to the PO mode, this procedure focus on the worst operation condition. Then, sweeping the inductance ratio and series resonant capacitor, the

Figure 28 – Charging trajectory in the gain-frequency mode boundaries of the LLC resonant converter.



Source: (DENG ET AL., 2015).

following features are assessed: operation mode boundary; voltage stress for resonant capacitor C_S; ZVS operation for primary switches; and resonant tank RMS current. Compared with the existing design methodologies, the proposed one has the advantages of high accuracy and small computation requirement, which makes its application in the industry possible. A $192-W$ experimental prototype was built to validate the effectiveness of the proposed design methodology.

2.5.2.1 LLC resonant LED driver based on time-domain analysis

Several works are dealing with the LLC resonant LED driver analysis, design, modeling, and control. However, usually, the classical FHA is employed due to its simplicity. Therefore, a research gap is identified and will be covered in this thesis. Specifically, the following opportunities for improvement are identified: LLC resonant LED driver TD analysis considering the LED electrical behavior, and LLC resonant LED driver design based on TD-analysis results.

2.5.3 Hybrid FHA and time-domain based design procedures

As aforementioned, to overcome the FHA approach's lack of accuracy, some studies propose to correct the load and/or resonant factor of the LLC gain curve. In (IVENSKY ET AL., 2011), adjustments in the load factor (see equation (2.14)) have been proposed after partially analyzing the circuit in the TD. So, this method is named as Frequency domain with partial TD correction (HFTD1). The Frequency domain with complete TD correction (HFTD2) is

presented in (J. LIU ET AL., 2017), where both resonant and load factors are adjusted. Thus, in the end, by combining time and frequency domain analysis, improved accuracy can be achieved. With a precise gain model, the design results can be more accurate that will address advantages for the performance of the LLC resonant converter, such as efficiency, control, soft switching area, and so on.

2.6 LLC RESONANT CONVERTER DYNAMIC MODELING

The early sections deal with the analysis and design of the LLC resonant converter. However, to put the designed converter to run in practical applications, it is indispensable to implement a control system, regardless if it is feed-forward, feedback, or any other approach. Nevertheless, to design the LLC control system, the dynamic behavior of the converter has to be known in advance. The system dynamic behavior is given by the small-signal model, mathematically represented as a transfer function (TF).

Because of the natural behavior of the resonant converters, their state variables do not have average values as in PWM DC/DC converters. Thus, traditional average state-space averaging (MIDDLEBROOK ET AL., 1976), and circuit averaging (ERICKSON ET AL., 2001), cannot be applied to model the LLC resonant converter. Therefore, several other approaches have been published in the literature: Extended describing function; approach based on the communication theory; sampled-data modeling approach; analysis based on ac-sweep simulation or bench measurement results. It is worthy of mentioning that all these models use numerical solutions instead of analytical solutions. Consequently, no simple equivalent circuit model is available, and no analytical expressions of transfer functions are presented.

Among these modeling approaches, the small-signal modeling technique based on the extended describing function (EDF) concept has been successfully applied to different resonant converters topologies. The EDF technique, systematically introduced by (E. X. YANG ET AL., 1991), is derived from the general procedure given in (SANDERS ET AL., 1991), and corresponds to the most successful approach to model resonant converters. Employing the EDF approach, the LCC resonant converter small-signal model is presented in (E. X. YANG ET AL., 1992A). Similarly, the series and parallel resonant converter small-signal model is described in (E. X. YANG ET AL., 1992B). In these models for the SRC, SPC, and LCC, the model accuracy is evaluated for different switching frequencies, quality factors, and modulation techniques (PWM and PFM). Experimental results show that the dynamic behavior predicted by the model is in agreement with the measured data.

The EDF procedure is given by 7 steps very well defined: **Step 1**: Time variant Nonlinear state-equations; **Step 2**: Harmonic approximation; **Step 3**: Extended Describing Function; **Step 4**: Harmonic balance; **Step 5**: Steady-state operating point; **Step 6**: Perturbation and Linearization of Harmonic balance equations; and **Step 7**: State-space model.

Further details of the EDF procedure, including detailed calculations, are presented (E. X.-Q. YANG, 1994), (AYACHIT, 2011) and (SHAIK ET AL., 2012).

Employing the EDF method, the small-signal modeling of LLC resonant converter supplying a resistive load is presented in (SHAIK ET AL., 2012), (C. H. CHANG, E. C. CHANG ET AL., 2012), (C. H. CHANG, C. A. CHENG ET AL., 2014). In these works, to verify the accuracy of the derived small-signal model, the LLC resonant converter operating around the main resonance and with a resistive load is evaluated. Under this scenario, the model accurately predicts the LLC converter dynamic behavior.

In (MCDONALD, 2014) the EDF method is employed to assess the LLC dynamic behavior under different operating conditions, making variations in the input voltage and load conditions, which push the operation beyond the main resonance. Nevertheless, since only theoretical results are presented, the model accuracy for operation points beyond the main resonance can not be verified. Due to the strong nonlinearity of resonant converters, the accuracy of the EDF method for a wide operation range is questioned in (KHANDEKAR ET AL., 2014). In this way, the authors propose using Least Square Method (LSM) to predict the LLC dynamic behavior.

Although the EDF method is widely used, some outcomes impair the method's practicability. Employing the EDF techniques usually result in high-order TF, which is represented by a set of matrices rather than an equivalent circuit. Consequently, the TF is still derived based on the numerical solution instead of analytical solutions. To overcome this issue, a methodology to simplify the equivalent circuit to obtain a reduced-order decoupled equivalent circuit is proposed by (TIAN, 2015). This simplification is possible by restricting the modulation frequency f_m below the f_{sw}. Thus, for $f_m << f_{sw}$, the authors show that the capacitor dynamic behavior functions as an inductor. So, the capacitors are transformed into equivalent inductors and therefore disappeared in the equivalent circuit, which reduces the order of the model. This procedure is then employed to the SRC in (TIAN, F. C. LEE ET AL., 2016A), where analytical solutions are provided for main the transfer functions of interest. The LLC dynamic behavior is explored in (TIAN, F. C. LEE ET AL., 2016B), and (TIAN, F. C. LEE ET AL., 2020), where analytical TF equations are also provided. In a general way, all the TF match very well with the experimental and simulations verification, except the fact that significant phase discrepancies are observed in the case of LLC.

Also, dealing with the equivalent circuit simplification, alternatives approaches have been proposed. In (Y. MA ET AL., 2020), the LLC circuit is simplified employing Thevenin and Norton equivalent transformation. Then, small-signal perturbations are superimposed in the phasor analysis of the equivalent AC circuit. Based on the homopolarity cycle concept, the small-signal model of the LLC is obtained in (MOHAMMADI ET AL., 2020). In this procedure, the homopolarity cycle concept is employed to obtain the converter behavioral average circuit, considering operations above and below the resonance. In the sequence, small-signal perturbations are applied to the signals of the LLC converter in order to

theoretically obtain the small-signal model of the LLC converter.

Recently, to model the small-signal dynamic behavior of the resonant converters, an alternative approach is proposed employing perturbation on the state plane and describing function (HSIEH ET AL., 2018), (HSIEH ET AL., 2019), (HSIEH ET AL., 2020). For the LLC modeled in (HSIEH ET AL., 2019), the simplified fourth-order model shows good accuracy up to switching frequency.

2.6.1 LLC resonant LED driver dynamic model

To obtain a trustworthy dynamic model of an LED driver, the LED electrical behavior must be carefully analyzed since it can be approximated by *Req* or by a piece-wise linear PWL model. For the buck and boost converters, their dynamic behavior is compared between its operation with equivalent load resistance *Req* and the LED equivalent PWL circuit, respectively in (ALMEIDA, MELLO ET AL., 2013) and (R. L. LIN E Y. F. CHEN, 2009). In these studies, it is shown that *Req* is not suitable to predict the converter dynamic when it is supplying a LED-based load. However, no further analyses are carried out to define the condition wherein the approximation of the LED load by a *Req* could outcome a satisfactory result.

Regarding the LLC resonant LED driver dynamic behavior, where the LED nonlinearity is taken into account during the modeling procedure, there is no analysis reported in the literature, except (MENKE, A. R. SEIDEL ET AL., 2019), being the main approach during the modeling process the approximation of the LED by a pure equivalent resistive *Req* load (Y. WANG, GUAN ET AL., 2015A), (Y. WANG, GAO ET AL., 2016), and (R.-L. LIN ET AL., 2018).

2.7 LLC RESONANT CONVERTER CONTROL SYSTEM

The control system has three fundamental goals: stability, reference tracking, and disturbance rejection. The LLC resonant converter is open-loop stable, then only after doing things to improve reference tracking and disturbance rejection that they become challenging to stabilize (MCDONALD, 2014).

As already discussed, to enhance the offline LED driver reliability and avoid increases in the volume and cost, E-Cap are being substituted by long lifespan F-Cap with reduced capacitance. However, to avoid that ΔV_{BUS} excite throughout the DC/DC stage an output ΔI_{LED} and so deteriorate the ALS operation due to the resultant flicker, the control system of the LED driver has to be properly designed in the way to satisfactory reject ΔV_{BUS} disturbance. This technique is known as active ripple compensation (ARC). In this way, this section aims to review the state-of-the-art technology related to the LLC resonant converter control system, whose design specifications are similar to LED drivers - DC regulation and reduced output

current ripple.

2.7.1 LLC resonant converter with reduced output current ripple

Focusing on the control system of resonant converters, where a reduced output current ripple is required, studies are mainly found in LED drivers and electrical vehicle (EV) battery charger applications. Linear, non-linear and hybrid solutions classify the controller's here assessed.

2.7.1.1 Linear controllers

Employing the classical control theory, in (C. LIU ET AL., 2015) a resonant controller is designed to suppress the low-frequency (LF) current ripple in an LLC resonant converter for EV battery chargers. Also employing the classical control theory, in (MENKE, A. R. SEIDEL ET AL., 2019) the Integrator plus a Quasi-resonant (IQR) controller is designed for the LLC resonant LED driver to achieve reduced ΔI_{LED} over a wide dimming range even with a considerable ΔV_{BUS} at 120 Hz. Nevertheless, in (MENKE, A. R. SEIDEL ET AL., 2019) a deteriorated performance is expected when the LED driver is connected to AC line with frequencies that differ from 60 Hz, since the IQR controller is optimized to reject 120 Hz Δv_{BUS} periodical perturbation. For (C. LIU ET AL., 2015), to obtain a satisfactory performance over a wide operating range, it is assumed that the frequency range variation with battery voltage is stored in a look-up table and compensated through feed-forward.

With a different perspective, in (Z. ZHANG ET AL., 2018) the mechanism of current ripple propagation in a digitally controlled LLC converter battery charger is investigated in three aspects: battery load, quantization error, and double line frequency perturbation at the input. Where to reduce quantization error and attenuate current oscillation, the synchronous frequency dither is proposed.

On the other hand, without compromise with the ripple reduction, a three-pole two-zero (3P2Z) is designed in (JANG ET AL., 2012) and (PIDAPARTHY ET AL., 2015) to secure stability and good performance for the LLC converter over a wide operating range. In these studies, it is initially proved that the small-signal dynamics of the LLC converter vary substantially as operational conditions are changed. Therefore, the worst small-signal dynamic condition is identified and used as the basis for the compensation design.

Notwithstanding, these approaches based on the classical control theory are subjected to an unpredictable and deteriorated performance when the converter is subjected to a wide operating range, since the linear controllers, such as IQR, PR, PI, 3P2Z, and PID are only valid near a particular operating point due to limitations of small-signal models (Z. FANG, J. WANG ET AL., 2018). These constraints are related to the lack of accuracy of the control-to-output

TF in resonant converters when normally the converter operates in frequencies different from f_o. In this way, the same tendency noticed in the LLC analysis and small-signal modeling can also be observed for the LLC converter control system. Classical solutions present satisfactory results when the converter operates around f_o, which accuracy will be lost when the converter diverges from this operating point.

2.7.1.2 Nonlinear controllers

Nonlinear controllers have been proposed in the literature to overcome small-signal model limitations, presenting strong robustness against disturbances, parameters uncertainties, parametric variation, unmodelled dynamics, and load variations. Precisely, to control the DC/DC LLC converter, sliding-mode control is proposed in (H. MA, Q. LIU ET AL., 2012). In this case, the controller operates at two fixed switching frequencies with sliding-mode control implementation. Improved dynamic response against transient load changes is obtained, preserving the closed-loop stability. However, the steady-state output voltage ripple is noticeably higher due to the chattering phenomenon of sliding-mode control.

In (ZHIYUAN HU ET AL., 2015) a bang-bang charge control method for the DC/DC LLC resonant converter is proposed. The proposed method utilizes the series resonant capacitor voltage level to trigger the half-bridge switching actions instead of f_{sw} control. As advantages, the authors claim a simple implementation and fast dynamic performance.

A robust controller is proposed in (NISHIMURA ET AL., 2012) to suppress the sudden output voltage and current variations in the LLC resonant converter. To enhance the converter efficiency under light load conditions, the burst mode control for the LLC resonant converter is assessed in (FENG ET AL., 2013) and (FENG ET AL., 2014). Actually, these studies employ trajectory control to adapt the switching pattern during the burst-on time, achieving high efficiency and reduced output voltage ripple.

Concerned with the limitations of typical linear control methods for the LLC resonant converter, the load feedback linearization control strategy is proposed in (Z. FANG, J. WANG ET AL., 2018). Compared with the classic PI controller, the feedback linearized control strategy achieves better performance by eliminating the converter intrinsic nonlinear characteristic. In (BUCCELLA ET AL., 2015), an observer-based controller is proposed, a better dynamic response is obtained compared to the traditional PID controller. However, ARC performance is not evaluated.

Dealing with DC/DC LLC converter supplying an LED load, the model reference adaptive controller (MRAC) is employed in (MENKE, TAMBARA AND SEIDEL, 2018). The MRAC is employed in order to overcome the drawback of closed-loop control system with changeable controller gains, which are needed to obtain a good performance at different operating points of the converter. The MRAC is designed to maintain the average LED current

regulated at the reference value, which is changed to obtain LED current amplitude modulation, consequently dimming. Furthermore, to avoid LED current modulating, raised from the unavoidable bus voltage ripple in an off-line LED driver, the adaptive controller algorithm measures the bus voltage ripple and adapts the control action in a way to attenuate its effect in the output LED current. Experimental results show the feasibility of adaptive control applied to the LED driver. Nevertheless, the complexity of this controller can impair the LED driver feasibility.

Nevertheless, compared to the linear compensation, the performance of the nonlinear controller is still undesirable in terms of dynamic response and/or steady-state and/or output ripple reduction. Besides, these nonlinear techniques usually require more computations to be done during the control law execution period, or the computations need to be done at the switching frequency of the converter, which is high (>100kHz) in resonant converters. Consequently, a high-performance digital processor is required, increasing the costs becoming impracticable for ALS. In this way, arguably the main challenge is to design a control system that is capable of maintaining I_{LED} controlled over a wide dimming range, attenuate LF current ripple excited by Δv_{BUS}, and hand over a good overall dynamic performance simultaneously without employing control systems that demand high-speed data processing.

2.7.1.3 Adaptive Periodic Disturbance Rejection

Additionally, to improve the nonlinear controllers' performance in rejecting periodic disturbances, the adaptive periodic disturbance rejection (APDR) controller has been developed for active noise, and vibration control applications (BODSON ET AL., 1997), (PIGG ET AL., 2006), (W. KIM ET AL., 2011). However, in the reported APDR controllers, the disturbance frequency and plant gain must be estimated. Therefore, these proposals can not be directly employed in LLC resonant LED drivers due to their intricate design and implementation difficulty using low-cost MCUs.

2.7.2 Final remarks on the LLC resonant control

As a conclusion of the previous exposition, the main challenge on current-controlled LED driver conception is the design of a stable control system that is capable of regulating the LED average current (I_{LED}) over a wide dimming range, attenuate low-frequency ($< 120\ Hz$) current ripple excited by ΔV_{BUS}, and provide to the driver a transient response with a reduced overshoot to avoid electrical stress in the LED, and a short settling time, preserving overall a simple implementation simultaneously.

2.8 FINAL REMARKS

This chapter presented a comprehensive overview of the LLC resonant converter modeling, analysis, design, and control. Besides, the LLC resonant converter applied in the LED driver is also reviewed.

This review shows that the FHA is the procedure usually employed to analyze the LLC converter regardless of the application. The FHA approach is a simple and accurate methodology for the operation around the main resonance. For the operation beyond the main resonance, it is noticed that the FHA presents significant errors in predicting the converter behavior. To overcome this issue, the TD analysis is successfully employed. However, due to the complexity involved in the TD analysis of the LLC resonant converter, there are some aspects not entirely enclosed by the literature. For instance, a partial number of state variables is considered, the load is considered essentially resistive load, the output is approximated by a voltage source, between other assumptions. If these assumptions are not considered, the commonly employed methodology to solve the LLC in the TD becomes very complex and laborious. Thus, alternative procedures that solve the LLC in the TD systematically, avoiding further assumptions and laborious analysis, are required. The same conclusions from the LLC analysis can be extended to LLC design. The design procedures derived from the FHA approach are the classical methodologies widely employed in the academy and industry. However, due to the FHA lack of accuracy, a poor design is achieved for applications where a wide operation range is demanded. Therefore, alternative methodologies, based on the TD analysis results, have been proposed. However, optimal solutions for LLC resonant LED drivers based on the TD analysis did not receive proper attention.

As shown in this chapter, the LLC resonant LED driver must be designed as a current-controlled system to feed an LED device properly. To design this control system, it becomes necessary to know the LLC resonant LED driver dynamic behavior as accurately as possible. The EDF method has been successfully employed to predict the dynamic behavior of the LLC resonant converter. However, since the LED electrical behavior is entirely different from a resistive load, it is necessary to include the LED nonlinearity in the modeling procedure.

Finally, focusing on the resonant converter control system, it can be seen that several controllers have been employed, from the simple linear PI to complex non-linear controllers. However, for LED drivers, where the system should preserve a simple implementation, complex controllers must be avoided. On the other hand, linear controllers will present a deteriorated performance when subjected to a wide operation range. Thus, it is identified an opportunity for improvements in this research topic.

3 LLC LED DRIVER SMALL SIGNAL MODELING

This chapter develops the small-signal model (SSM) of the DC/DC LLC resonant converter employed to supply an LED load. The modeling procedure employs the Extended Describing Function Method (EDF). Experimental results show that a SSM with enhanced accuracy is achieved when the LED electrical behavior is approximate by a piece-wise linear circuit instead of the equivalent load resistance R_{eq}. Besides, based on experiential analysis, it is concluded that the proposed model is suitable only for the LLC operating close to the main resonance f_o.[1]

3.1 INTRODUCTION

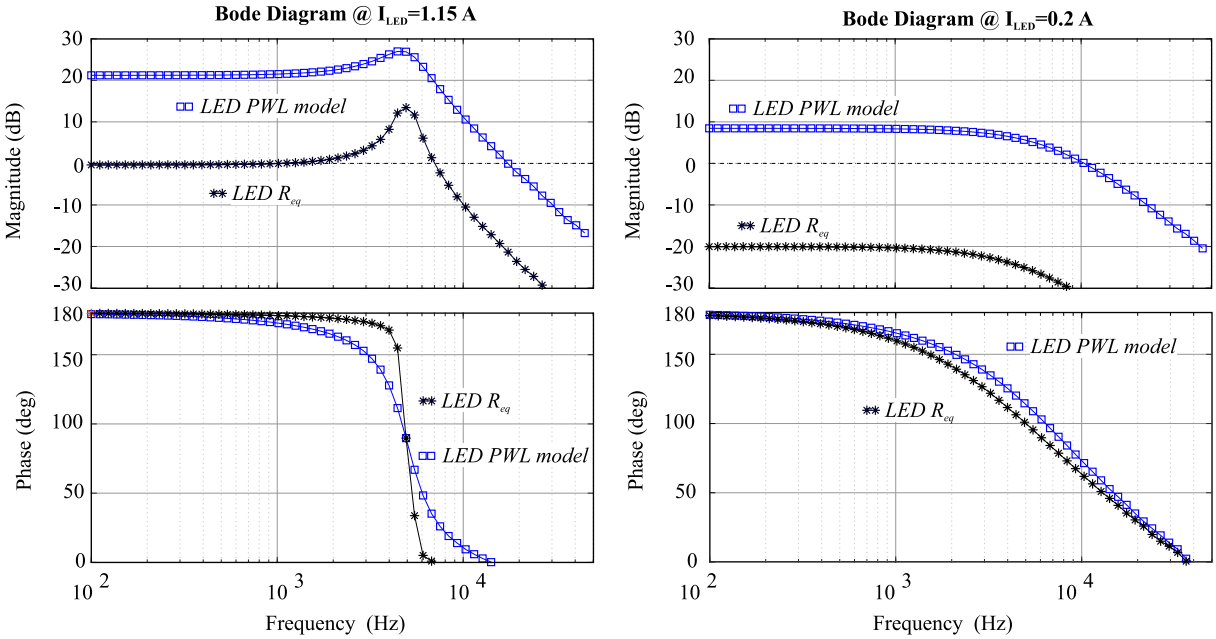
To properly feed an LED device, the LED driver must be designed as a current-controlled system. Therefore, a feedback loop is incorporated into the LED driver control system to regulate the output current. Nevertheless, to design this control system using the classical control theory, it becomes necessary to known in advance the LLC resonant LED driver dynamic behavior as accurately as possible. Mathematically, this dynamic behavior is obtained from the analysis of the small-signal linear relationship between converter output and its control action, yielding the small-signal control-to-output transfer function (FT), also known as the small-signal model (SSM) (TIAN, F. C. LEE ET AL., 2016B).

The dynamic behavior of the buck and boost converters supplying an LED load is investigated in (ALMEIDA, MELLO ET AL., 2013) and (R. L. LIN E Y. F. CHEN, 2009), respectively. In these studies, it is shown that the employment of the LED equivalent load resistance R_{eq} during the modeling procedure is not suitable to predict the real converter dynamic behavior. In order to overcome this issue, the electrical behavior of the LED is approximated by the piece-wise linear (PWL) circuit.

Employing simulation results, Fig. 29 shows the control-to-output TF frequency response of the LLC resonant LED driver when the LED PWL model is employed in comparison to LED load R_{eq}. As can be seen, there is a considerable difference ($> 20\ dB$) in terms of dynamic behavior, which highlights the necessity to develop the LLC resonant LED driver modeling taking into account the LED electrical behavior.

[1] Portions of this chapter have been published in (MENKE, A. R. SEIDEL ET AL., 2019)

Figure 29 – LLC resonant LED driver control-to-output TF frequency response when LED PWL model is employed in comparison to LED load equivalent resistance R_{eq}. Results from ac-sweep simulation on PSIM: Left-trace: Nominal LED current; Right-trace: Minimum LED current.



Source: Author.

3.2 LLC LED DRIVER SMALL SIGNAL MODELING

Owing to their natural operation, the state variables in the resonant converters do not have average values as in PWM DC/DC converters. Thus, traditional averaging techniques cannot be applied to model the LLC resonant converter (MIDDLEBROOK ET AL., 1976), (SHAIK ET AL., 2012). As an alternative, the small-signal modeling approach based on the extended describing function (EDF) concept has been successfully applied to different resonant converters topologies (E. X. YANG ET AL., 1992A) (E. X.-Q. YANG, 1994). Employing the EDF method, the SSM of LLC resonant converter supplying a resistive load is presented in (SHAIK ET AL., 2012), (C. H. CHANG, E. C. CHANG ET AL., 2012), (C. H. CHANG, C. A. CHENG ET AL., 2014). However, the SSM of the LLC converter considering the LED load dynamics and further analysis has not been described in the literature, except by (MENKE, A. R. SEIDEL ET AL., 2019), becoming the focus of this chapter.

The small-signal modeling procedure presented in this chapter follows (SHAIK ET AL., 2012), (C. H. CHANG, E. C. CHANG ET AL., 2012), where the main difference lies in the load's electrical model. This chapter does not aim to define the best modeling procedure (EDF or counterparts) or propose new modeling procedures. The goal is to develop a dynamic model for the LLC resonant LED driver with enhanced accuracy by considering the LED PWL model

instead of its R_{eq}. Therefore, this section follows presenting the step-by-step development of the modeling procedure.

3.2.1 Nonlinear state-space equations

Fig. 30 shows the equivalent circuit of LLC resonant LED driver considering the LED equivalent PWL circuit - Ideal diode in series with LED series resistance r_d and device forward voltage drop V_{th}, where r_d and V_{th} are defined in Fig. 6 as a function of I_{LED}. Besides, in Fig. 30, r_C is the equivalent series resistance (ESR) of output capacitor (C_O), and r_S the series inductor (L_S) DC resistance. The voltage $v_{ab}(t)$ is obtained from the HB switches (S_1, S_2) alternately conducting. Neglecting ΔV_{BUS}, the $v_{ab}(t)$ amplitude is given by the bus voltage V_{BUS}.

The system state equations are obtained by applying Kirchhoff's voltage and current laws on the LLC resonant LED driver equivalent circuit shown in Fig. 30. For the network involving v_{ab}, (3.1.a) is obtained. The resonant filter current i_R is given by (3.1.b), and transformer primary side voltage can be defined by (3.1.c).

$$v_{ab}(t) = L_S\frac{di_R(t)}{dt} + r_S i_R(t) + v_{Cs}(t) + L_M\frac{di_M(t)}{dt} \tag{3.1a}$$

$$i_R(t) = C_S\frac{dv_{Cs}(t)}{dt} \tag{3.1b}$$

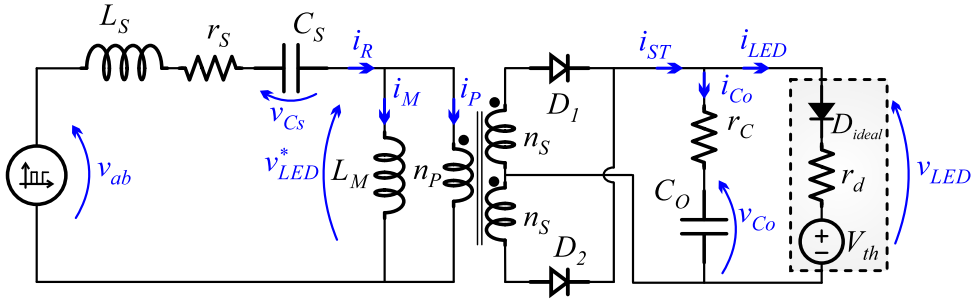
$$L_M\frac{di_M(t)}{dt} = sign(i_P(t))v^*_{LED}(t) \tag{3.1c}$$

where:

$$sign(i_P(t)) = \begin{cases} -1 & \text{if} \quad (i_R(t) - i_M(t)) < 0, \\ 1 & \text{if} \quad (i_R(t) - i_M(t)) \geq 0. \end{cases} \tag{3.2}$$

Analyzing the loop composed by C_O and LED equivalent circuit, (3.3.a) is obtained. The secondary's total rectified current i_{ST} is given by $i_{LED} + i_{Co}$, which is defined by (3.3.b). The LED module voltage v_{LED} is given by (3.3.c).

Figure 30 – Schematic diagram of LLC resonant converter supplying an LED load.



Source: Author.

$$v_{LED}(t) = r_C i_{Co}(t) + v_{Co}(t) = r_{ac} i_{LED}(t) + V_{th} \tag{3.3a}$$

$$i_{ST}(t) = \frac{C_O dv_{Co}(t)}{dt}\left(1 + \frac{r_C}{r_{ac}}\right) + \frac{v_{Co}(t)}{r_{ac}} - \frac{V_{th}}{r_{ac}} \tag{3.3b}$$

$$v_{LED}(t) = i_{ST}(t) r_C^* + \left(\frac{r_C^*}{r_{ac}}\right) V_{th} + \left(\frac{r_C^*}{r_C}\right) v_{Co}(t) \tag{3.3c}$$

where $r_{ac} = r_d$, and

$$r_C^* = \frac{r_C r_{ac}}{r_C + r_{ac}} \tag{3.4}$$

The LED current (i_{LED}), which is the output variable of interest is defined by (3.5).

$$i_{LED}(t) = \frac{i_{ST}(t) r_C^*}{r_{ac}} + \frac{v_{Co}(t)}{r_{ac} + r_C} - \frac{V_{th}}{r_{ac} + r_C} \tag{3.5}$$

3.2.2 Harmonic approximation

Under steady-state operation, i_R, i_M, and v_{Cs} are assumed to be nearly sinusoidal. Thus, these current and voltage waveforms are approximated by its fundamental harmonic term through the Fourier series, which is used to decompose these periodic signals into a sum of sines and cosines, as following:

$$i_R(t) = i_S(t)\sin(\omega_S t) - i_C(t)\cos(\omega_S t) \tag{3.6a}$$

$$i_M(t) = i_{MS}(t)\sin(\omega_S t) - i_{MC}(t)\cos(\omega_S t) \tag{3.6b}$$

$$v_{Cs}(t) = v_S(t)\sin(\omega_S t) - v_C(t)\cos(\omega_S t) \tag{3.6c}$$

where ω_S is the converter angular f_{sw}; and $i_S(t)$, $i_C(t)$, $i_{MS}(t)$, $i_{MC}(t)$, $v_S(t)$, and $v_C(t)$ are the harmonic components amplitude, also denoted as envelope terms. These envelope terms are considered slowly time-varying (E. X. YANG ET AL., 1991) (E. X. YANG ET AL., 1992A),(E. X. YANG ET AL., 1992B). In this way, the dynamic behavior of these terms can be investigated when the system is modulated.

To start with the assessment of the envelope terms dynamic behavior, the derivatives of resonant current and voltage defined in (3.6) are obtained, given by (3.7).

$$\frac{di_R(t)}{dt} = \left(\frac{di_S(t)}{dt} + \omega_S i_C(t)\right)\sin(\omega_S t) - \left(\frac{di_C(t)}{dt} - \omega_S i_S(t)\right)\cos(\omega_S t) \tag{3.7a}$$

$$\frac{di_M(t)}{dt} = \left(\frac{di_{MS}(t)}{dt} + \omega_S i_{MC}(t)\right)\sin(\omega_S t) - \left(\frac{di_{MC}(t)}{dt} - \omega_S i_{MS}(t)\right)\cos(\omega_S t) \tag{3.7b}$$

$$\frac{dv_{Cs}(t)}{dt} = \left(\frac{dv_S(t)}{dt} + \omega_S v_C(t)\right)\sin(\omega_S t) - \left(\frac{dv_C(t)}{dt} - \omega_S v_S(t)\right)\cos(\omega_S t) \tag{3.7c}$$

3.2.3 Extended describing function

One of the most important steps of the modeling procedure is to represent the nonlinearity of the state-space equations by approximated slowly varying terms (E. X. YANG ET AL., 1991). To tackle this task, the EDF concept is employed to approximate the nonlinear terms v_{ab}, $sign(i_P)$ and i_{ST} by their fundamental sine and cosine components or by the DC terms (E. X. YANG ET AL., 1992B), as given by (3.8).

$$v_{ab}(t) = f_1(d, V_{BUS})\sin(\omega_S t) \tag{3.8a}$$

$$sign(i_P)v^*_{LED} = f_2(i_{SS}, i_{SP}, v^*_{LED})\sin(\omega_S t) - f_3(i_{SC}, i_{SP}, v^*_{LED})\cos(\omega_S t) \tag{3.8b}$$

$$i_{ST}(t) = f_4(i_{SS}, i_{SC}) \tag{3.8c}$$

These $f_k(*,*)$ functions above, are called EDFs (E. X. YANG ET AL., 1991), and it can be calculated by Fourier expansions for the nonlinear terms. The EDF is so-called once it considers multiple inputs and outputs instead of a single input as it is done on Describing Function. Thus, calculating the fundamental component of $v_{ab}(t)$, $sign(i_P)v^*_{LED}$ and the DC component of i_{ST}, the EDFs are obtained as given by (3.9).

$$f_1(d, V_{BUS}) = \frac{2V_{BUS}}{\pi}\sin\left(\frac{\pi d}{2}\right) = v_{es} \tag{3.9a}$$

$$f_2(i_{SS}, i_{SP}, v^*_{LED}) = \frac{4}{\pi}\frac{i_{PS}}{i_{PP}}v^*_{LED} \approx \frac{4n}{\pi}\frac{i_{PS}}{i_{PP}}v_{Co} = v_{PS} \tag{3.9b}$$

$$f_3(i_{SC}, i_{SP}, v^*_{LED}) = \frac{4}{\pi}\frac{i_{PC}}{i_{PP}}v^*_{LED} \approx \frac{4n}{\pi}\frac{i_{PC}}{i_{PP}}v_{Co} = v_{PC} \tag{3.9c}$$

$$f_4(i_{SS}, i_{SC}) = \frac{2}{\pi}i_{ST} \tag{3.9d}$$

Where d is the HB duty-cycle, i_{PS} and i_{PC} are the sine and cosine components of the transformer primary current, respectively; i_{SS} and i_{SC} are the sine and cosine components of the transformer

secondary current, respectively; and i_{PP}, defined in (3.10), is the total current in transformer primary side. Furthermore, v_{es}, v_{PS}, and v_{PC} are respectively the sine component of v_{ab}, and sine and cosine component of transformer primary voltage.

$$i_{PP} = \sqrt{(i_{PS})^2 + (i_{PC})^2} \tag{3.10a}$$

$$i_{ST} = \sqrt{(i_{SS})^2 + (i_{SC})^2} = n\sqrt{(i_{PS})^2 + (i_{PC})^2} = n i_{PP} \tag{3.10b}$$

It is essential to mention that the EDFs are calculated assuming the LLC operating at the main resonance frequency f_o. Thus, when f_{sw} diverges from f_o, the model starts to present deviations once the waveforms shape changes and, consequently, their fundamental and DC approximation. In this way, additional attention has to be given to the analysis when f_{sw} is far from f_o, once it is expected a reduce accuracy for the LLC resonant converter SSM.

3.2.4 Harmonic balance

Harmonic balance is a frequency domain method used to calculate the steady-state response of nonlinear differential equations (SHAIK ET AL., 2012). With the perturbation/modulation frequencies (f_m) much lower than the f_{sw}, the converter can be observed during steady-state operation. Substituting the equations from harmonic approximation (3.7) and EDF (3.9) into the nonlinear steady-state equations (3.1) and (3.3), and then equating the sine, cosine and DC coefficients, the harmonic balance is obtained, as defined by (3.11).

$$v_{es} = L_S\left(\frac{di_S}{dt} + \omega_S i_C\right) + r_S i_S + v_S + \frac{4n}{\pi}\frac{i_{PS}}{i_{PP}}v_{Co} = \frac{2V_{BUS}}{\pi}\sin\left(\frac{\pi d}{2}\right) \tag{3.11a}$$

$$v_{ec} = L_S\left(\frac{di_C}{dt} - \omega_S i_S\right) + r_S i_C + v_C + \frac{4n}{\pi}\frac{i_{PC}}{i_{PP}}v_{Co} = 0 \tag{3.11b}$$

$$i_S = C_S\left(\frac{dv_S}{dt} + \omega_S v_C\right) \tag{3.11c}$$

$$i_C = C_S\left(\frac{dv_C}{dt} - \omega_S v_S\right) \tag{3.11d}$$

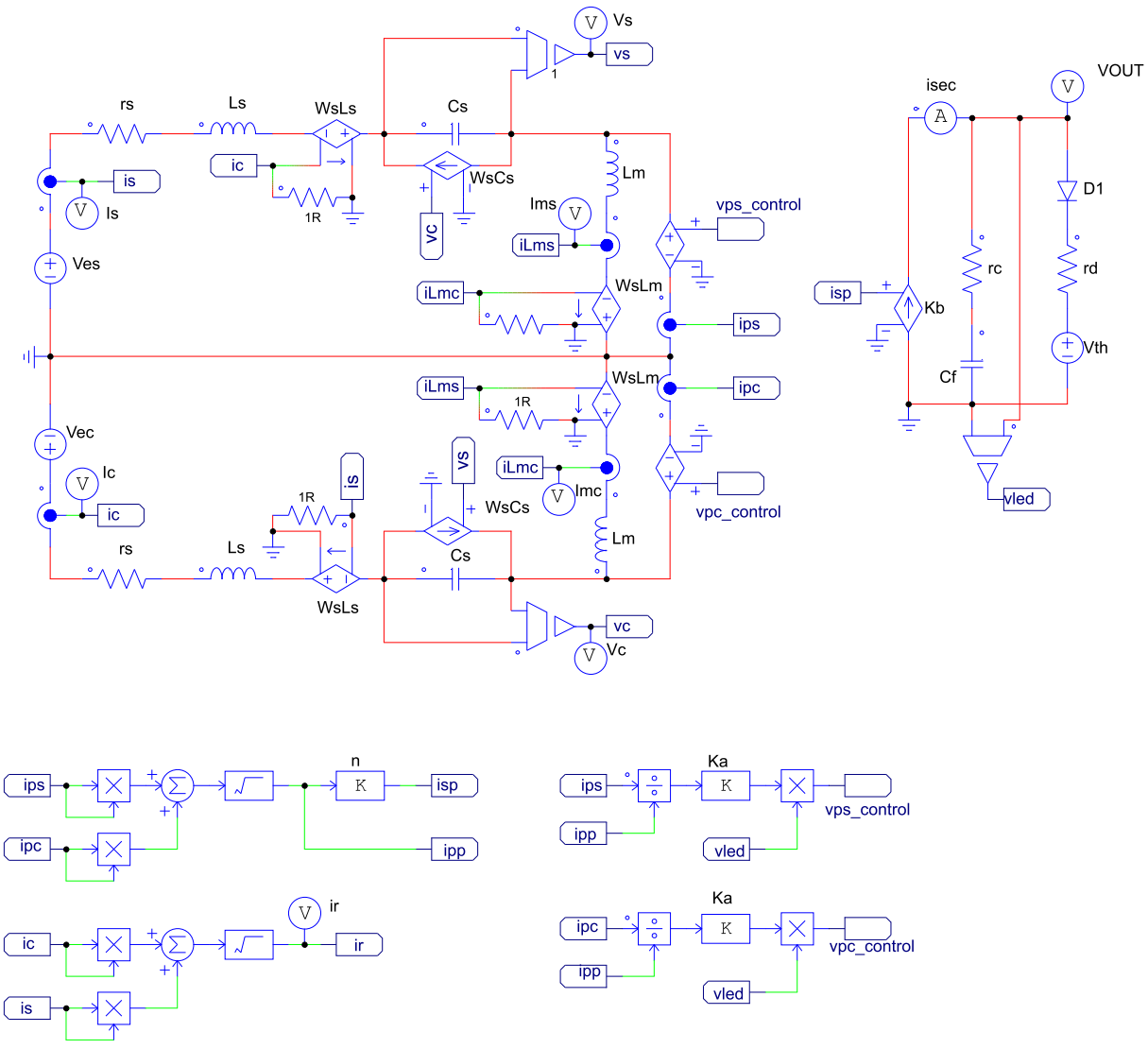
$$v_{PS} = L_M\left(\frac{di_{MS}}{dt} + \omega_S i_{MC}\right) = \frac{4n}{\pi}\frac{i_{PS}}{i_{PP}}v_{Co} \tag{3.11e}$$

$$v_{PC} = L_M\left(\frac{di_{MC}}{dt} - \omega_S i_{MS}\right) = \frac{4n}{\pi}\frac{i_{PC}}{i_{PP}}v_{Co} \tag{3.11f}$$

$$\frac{2}{\pi} i_{ST} = \frac{C_O dv_{Co}}{dt}\left(1+\frac{r_C}{r_{ac}}\right)+\frac{v_{Co}}{r_{ac}}-\frac{V_{th}}{r_{ac}} \tag{3.11g}$$

Equations in (3.11) describe the approximated large-signal model (LSM) of the LLC resonant LED driver. Fig. 31 illustrate the LSM implemented with PSIM, allowing one to assess the envelope terms behavior under steady-state operation. Because of the product of time-varying parameters, the approximated LSM remains with some non-linear terms (DEGIOANNI ET AL., 2018). Nevertheless, the system can be linearized around a steady-state operating point.

Figure 31 – Large-signal model of the LLC resonant LED driver realized with PSIM.



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3.2.5 Steady-state solution

The steady-state operating point of any converter must be known before determining its small-signal response (VORPÉRIAN ET AL., 1983), since the dynamic behavior is a function of the steady-state. The steady-state solution provides the results of DC analysis. In this way, under steady-state condition the LLC resonant LED driver new state variables – envelope terms: i_S, i_C, v_S, v_C, i_{MS}, i_{MC}, v_{Co} – are not changing with time, then their derivatives in (3.11) should be zero. Thus, the steady-state solution can be obtained for a given operating point with V_{BUS}, Ω_S (steady-state angular switching frequency), D, and V_{th}. Uppercase letters are used to denote the steady-state value.

Substituting (3.10) into (3.11.g) and considering the derivative equal to zero yields in (3.12.a), whose equation computes the average output voltage. With a similar procedure, one can obtain (3.12.b), which defines the average LED current (I_{LED}) in steady-state.

$$V_{Co} = V_{LED} = (2nI_{PP}r_{ac}/\pi) + V_{th} \tag{3.12a}$$

$$I_{LED} = \frac{2nI_{PP}r_C}{\pi(r_{ac}+r_C)} + \frac{V_{Co}}{r_{ac}+r_C} - \frac{V_{th}}{r_{ac}+r_C} \tag{3.12b}$$

Substituting (3.10) and (3.12) into (3.11) and doing all derivative equal to zero, the set of equations given in (3.13) is obtained. Analyzing (3.13), it can be seen as a non-linear system of equations, which has to be solved to obtain the steady-state values of the envelope terms I_S, I_C, V_S, V_C, I_{MS}, I_{MC} and output variables of interest I_{LED} and V_{LED}.

$$(r_S+R_{ac})I_S + L_S\Omega_S I_C + V_S - R_{ac}I_{MS} + \frac{4nV_{th}(I_S-I_{MS})}{\pi\sqrt{(I_S-I_{MS})^2+(I_C-I_{MC})^2}} = V_{es} \tag{3.13a}$$

$$-L_S\Omega_S I_S + (r_S+R_{ac})I_C + V_C - R_{ac}I_{MC} + \frac{4nV_{th}(I_C-I_{MC})}{\pi\sqrt{(I_S-I_{MS})^2+(I_C-I_{MC})^2}} = V_{ec} \tag{3.13b}$$

$$I_S - C_S\Omega_S V_C = 0 \tag{3.13c}$$

$$I_C + C_S\Omega_S V_S = 0 \tag{3.13d}$$

$$-R_{eq}I_S + L_M\Omega_S I_{MC} + R_{ac}I_{MS} - \frac{4nV_{th}(I_S-I_{MS})}{\pi\sqrt{(I_S-I_{MS})^2+(I_C-I_{MC})^2}} = 0 \tag{3.13e}$$

$$-R_{eq}I_C - L_M\Omega_S I_{MS} + R_{ac}I_{MC} - \frac{4nV_{th}(I_C-I_{MC})}{\pi\sqrt{(I_S-I_{MS})^2+(I_C-I_{MC})^2}} = 0 \tag{3.13f}$$

where:

$$R_{ac} = \frac{8n^2 r_{ac}}{\pi^2} \tag{3.14a}$$

$$I_{PS} = I_S - I_{MS} \tag{3.14b}$$

$$I_{PC} = I_C - I_{MC} \tag{3.14c}$$

$$I_{PP} = \sqrt{(I_S - I_{MS})^2 + (I_C - I_{MC})^2} \tag{3.14d}$$

3.2.6 Perturbation and Linearization of the harmonic balance equations

In this section, the large-signal model is perturbed around the determined steady-state operation point, and then with the small-signal assumption, the linearization is developed. In this way, it is assumed that the state-space variables, input and output signals are given by a small-signal AC variation (signal with "^") summed to a DC component (upper case), as shown in (3.15). For sake of completeness, input signals are v_{BUS}, v_{th}, d, and ω_S, and output signal correspond to i_{LED}.

$$i_S = I_S + \hat{i}_S \tag{3.15a}$$

$$i_C = I_C + \hat{i}_C \tag{3.15b}$$

$$v_{PS} = V_{PS} + \hat{v}_{PS} \tag{3.15c}$$

$$v_{PC} = V_{PC} + \hat{v}_{PC} \tag{3.15d}$$

$$v_S = V_S + \hat{v}_S \tag{3.15e}$$

$$v_C = V_C + \hat{v}_C \tag{3.15f}$$

$$i_{MS} = I_{MS} + \hat{i}_{MS} \tag{3.15g}$$

$$i_{MC} = I_{MC} + \hat{i}_{MC} \tag{3.15h}$$

$$v_{BUS} = V_{BUS} + \hat{v}_{BUS} \tag{3.15i}$$

$$v_{Co} = V_{Co} + \hat{v}_{Co} \tag{3.15j}$$

$$v_{th} = V_{th} + \hat{v}_{th} \tag{3.15k}$$

$$d = D + \hat{d} \tag{3.15l}$$

$$i_{LED} = I_{LED} + \hat{i}_{LED} \tag{3.15m}$$

$$\omega_S = \Omega_S + \frac{\omega_0 \hat{\omega}}{\omega_0} = \Omega_S + \omega_0 \hat{\omega}_{SN} \tag{3.15n}$$

Substituting (3.15) into the non-linear large-signal model (3.11), and by making linearization[2] under the small-signal assumption, the state variables small-signal differential equations are obtained, given in (3.16).

$$\frac{d\hat{i}_S}{dt} = -\frac{H_{ips}+r_S}{L_S}\hat{i}_S - \frac{H_{ipc}+\Omega_S L_S}{L_S}\hat{i}_C - \frac{1}{L_S}\hat{v}_S + \frac{H_{ips}}{L_S}\hat{i}_{MS} + \frac{H_{ipc}}{L_S}\hat{i}_{MC} - \frac{H_{vco}}{L_S}\hat{v}_{Co} + \frac{K_1}{L_S}\hat{v}_{BUS} + \frac{K_2}{L_S}\hat{d} - \omega_O I_C \hat{\omega}_{SN} \tag{3.16a}$$

$$\frac{d\hat{i}_C}{dt} = \frac{L_S\Omega_S - G_{ips}}{L_S}\hat{i}_S - \frac{G_{ipc}+r_S}{L_S}\hat{i}_C - \frac{1}{L_S}\hat{v}_C + \frac{G_{ips}}{L_S}\hat{i}_{MS} + \frac{G_{ipc}}{L_S}\hat{i}_{MC} - \frac{G_{vco}}{L_S}\hat{v}_{Co} + \omega_O I_S \hat{\omega}_{SN} \tag{3.16b}$$

$$\frac{d\hat{v}_S}{dt} = \frac{1}{C_S}\hat{i}_S - \Omega_S \hat{v}_C - V_C \omega_0 \hat{\omega}_{SN} \tag{3.16c}$$

$$\frac{d\hat{v}_C}{dt} = \frac{1}{C_S}\hat{i}_C + \Omega_S \hat{v}_S + V_S \omega_0 \hat{\omega}_{SN} \tag{3.16d}$$

$$\frac{d\hat{i}_{MS}}{dt} = \frac{H_{ips}}{L_M}\hat{i}_S + \frac{H_{ipc}}{L_M}\hat{i}_C - \frac{H_{ips}}{L_M}\hat{i}_{MS} - \left(\frac{H_{ipc}+L_M\Omega_S}{L_M}\right)\hat{i}_{MC} + \frac{H_{vco}}{L_M}\hat{v}_{Co} - \omega_0 I_{MC}\hat{\omega}_{SN} \tag{3.16e}$$

$$\frac{d\hat{i}_{MC}}{dt} = \frac{G_{ips}}{L_M}\hat{i}_S + \frac{G_{ipc}}{L_M}\hat{i}_C - \left(\frac{G_{ips}-L_M\Omega_S}{L_M}\right)\hat{i}_{MS} - \frac{G_{ipc}}{L_M}\hat{i}_{MC} + \frac{G_{vco}}{L_M}\hat{v}_{Co} + \omega_0 I_{MS}\hat{\omega}_{SN} \tag{3.16f}$$

$$\frac{d\hat{v}_{Co}}{dt} = \frac{K_{ips}r_{ac}}{C_o(r_{ac}+r_C)}\hat{i}_S + \frac{K_{ipc}r_{ac}}{C_o(r_{ac}+r_C)}\hat{i}_C - \frac{K_{ips}r_{ac}}{C_o(r_{ac}+r_C)}\hat{i}_{MS} - \frac{K_{ipc}r_{ac}}{C_o(r_{ac}+r_C)}\hat{i}_{MC} - \frac{1}{C_o(r_{ac}+r_C)}\hat{v}_{Co} + \frac{1}{C_o(r_{ac}+r_C)}\hat{v}_{th} \tag{3.16g}$$

In the same way, for the output equation given in (3.5), applying (3.15) outcomes in (3.17). Equation (3.18) presents the parameters employed in (3.16) and (3.17).

$$\hat{i}_{LED} = \frac{K_{ips}r_C^*}{r_{ac}}\hat{i}_S + \frac{K_{ipc}r_C^*}{r_{ac}}\hat{i}_C - \frac{K_{ips}r_C^*}{r_{ac}}\hat{i}_{MS} - \frac{K_{ipc}r_C^*}{r_{ac}}\hat{i}_{MC} + \frac{1}{r_{ac}+r_C}\hat{v}_{Co} - \frac{1}{r_{ac}+r_C}\hat{v}_{th} \tag{3.17}$$

$$H_{ips} = \frac{4nV_{Co}}{\pi}\frac{(I_{PC})^2}{(I_{PP})^3} \tag{3.18a}$$

[2]Second order and DC terms are removed

$$H_{ipc} = -\frac{4nV_{Co}}{\pi}\frac{I_{PS}I_{PC}}{(I_{PP})^3} \tag{3.18b}$$

$$H_{vco} = \frac{4n}{\pi}\frac{I_{PS}}{I_{PP}} \tag{3.18c}$$

$$G_{ips} = -\frac{4nV_{Co}}{\pi}\frac{I_{PC}I_{PS}}{(I_{PP})^3} \tag{3.18d}$$

$$G_{ipc} = \frac{4nV_{Co}}{\pi}\frac{(I_{PS})^2}{(I_{PP})^3} \tag{3.18e}$$

$$G_{vco} = \frac{4n}{\pi}\frac{I_{PC}}{I_{PP}} \tag{3.18f}$$

$$K_1 = \frac{2}{\pi}\sin\left(\frac{\pi D}{2}\right) \tag{3.18g}$$

$$K_2 = V_{BUS}\cos\left(\frac{\pi D}{2}\right) \tag{3.18h}$$

$$K_{ips} = \frac{2n}{\pi}\frac{I_{PS}}{\sqrt{(I_{PS})^2 + (I_{PC})^2}} \tag{3.18i}$$

$$K_{ipc} = \frac{2n}{\pi}\frac{I_{PC}}{\sqrt{(I_{PS})^2 + (I_{PC})^2}} \tag{3.18j}$$

At this point, analyzing (3.18), it is clear to see that the small-signal behavior depends on the converter parameters, steady-state operating point, and input signals.

Finally, two distinguish procedures can be employed to obtain the frequency response of the control-to-output TF. Analyzing (3.16) and (3.17), the corresponding equivalent circuit of the small-signal model can be developed and then employed under ac-sweep simulations to extracted the TF of interest. On the other hand, as presented in the next section, the system can be analyzed using state-space representation. Then employing Laplace Transformation, the TF of interest could be defined.

3.2.7 Small-signal model state-space representation

The state-space representation for a linear time-invariant (LTI) system is given by (3.19). Wherein $\mathbf{x}(t)$ is the state-vector, $\mathbf{u}(t)$ is the input of the system and **A**, **B**, **C** and **D** are constant matrices.

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \tag{3.19a}$$

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t) \tag{3.19b}$$

Analyzing the last section that deals with the perturbation and linearization of the harmonic balance equations, it can be seen that an LTI system is obtained for the small-signal behavior model of the LLC resonant LED driver. Thus, the SSM can be presented in state-space representation. However, in the small-signal assumption, the state-vector, input signal, and output signals receive " ˆ". Hence, the LLC resonant LED driver small-signal model can be represented in a state-space representation, as shown in (3.20).

$$\hat{\dot{\mathbf{x}}} = \mathbf{A}\hat{\mathbf{x}}(\mathbf{t}) + \mathbf{B}\hat{\mathbf{u}}(\mathbf{t}) \tag{3.20a}$$

$$\hat{\mathbf{y}}(t) = \mathbf{C}\hat{\mathbf{x}}(t) + \mathbf{E}\hat{\mathbf{u}}(t) \tag{3.20b}$$

Considering the developed LLC resonant LED driver SSM, the state-vector is given by (3.21).

$$\hat{\mathbf{x}} = \begin{bmatrix} \hat{i}_S & \hat{i}_C & \hat{v}_S & \hat{v}_C & \hat{i}_{ms} & \hat{i}_{mc} & \hat{v}_{Co} \end{bmatrix} \tag{3.21}$$

The output signal is given by (3.22).

$$\hat{y} = i_{LED} \tag{3.22}$$

On the other hand, the input signals are defined by (3.23).

$$\hat{\mathbf{u}} = \begin{bmatrix} \hat{v}_{BUS} & \hat{v}_{th} & \hat{d} & \hat{\omega}_{SN} \end{bmatrix} \tag{3.23}$$

Finally, the constant matrices **A**, **B**, **C**, and **E** are respectively given in (3.24), (3.25), (3.26) and (3.27).

$$\mathbf{A} = \begin{bmatrix} -\frac{H_{ips}+r_S}{L_S} & -\frac{H_{ipc}+\Omega_S L_S}{L_S} & -\frac{1}{L_S} & 0 & \frac{H_{ips}}{L_S} & \frac{H_{ipc}}{L_S} & -\frac{H_{vco}}{L_S} \\ \frac{\Omega_s L_s - G_{ips}}{L_S} & -\frac{G_{ipc}+r_s}{L_S} & 0 & -\frac{1}{L_S} & \frac{G_{ips}}{L_S} & \frac{G_{ipc}}{L_S} & -\frac{G_{vco}}{L_S} \\ 1/C_S & 0 & 0 & -\Omega_S & 0 & 0 & 0 \\ 0 & 1/C_S & \Omega_S & 0 & 0 & 0 & 0 \\ \frac{H_{ips}}{L_M} & \frac{H_{ipc}}{L_M} & 0 & 0 & -\frac{H_{ips}}{L_M} & -\frac{H_{ipc}+L_M\Omega_S}{L_M} & \frac{H_{vco}}{L_M} \\ \frac{G_{ips}}{L_M} & \frac{G_{ipc}}{L_M} & 0 & 0 & -\frac{G_{ips}-L_M\Omega_S}{L_M} & -\frac{G_{ipc}}{L_M} & \frac{G_{vco}}{L_M} \\ \frac{K_{ips}r_{ac}}{C_O(r_{ac}+r_C)} & \frac{K_{ipc}r_{ac}}{C_O(r_{ac}+r_C)} & 0 & 0 & -\frac{K_{ips}r_d}{C_O(r_{ac}+r_C)} & -\frac{K_{ipc}r_{ac}}{C_O(r_{ac}+r_C)} & -\frac{1}{C_O(r_{ac}+r_C)} \end{bmatrix} \tag{3.24}$$

$$\mathbf{B} = \begin{bmatrix} \frac{K_1}{L_S} & 0 & \frac{K_2}{L_S} & -\omega_0 I_C \\ 0 & 0 & 0 & \omega_0 I_S \\ 0 & 0 & 0 & -\omega_0 V_C \\ 0 & 0 & 0 & \omega_0 V_S \\ 0 & 0 & 0 & -\omega_0 I_{MC} \\ 0 & 0 & 0 & \omega_0 I_{MS} \\ 0 & \frac{1}{C_O(r_{ac}+r_C)} & 0 & 0 \end{bmatrix} \tag{3.25}$$

$$\mathbf{C} = \begin{bmatrix} K_{ips}r_C^*/r_{ac} & K_{ipc}r_C^*/r_{ac} & 0 & 0 & -K_{ips}r_C^*/r_{ac} & -K_{ipc}r_C^*/r_{ac} & 1/(r_{ac}+r_C) \end{bmatrix} \tag{3.26}$$

$$\mathbf{E} = \begin{bmatrix} 0 & -\frac{1}{r_{ac}+r_C} & 0 & 0 \end{bmatrix} \tag{3.27}$$

It is worthy of mentioning that the eigenvalues of matrix **A** represent the poles of the linearized SSM for LLC resonant LED driver operating around the considered steady-state condition. Thus, their position in the complex plane could be assessed to investigate the dynamic behavior of the system. Besides, from a different perspective, matrices **A** and **B** are the Jacobian matrices of the system.

Alternatively, the dynamic behavior can be analyzed by the frequency response of the TF of interest. With the SSM in state-space representation, the TF of the LLC converter output

(i_{LED}) related to their different inputs ($\hat{\mathbf{u}}_\mathbf{i}$) can be obtained solving (3.28).

$$G_P(s) = \frac{\hat{i}_{LED}}{\hat{\mathbf{u}}_\mathbf{i}} = \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} + \mathbf{E} \tag{3.28}$$

Owing to the system's different input signals, to extract, for instance, the control-to-output TF for a pulse-frequency modulated LLC converter ($G_p(s) = \hat{i}_o/\hat{\omega}_{SN}$), the fourth input signal has to be selected. In this case, the MATLAB command `ss2tf(A,B,C,E,4)` could be employed. This command gives the TF that relates the system output ($\hat{i}_{LED}$) with the fourth input signal ($\hat{\omega}_{SN}$).

3.3 SIMULATION RESULTS

Focusing on the frequency response, several analyses are developed in this section to verify the accuracy of the presented small-signal modeling procedure. Initially, employing simulation results, the model accuracy is evaluated for the LLC resonant LED driver operating at main resonance f_o. In the sequence, a comparison between the employment of LED equivalent resistance and the LED PWL model is carried out to evaluate the condition where both models converge to the same dynamic behavior. Finally, the model accuracy under a wide operating range is assessed.

The LLC resonant converter parameters employed in this section are given in Table 3. The converter design follows the classical design procedure presented in Appendix A. The employed LED module is given by three BXRC-50C400 COB LED connected in series

Table 3 – LLC resonant LED driver parameters

Parameter	**Designator**	**Value**
LLC LED driver design specification		
Nominal DC input voltage	V_{BUS}	400 V
Minimal DC input	$V_{BUS.MIN}$	360 V
Maximum DC input voltage	$V_{BUS.MAX}$	420 V
LLC converter resonant frequency	f_o	100 kHz
Maximum LLC converter output power	P_O	100 W
Minimum LLC converter output power	$P_{O.MIN}$	≈15 W
Designed LLC LED driver resonant converter		
Average LED current range	I_{LED}	$0.2 - 1.15\ A$
Average LED voltage	V_{LED}	$80.4 - 87.3\ V$
Resonant capacitor	C_S	12 nF
Resonant inductor	L_S	211 μH
Magnetizing inductance	L_M	633 μH
Output capacitor (Film capacitor)	C_O	10 μF/100V
Transformer turns ratio (n)	N_P/N_S	2.29
Half-bridge switching frequency	f_{sw}	86.9–131.1 kHz

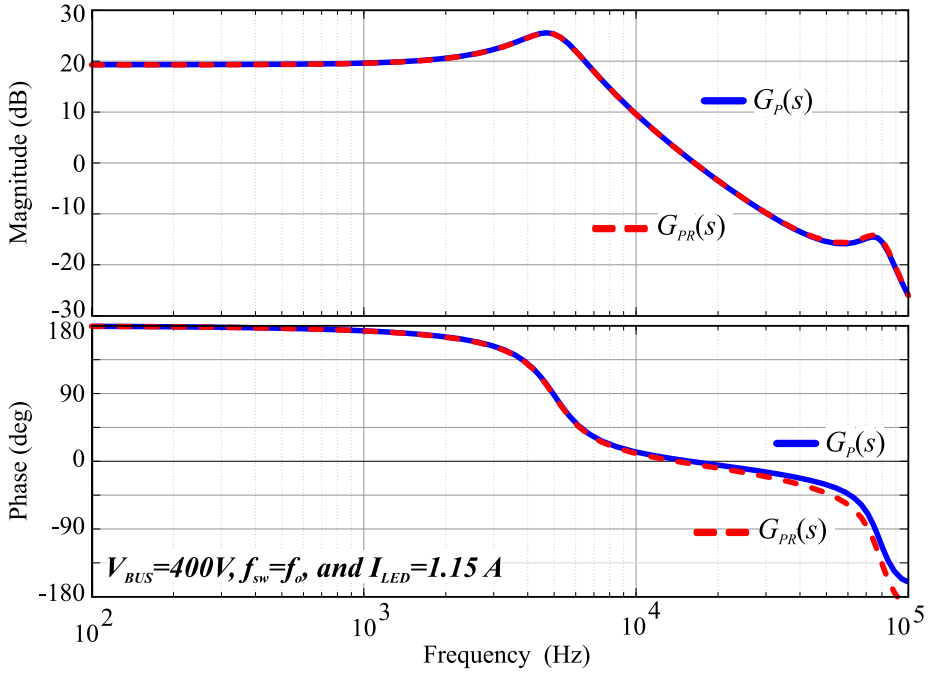
(BRIDGELUX, 2014), whose electrical behavior was described in section 2.1.

At this point, considering the parameters given in Table 3, and being $r_C = 50\ m\Omega$ and $r_S = 0.1\ \Omega$, the control-to-output TF for a pulse-frequency modulated LLC converter ($G_p(s) = \hat{i}_o/\hat{\omega}_{SN}$) operating at nominal conditions ($f_{sw} = f_o$) is computed employing the described modeling procedure. The obtained TF is a seventh order system, given by (3.29). Neglecting zeros and poles away from f_{sw}, except the RHP zero, outcomes in a fourth-order system given by (3.30). Fig. 32 shows the Bode diagram of both full 7^{th} and reduced 4^{th} order responses. As can be seen, the reduced-order presents satisfactory accuracy and could be used without loose of generality. The script developed in MATLAB to compute and plot the LLC resonant LED driver dynamic behavior can be accessed in the supplementary material of this thesis, which is described in Appendix G.

$$G_P(s) = \frac{3.6551\cdot 10^6(s+1.503\cdot 10^9)(s+2\cdot 10^6)}{(s+1.709\cdot 10^6)(s^2+1.594\cdot 10^4 s+9.968\cdot 10^8)} \cdot \frac{(s-5.633\cdot 10^5)(s^2+5.638\cdot 10^5 s+7.129\cdot 10^{11})}{(s^2+1.35\cdot 10^5 s+2.455\cdot 10^{11})(s^2+1.943\cdot 10^5 s+1.142\cdot 10^{12})} \tag{3.29}$$

$$G_{PR}(s) = \frac{4.0124\cdot 10^{15}(s-5.633\cdot 10^5)}{(s^2+1.594\cdot 10^4 s+9.968\cdot 10^8)(s^2+1.353\cdot 10^5 s+2.455\cdot 10^{11})} \tag{3.30}$$

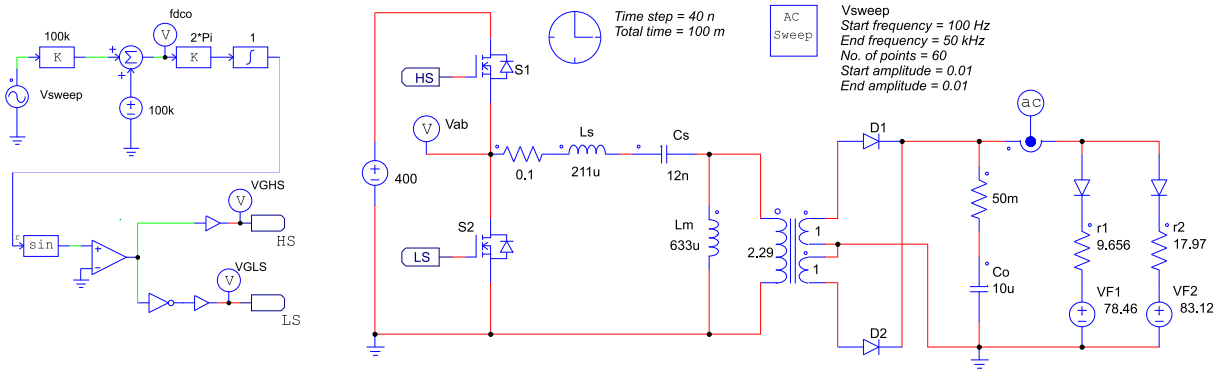
Figure 32 – Bode Diagram of the LLC resonant LED driver small-signal model, comparing full order and reduced order approaches.



Source: Author.

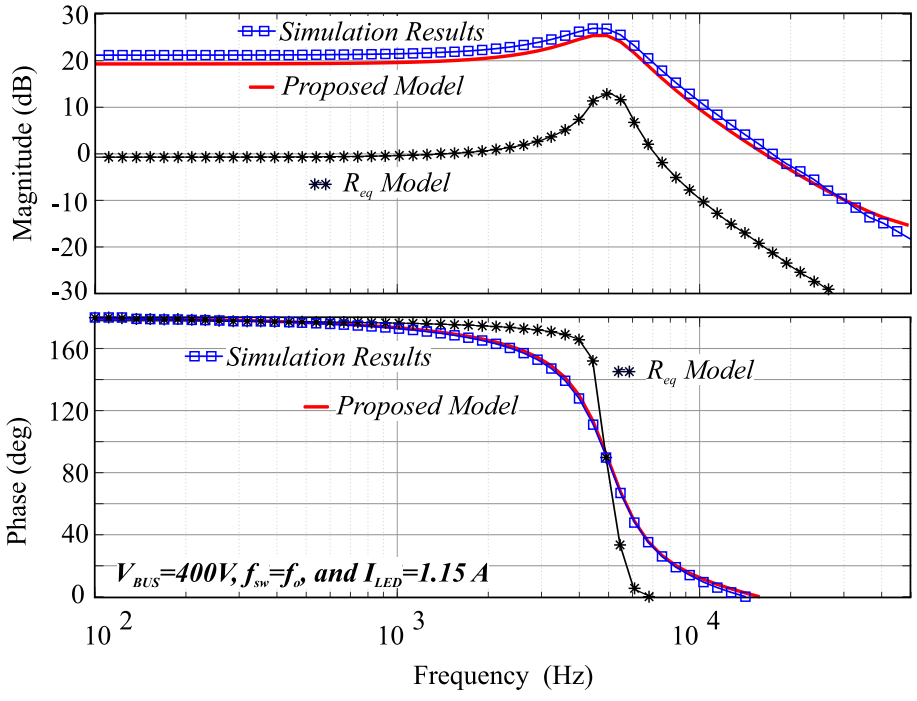
To evaluate the accuracy of the proposed modeling procedure, it is assumed that Powersim (PSIM) simulation results provide the real converter dynamic behavior. Employing ideal elements, Fig. 33 shows the LLC schematic developed in PSIM to obtain the converter frequency-response under ac-sweep simulations. Finally, Fig. 34 shows the frequency response for LLC resonant LED converter, where simulations results are compared with results obtained from the proposed model; besides, the results for the case where R_{eq} approximates the LED electrical behavior are also presented. As can be seen, the proposed model response described

Figure 33 – PSIM schematic circuit for ac-sweep simulation with the purpose of obtained the control-to-output frequency response of the LLC LED driver.



Source: Author.

Figure 34 – Frequency response of the LLC LED driver for different approaches: Simulation results, proposed model response, and behavior when LED is approximated by its R_{eq}



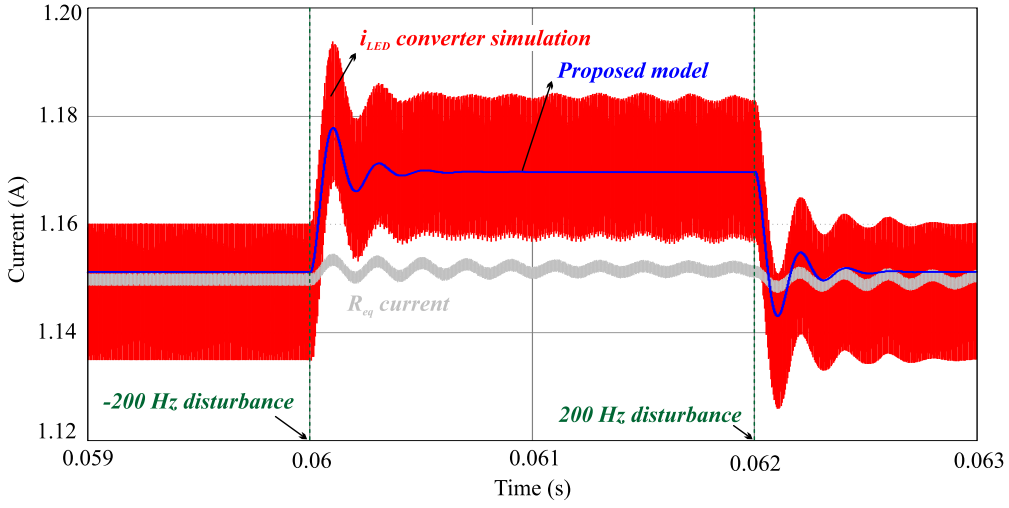
Source: Author

satisfactorily the converter dynamic behavior. On the other hand, when LED is model by its R_{eq} the obtained frequency response strongly deviates from the real one, here assumed as the simulation results.

Fig. 35 shows the LED current time response when the system is submitted to f_{sw} step-down and step-up transients, applied simultaneously to the three following approaches: 1) LLC resonant LED driver circuit, which provides the reference dynamic behavior of the converter (i_{LED} *converter simulation*); 2) TF given by (3.29), which is the outcome of the proposed model; and 3) LLC converter employing the LED equivalent resistance R_{eq}, which is the usually employed approach. As can be seen, the proposed small-signal model faithfully emulates the dynamic behavior of LLC resonant LED driver converter. This means that the proposed small-signal modeling procedure, which employs the EDF method and considers the LEDs PWL circuit model instead of its R_{eq}, outcomes in an enhanced modeling approach for LLC resonant LED driver, achieving the primary goal of this chapter.

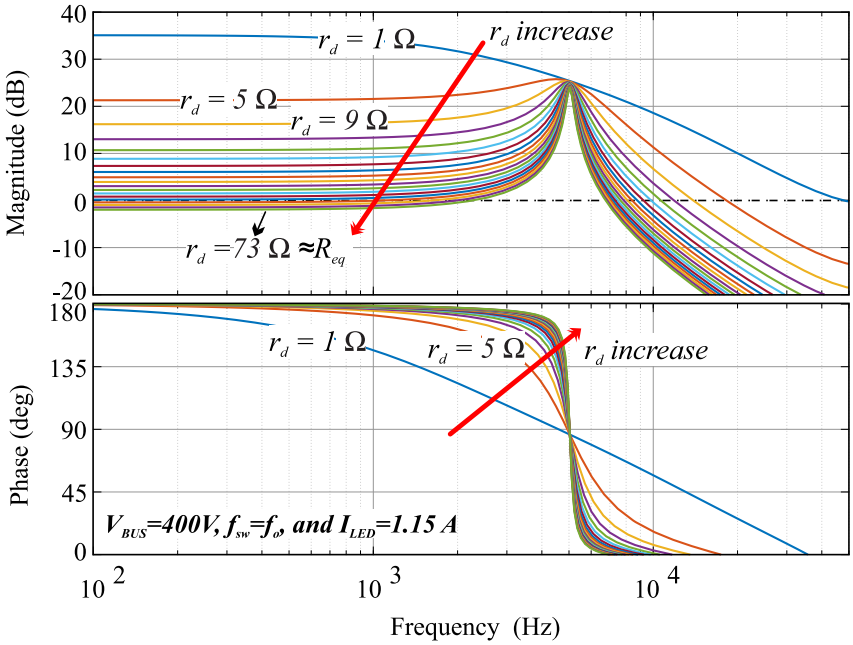
Based on the above presented results, it can be noticed that the dynamic model of the LLC resonant LED driver is improved when the LED non-linearity is taken into account throughout the modeling procedure. However, in order to evaluate the condition where the R_{eq} approach does not reflect the real dynamic behavior of the converter, Fig. 36 shows the frequency response for the designed LLC resonant LED driver supplying different LED modules. These modules are given by a different combination of r_d and V_{th}, where r_d is changed to a specific value (1 Ω, 5 Ω, 9 Ω, etc) and V_{th} is calculated in order to obtain 100 W for the nominal V_{LED} and I_{LED} (see Table 3). As it can be seen in Fig. 36, as function as r_{ac} becomes closer to the R_{eq} value, smaller is the difference between the Bode Diagram considering the LED non-linearity and the Bode Diagram for R_{eq}. Thus, it can be stated that the more significant the difference between r_d and R_{eq}, the more significant will be the error

Figure 35 – LLC converter output current dynamic response comparison among the converter simulation, proposed model which consider the LED PWL model, and usual approach that employs R_{eq}.



Source: Author

Figure 36 – Analysis of the frequency response of the designed LLC LED driver supplying a 100 W LED module as a function of r_{ac} and V_{th}.



Source: Author

related to the small-signal model if the R_{eq} approach is used. Consequently, considering the TF obtained from the R_{eq} approach, the feedback controller designed to achieve, for instance, active ripple compensation, will not behave as expected, leading the system to instability, or with a compromised performance. In this way, considering the designed LLC resonant LED driver supplying and COB LED module with r_d more than ten times smaller than R_{eq}, the use of the proposed small-signal modeling procedure is mandatory. As a general rule, if r_d is smaller than half of the R_{eq} value, the approach where the LED non-linearity is neglected becomes unreliable and has to be avoided.

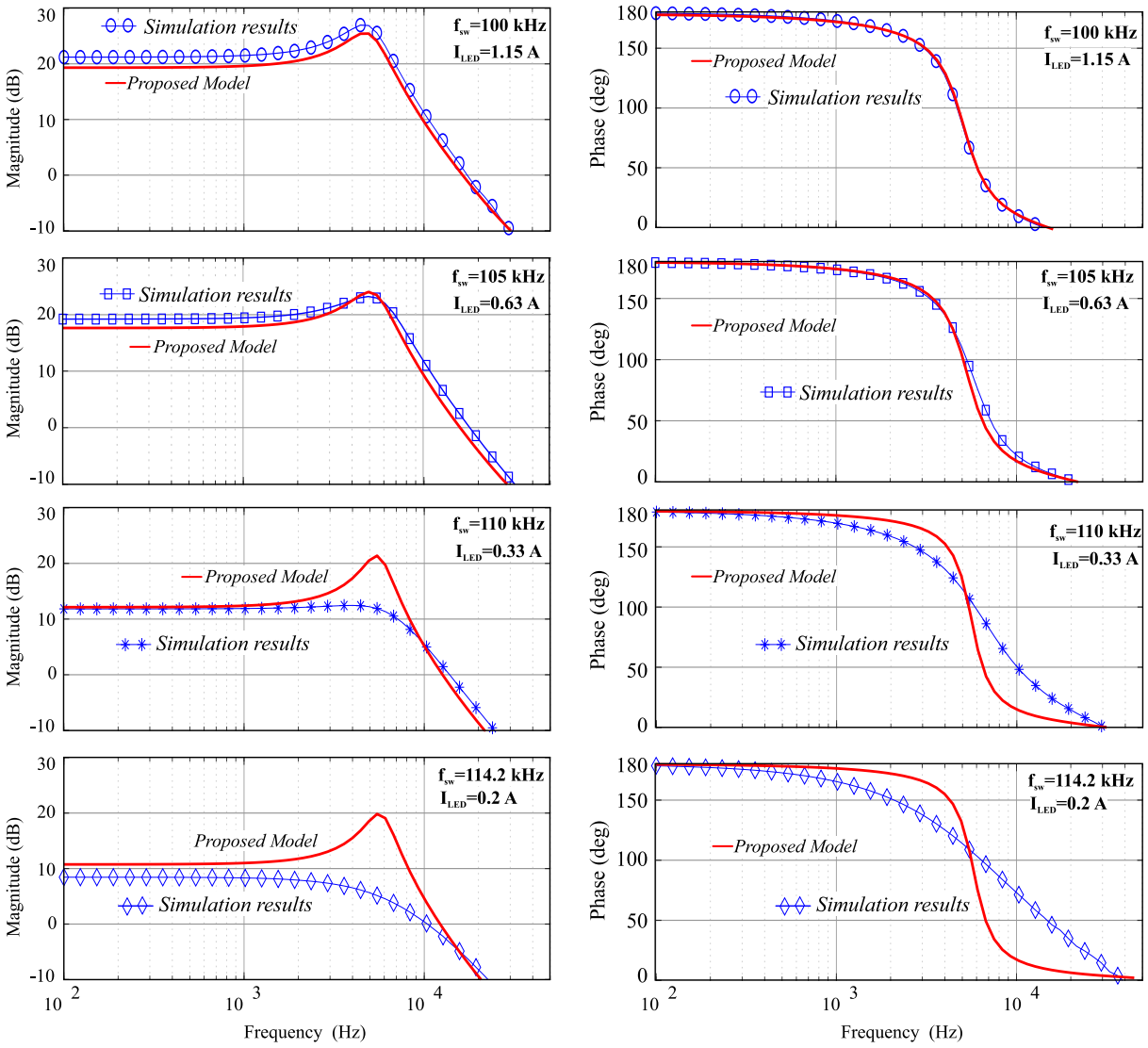
It is worthy of highlighting that the analysis presented above considered the LLC resonant LED driver operating at the main resonance f_o. However, to maintain output regulated under parametric variation or perform dimming by changing the LED average value reference, the LLC resonant LED driver f_{sw} is modulated. So, one should question what happens with the modeling accuracy when the converter operates beyond f_o. Therefore, to evaluate the modeling procedure in this perspective, further analyses are presented in the next section.

3.3.1 LLC resonant LED driver operation beyond f_o

To assess the modeling accuracy when f_{sw} deviates from f_o, Fig. 37 shows the frequency response of the LLC resonant LED driver in comparison to the response predicted

by the proposed model. As can be seen, in the way that f_{sw} becomes higher than f_o, the greater is the difference between the converter's dynamic behavior obtained by simulation and the behavior predicted by the proposed model. Further assessing the dynamic behavior of the LLC resonant LED driver, Fig. 38 shows the simulated LED current response during step-up and step-down transients in f_{sw}. In addition, the dynamic behavior predicted with the proposed model is also shown in Fig. 38, where an offset adjustment is developed to attenuate the error between model and converter behavior. As can be seen, for $f_{sw} = 105\ kHz$, the proposed model deviates from the converter dynamic in a dc value only, so with a simple gain adjustment, the proposed model could be adapted for this case. On the other hand, for $f_{sw} = 110\ kHz$ and $f_{sw} = 114.2\ kHz$ a dc adjustment is not enough to enhance the model

Figure 37 – Comparison of the frequency response between proposed model and LLC resonant LED driver when f_{sw} deviates from f_o.

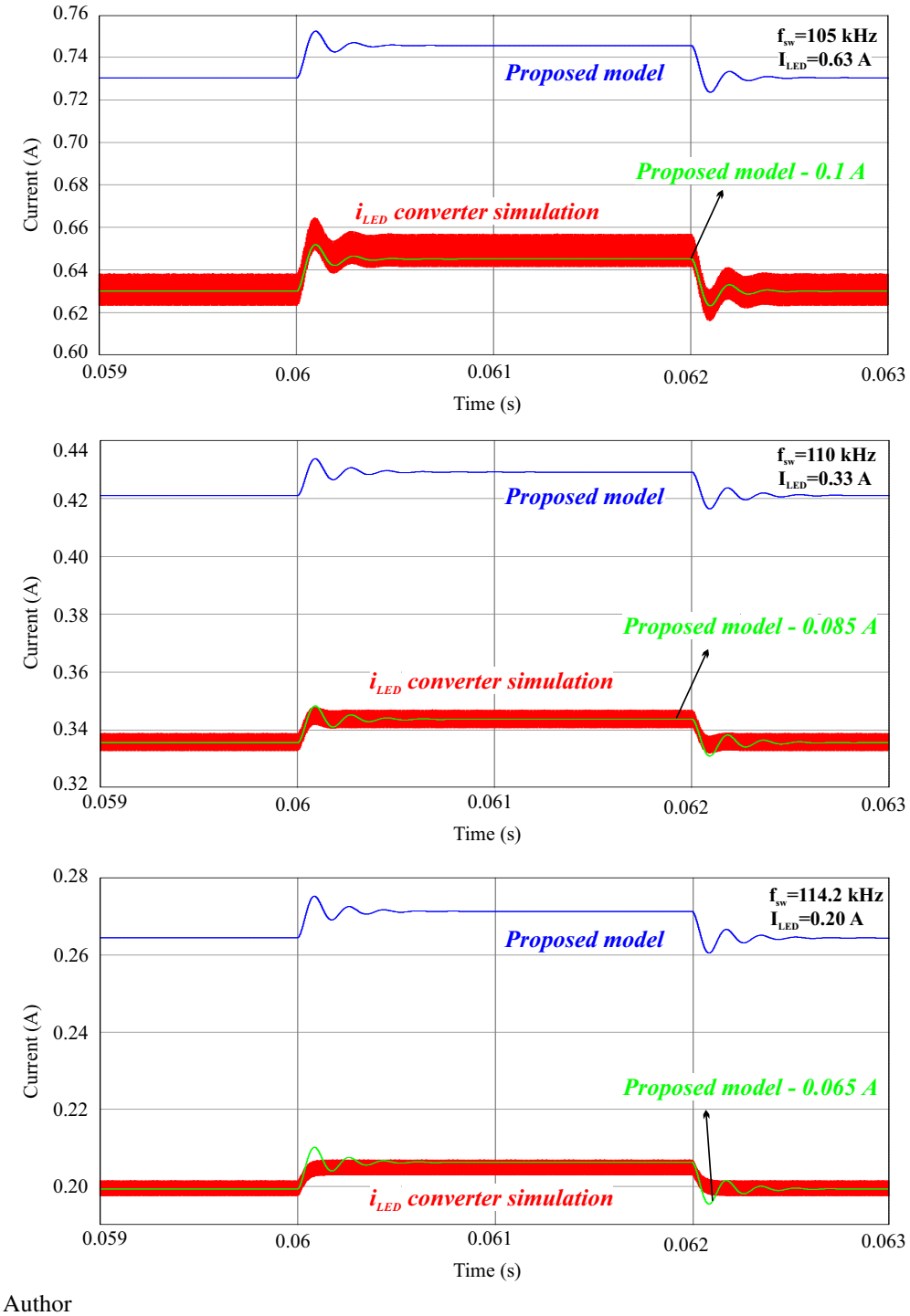


Source: Author

accuracy since the transient behavior differs considerably. Nevertheless, this error was expected to occur since the FHA is employed throughout the EDF modeling procedure.

Based on the above discussion, it can be concluded that the proposed modeling procedure is suitable for the LLC resonant LED driver operation only around f_o. For the operation beyond f_o, the predicted dynamic behavior deviates from the converter response.

Figure 38 – LED current time response comparison among the converter simulation and proposed model when operating f_{sw} deviates from f_o.



Source: Author

3.4 SUMMARY

In this chapter, the LLC resonant LED driver small-signal modeling procedure has been presented. In comparison to the usually employed approach for the LLC resonant LED driver small-signal model, which considers the LED as a single equivalent resistance R_{eq}, the novelty of the proposed model is the consideration of the nonlinear electrical behavior of the LED.

Experimental results showed the feasibility of the proposed model, which predicts the dynamic behavior of the LLC resonant LED driver when it operates around the main resonance. Further analysis demonstrated that the higher the difference between r_d and R_{eq}, the higher is the error in predicting the LLC resonant LED driver dynamic response employing the classical approach where LED is approximate by an R_{eq}.

On the other hand, as expected, the inherent limitations of the proposed modeling procedure also have been presented. Based on the analysis of converter operation beyond the main resonance, it is concluded that the proposed modeling procedure for the LLC resonant LED driver is valid when the operating point is near the main resonance. Otherwise, significant errors can be noticed.

4 LLC LED DRIVER TIME-DOMAIN ANALYSIS

This chapter presents the general time-domain (TD) solution for the LLC resonant LED driver converter, obtained from the state-space representation direct TD solution. Dissimilar to preceding TD analyses, all the converter states are considered, and no current and voltage waveforms sinusoidal or average value approximations are taken. Methodically, considering the variable structure behavior of the LLC converter, each operation mode of the LLC is solved in the TD. In addition, a new operation mode area mapping and mode solver algorithms are proposed. Finally, simulation and experimental results verify the enhanced accuracy of the proposed TD solution in predicting the converter performance regardless of the converter's parameters and operating point. In this way, it is possible to develop advanced analyses for the converter and develop new design procedures once the system's real behavior is predicted.[1]

4.1 INTRODUCTION

Analyzing the literature that deals with LLC converter steady-state TD analysis, several studies originated from the methodology proposed in (LAZAR ET AL., 2001). These studies (DENG ET AL., 2015; X. FANG, HU, Z. J. SHEN ET AL., 2012; Z. FANG, CAI ET AL., 2015; LAZAR ET AL., 2001; MUMTAHINA ET AL., 2018; SHAFIEI ET AL., 2017; SIMONE ET AL., 2006; H. WANG E BLAABJERG, 2014; R. YU ET AL., 2012), which follows the same backbone when considering the LLC TD solution, summarize the state-of-art technology, where details are discussed in Chapter 2.

Considering the approaches reported in the literature, even that accurate results are obtained in predicting the DC/DC LLC converter behavior in the TD, usually employed approximations do not allow a general and theoretically exact solution. These main approximations that simplify the analysis but avoids further insights of the converter are: (i) The converter output voltage is considered as a constant voltage source (V_O), which does not allow enhance the output filter design and evaluate the output voltage and current ripple, crucial in applications such as LED drivers and battery chargers; (ii) Voltage and current analysis in all the converter elements is avoided, being analyzed only a partial number of the system states variables; (iii) The operation of the LLC converter is given for a 50% duty-cycle

[1] Portions of this chapter have been published in (MENKE, DURANTI ET AL., 2020).

with pulse-frequency-modulation (PFM); (iv) All elements are considered ideal; and, (v) Load is treated as purely resistive.

In order to overcome several of these shortcomings, a new TD solution procedure for the LLC converter is proposed based on the system state-space representation direct TD solution. In this solution, all the state-variables of the converter are considered in the analysis; the output voltage is defined as the output filter capacitor voltage; and the LED load is examined as a PWL circuit. In this way, since a reduced number of assumptions are made, it can be stated that the state-space-based TD solution provides the most accurate results in comparison to previously reported studies, where state-space representation is avoided.

The employment of the state-space TD solution analysis in power electronics converters is usually set aside due to their complexity. Nevertheless, as it will be shown, employing the presented procedure, the complexity will be diminished, and all the effort will be redirected to numerical computational software. Although some designers try to avoid numerical computational software, there is no going back. The employment of optimized design and analysis tools is becoming a natural trend in the power electronics field. Additionally, a closed-form solution is obtained for the LLC converter in the continuous conduction mode (CCM) operation; however, it is not the case for the discontinuous conduction mode (DCM) since it involves nonlinear equations solving. In this way, to unify the analysis, the use of numerical approaches is more suitable.

4.2 FUNDAMENTALS OF THE EMPLOYED TD SOLUTION

A continuous time (CT) linear time-invariant (LTI) system representation in state-space equations is given by (4.1) (C. T. CHEN, 1995), (CHI TSONG CHEN, 2012).

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \tag{4.1a}$$

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t) \tag{4.1b}$$

where $\mathbf{x}(t)$ is the state-vector; $\mathbf{u}(t)$ is the input of the system; and $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$ and $\mathbf{D}$ are constant matrices.

In this sort of system representation, we are interested in find the solution for the state-vector $\mathbf{x}(t)$ and the output $\mathbf{y}(t)$ excited by an input $\mathbf{u}(t)$ and state-vector initial conditions $\mathbf{x}(t_0)$ for $t \geq 0$. This problem can be solved directly in the TD or indirectly by using the Laplace transform (C. T. CHEN, 1995). Following the analysis in (CHI TSONG CHEN, 2012), the direct TD solution of (4.1) due to $\mathbf{u}(t)$ and $\mathbf{x}(t_0)$, is given by (4.2).

$$\mathbf{x}(t) = e^{\mathbf{A}t}\mathbf{x}(0) + \int_0^t e^{\mathbf{A}(t-\tau)}\mathbf{B}\mathbf{u}(\tau)d\tau \tag{4.2a}$$

$$\mathbf{y}(t) = \mathbf{C}e^{\mathbf{A}t}\mathbf{x}(0) + \mathbf{C}\int_0^t e^{\mathbf{A}(t-\tau)}\mathbf{B}\mathbf{u}(\tau)d\tau + \mathbf{D}\mathbf{u}(t) \tag{4.2b}$$

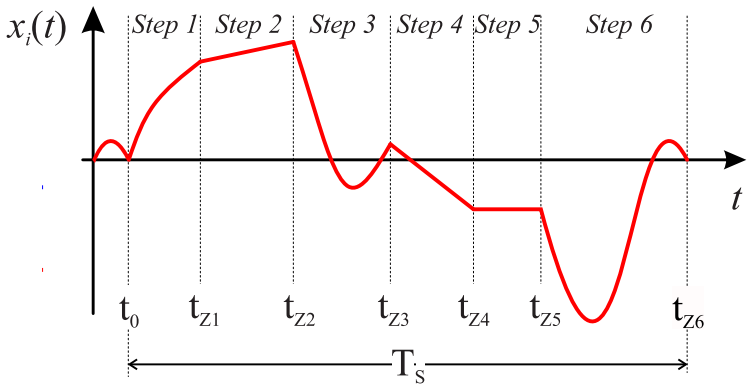
Equation (4.2) is the TD solution for a CT LTI system. However, considering any switched converter's, a different equivalent circuit is obtained for each controlled or uncontrolled switch state, which characterizes a nonlinear system over a switching cycle. On the other hand, each equivalent circuit of the system as a function of the switches state can be analyzed by a CT LTI system. Thus, the converter operation over a switching cycle can be modeled as a variable structure system, also named a piece-wise linear (PWL) system. Nevertheless, the problem remains in find $\mathbf{x}(t)$ excited by $\mathbf{x}(t_0)$ and $\mathbf{u}(t)$ for $t \geq 0$. For power electronics converters under steady-state operation, the $\mathbf{x}(t_0)$ usually define the inductor current and capacitor voltage values at the beginning of each switching cycle, which are unknown values. Thus, excited by the input $\mathbf{u}(t)$, the problem is extended to find the TD solution for $\mathbf{x}(t)$ and $\mathbf{y}(t)$, and find the state-vector initial condition $\mathbf{x}(t_0)$.

The TD solution of the state-equation for an LTI system or even for a PWL system is not new in literature, being earlier studied in power electronics applications by (KASSAKIAN ET AL., 1991). However, the solution is developed in the discrete-time, differing from the CT employed here. On the other hand, state-space TD solution is not commonly employed to analyze the steady-state behavior of resonant converters, which is seen as an opportunity to assess its potentialities further and pave the way to consolidate this procedure. With this purpose, this chapter follows presenting a generic PWL system and its TD solution. In sequence, the DC/DC LLC resonant LED driver TD solution is developed.

4.2.1 TD Solution of a PWL System

Fig. 39 shows the evolve of a single state variable $x_i(t)$ over a switching cycle T_S for a characterized PWL system. Each step in Fig. 39 corresponds to a CT LTI system. During the proposed analysis, t_0 is considered the origin time 0, which is in phase with the switch's control signal. The time t_{Z1} is the instantaneous transition time between Step 1 (S1) and Step 2 (S2),

Figure 39 – Generic state-variable waveform in a variable structure system.



Source: Author.

t_{Z2} correspond to the transition time between S2 and Step 3 (S3), and so on. For the case shown in Fig. 39, the converter switching cycle is composed of six stages, and t_{Z6} corresponds to the switching period T_S.

It is worth mentioning that because of the resonant converter's natural behavior, some transition times arise from indirectly controlled events, so they also become unknown variables. In this way, the problem is further extended to find the indirectly controlled transition times, the state-vector $\mathbf{x}(t)$ and the state-vector initial condition $\mathbf{x}(t_0)$ excited by the input $\mathbf{u}(t)$ for $t \geq 0$. Power electronics converters with indirectly determined transition times present a more complex solution since they depend on the converter parameters, load conditions, and steady-state conditions. Thus, an exact prediction, principally of the indirectly controlled transition times, could be a fundamental key to better understand the converter behavior.

4.2.1.1 Step 1 (S1) time-domain solution : $(t_0, t_{Z1}]$

The choice of 0 as the time origin is arbitrary for a time invariant system (KASSAKIAN ET AL., 1991), thus the state-vector TD solution given in (4.2) can be rewrite as (4.3).

$$\mathbf{x}(t) = e^{\mathbf{A}(t-t_0)}\mathbf{x}(t_0) + \int_{t_0}^{t} e^{\mathbf{A}(t-\tau)}\mathbf{B}\mathbf{u}(\tau)d\tau \tag{4.3}$$

In this way, the TD solution for the first step $\mathbf{x_{S1}}(t)$ is given by (4.4). Where $\mathbf{A_{S1}}$ and $\mathbf{B_{S1}}$ are the matrices related to step 1 (S1).

$$\mathbf{x_{S1}}(t) = e^{\mathbf{A_{S1}}(t-t_0)}\mathbf{x_{S1}}(t_0) + \int_{t_0}^{t} e^{\mathbf{A_{S1}}(t-\tau)}B_{\mathbf{S1}}\mathbf{u}(\tau)d\tau \tag{4.4}$$

At the end of the first step $S1$, exactly at t_{Z1}, the state-vector value is given by (4.5).

$$\mathbf{x_{S1}}(t_{Z1}) = e^{\mathbf{A_{S1}}(t_{Z1}-t_0)}\mathbf{x_{S1}}(t_0) + \int_{t_0}^{t_{Z1}} e^{\mathbf{A_{S1}}(t_{Z1}-\tau)}\mathbf{B_{S1}}\mathbf{u}(\tau)d\tau \tag{4.5}$$

Simplifying (4.5), expression (4.6) is obtained.

$$\mathbf{x_{S1}}(t_{Z1}) = e^{\mathbf{A_{S1}}(t_{Z1}-t_0)}\mathbf{x_{S1}}(t_0) + e^{\mathbf{A_{S1}}(t_{Z1})}\int_{t_0}^{t_{Z1}} e^{-\mathbf{A_{S1}}(\tau)}\mathbf{B_{S1}}\mathbf{u}(\tau)d\tau \tag{4.6}$$

Adopting integration by substitution, making $\tau = \zeta + t_0$ and after some calculations, the state-vector at t_{Z1} is given by (4.7).

$$\mathbf{x_{S1}}(t_{Z1}) = e^{\mathbf{A_{S1}}(t_{Z1}-t_0)}\mathbf{x_{S1}}(t_0) + e^{\mathbf{A_{S1}}(t_{Z1})}\int_0^{t_{Z1}-t_0} e^{-\mathbf{A_{S1}}(\zeta+t_0)}\mathbf{B_{S1}}\mathbf{u}(\zeta)d\zeta \tag{4.7}$$

Simplifying (4.7), one obtain (4.8).

$$\mathbf{x_{S1}}(t_{Z1}) = e^{\mathbf{A_{S1}}(t_{Z1}-t_0)}\mathbf{x_{S1}}(t_0) + e^{\mathbf{A_{S1}}(t_{Z1}-t_0)}\int_0^{t_{Z1}-t_0} e^{-\mathbf{A_{S1}}(\zeta)}\mathbf{B_{S1}}\mathbf{u}(\zeta)d\zeta \tag{4.8}$$

In order to compress the representation of (4.8), the variables $\mathbf{\Psi h_{S1}}$ and $\mathbf{\Psi p_{S1}}$ given in (4.9) and (4.10) are defined, which are related to the zero-input and zero-state response, respectively. The solution of (4.9) is also known as the state-transition matrix.

$$\mathbf{\Psi h_{S1}}(t_{Z1}) = e^{\mathbf{A_{S1}}(t_{Z1}-t_0)} \tag{4.9}$$

$$\mathbf{\Psi p_{S1}}(t_{Z1}) = \int_0^{t_{Z1}-t_0} e^{-\mathbf{A_{S1}}(\zeta)}B_{\mathbf{S1}}\mathbf{u}(\zeta)d\zeta \tag{4.10}$$

Now substituting (4.9) and (4.10) in (4.8), the state-vector value at t_{Z1} can be rewrite by (4.11).

$$\mathbf{x_{S1}}(t_{Z1}) = \mathbf{\Psi h_{S1}}(t_{Z1})\mathbf{x_{S1}}(t_0) + \mathbf{\Psi h_{S1}}(t_{Z1})\mathbf{\Psi p_{S1}}(t_{Z1}) \tag{4.11}$$

4.2.1.2 Step 2 (S2) time-domain solution: $(t_{Z1}, t_{Z2}]$

Employing (4.3), the second step (S2) TD solution is given by (4.12).

$$\mathbf{x_{S2}}(t) = e^{\mathbf{A_{S2}}(t-t_0)}\mathbf{x_{S2}}(t_0) + \int_{t_0}^{t} e^{\mathbf{A_{S2}}(t-\tau)}\mathbf{B_{S2}}\mathbf{u}(\tau)d\tau \tag{4.12}$$

The second step involves the time interval $(t_{Z1}, t_{Z2}]$, hence in S2 the $t_0 = t_{Z1}$, which means that the initial time of the second step corresponds to the final time of the first step. This condition is in agreement with (KASSAKIAN ET AL., 1991), where it is stated that to invoke the continuity of the state variables, the final state of one step becomes the initial state for the next. This statement is better understood when the state variables are capacitor voltages and inductor currents, where discontinuities in the instantaneous transitions times are physically not allowed.

Thus, being $t_0 = t_{Z1}$, and considering that S2 ends at t_{Z2}, the state-vector TD solution

for S2 is given by (4.13).

$$\mathbf{x_{S2}}(t) = e^{\mathbf{A_{S2}}(t-t_{Z1})}\mathbf{x_{S2}}(t_{Z1}) + \int_{t_{Z1}}^{t_{Z2}} e^{\mathbf{A_{S2}}(t-\tau)}\mathbf{B_{S2}}\mathbf{u}(\tau)d\tau \tag{4.13}$$

Considering the state variables evolve during S2 due to the initial condition $\mathbf{x_{S1}}(t_{Z1}) = \mathbf{x_{S2}}(t_{Z1})$ and the input $\mathbf{u}(t)$ excitation, and assuming $\tau = \zeta + t_{Z1}$, after some simplifications, the state-vector at t_{Z2} is given by (4.14).

$$\mathbf{x_{S2}}(t_{Z2}) = e^{\mathbf{A_{S2}}(t_{Z2}-t_{Z1})}\mathbf{x_{S2}}(t_{Z1}) + e^{\mathbf{A_{S2}}(t_{Z2}-t_{Z1})}\int_{0}^{t_{Z2}-t_{Z1}} e^{-\mathbf{A_{S2}}(\zeta)}\mathbf{B_{S2}}\mathbf{u}(\zeta)d\zeta \tag{4.14}$$

In the same way, as it was done for S1, to simplify the representation of the solution, (4.15) is defined.

$$\mathbf{\Psi h_{S2}}(t_{Z2}) = e^{\mathbf{A_{S2}}(t_{Z2}-t_{Z1})} \tag{4.15a}$$

$$\mathbf{\Psi p_{S2}}(t_{Z2}) = \int_{0}^{t_{Z2}-t_{Z1}} e^{-\mathbf{A_{S2}}(\zeta)}B_{\mathbf{S2}}\mathbf{u}(\zeta)d\zeta \tag{4.15b}$$

In this way, the state-vector value at t_{Z2} can be rewrite by (4.16).

$$\mathbf{x_{S2}}(t_{Z2}) = \mathbf{\Psi h_{S2}}(t_{Z2})\mathbf{x_{S2}}(t_{Z1}) + \mathbf{\Psi h_{S2}}(t_{Z2})\mathbf{\Psi p_{S2}}(t_{Z2}) \tag{4.16}$$

As aforesaid, due to the continuity of state variables, the final state of one step becomes the initial state for the next one, which is given by (4.17) for the second step.

$$\mathbf{x_{S2}}(t_{Z1}) = \mathbf{x_{S1}}(t_{Z1}) \tag{4.17}$$

Thus, considering (4.17), and substituting (4.11) into (4.16), the state-vector value at t_{Z2} is be given by (4.18).

$$\mathbf{x_{S2}}(t_{Z2}) = \mathbf{\Psi h_{S2}}(t_{Z2})\mathbf{\Psi h_{S1}}(t_{Z1})\mathbf{x_{S1}}(t_0) + \mathbf{\Psi h_{S2}}(t_{Z2})\mathbf{\Psi h_{S1}}(t_{Z1})\mathbf{\Psi p_{S1}}(t_{Z1}) + \mathbf{\Psi h_{S2}}(t_{Z2})\mathbf{\Psi p_{S2}}(t_{Z2}) \tag{4.18}$$

4.2.1.3 Step 3 (S3) time-domain solution: $(t_{Z2}, t_{Z3}]$

The third step is analyzed following the same methodology employed in the previous two steps. Therefore, $t_0 = t_{Z2}$. During the third step, the state-vector variables will evolve as given by (4.19), up until its convergence to the value given in (4.20) for $t = t_{Z3}$.

$$\mathbf{x_{S3}}(t) = e^{\mathbf{A_{S3}}(t-t_{Z2})}\mathbf{x_{S3}}(t_{Z2}) + \int_{t_{Z2}}^{t} e^{\mathbf{A_{S3}}(t-\tau)}\mathbf{B_{S3}}\mathbf{u}(\tau)d\tau \tag{4.19}$$

$$\mathbf{x_{S3}}(t_{Z3}) = e^{\mathbf{A_{S3}}(t_{Z3}-t_{Z2})}\mathbf{x_{S3}}(t_{Z2}) + \int_{t_{Z2}}^{t_{Z3}} e^{\mathbf{A_{S3}}(t_{Z3}-\tau)}\mathbf{B_{S3}}\mathbf{u}(\tau)d\tau \tag{4.20}$$

With integration by substitution, where $\tau = \zeta + t_{Z2}$ and after some simplifications, the state-vector value at t_{Z3} is given by (4.21).

$$\mathbf{x_{S3}}(t_{Z3}) = e^{\mathbf{A_{S3}}(t_{Z3}-t_{Z2})}\mathbf{x_{S3}}(t_{Z2}) + e^{\mathbf{A_{S3}}(t_{Z3}-t_{Z2})}\int_{0}^{t_{Z3}-t_{Z2}} e^{-\mathbf{A_{S3}}(\zeta)}\mathbf{B_{S3}}\mathbf{u}(\zeta)d\zeta \tag{4.21}$$

Taking into account the definitions in (4.22), the state-vector value at t_{Z3} defined in (4.21) can be rewrite by (4.23).

$$\mathbf{\Psi h_{S3}}(t_{Z3}) = e^{\mathbf{A_{S3}}(t_{Z3}-t_{Z2})} \tag{4.22a}$$

$$\mathbf{\Psi p_{S3}}(t_{Z3}) = \int_{0}^{t_{Z3}-t_{Z2}} e^{-\mathbf{A_{S3}}(\zeta)}B_{\mathbf{S3}}\mathbf{u}(\zeta)d\zeta \tag{4.22b}$$

$$\mathbf{x_{S3}}(t_{Z3}) = \mathbf{\Psi}\boldsymbol{h}_{\mathbf{S3}}(t_{Z3})\mathbf{x_{S3}}(t_{Z2}) + \mathbf{\Psi}\boldsymbol{h}_{\mathbf{S3}}(t_{Z3})\mathbf{\Psi}\boldsymbol{p}_{\mathbf{S3}}(t_{Z3}) \tag{4.23}$$

Due to the continuity of the state variables $\mathbf{x_{S3}}(t_{Z2}) = \mathbf{x_{S2}}(t_{Z2})$. Then, substituting (4.18) into (4.23), the state-vector condition at t_{Z3} will be given by (4.24).

$$\begin{aligned}\mathbf{x_{S3}}(t_{Z3}) = {} & \mathbf{\Psi h_{S3}}(t_{Z3})\mathbf{\Psi h_{S2}}(t_{Z2})\mathbf{\Psi h_{S1}}(t_{Z1})\mathbf{x_{S1}}(t_0) + \mathbf{\Psi h_{S3}}(t_{Z3})\mathbf{\Psi h_{S2}}(t_{Z2})\mathbf{\Psi h_{S1}}(t_{Z1})\mathbf{\Psi p_{S1}}(t_{Z1}) \\ & + \mathbf{\Psi h_{S3}}(t_{Z3})\mathbf{\Psi h_{S2}}(t_{Z2})\mathbf{\Psi p_{S2}}(t_{Z2}) + \mathbf{\Psi h_{S3}}(t_{Z3})\mathbf{\Psi p_{S3}}(t_{Z3})\end{aligned} \tag{4.24}$$

As shown in the presented analysis up to this point, there are two main equations for each step. The first one dictates the evolve for the state-vector variables taking into account

the initial condition at this step and the input excitation. The second equation computes the state-vector exact value at the transition time that characterizes the end of this step. To avoid further equations obtained from the same systematic development, the solution for N steps is generalized in the following subsection.

4.2.1.4 General time-domain solution for N steps

The general equation that governs the evolve of the state-vector variables during a specific step N (SN) is given by (4.25). Throughout SN, the state-vector values evolve from their initial condition ($\mathbf{x_{S(N-1)}}(t_{Z(N-1)})$) up to its convergence value given by the state-vector value at the transition time t_{ZN} that characterize the end of the current N step and the beginning of the next step $N+1$. The convergence value $\mathbf{x_{SN}}(t_{ZN})$ is given by (4.26). Wherein, $\mathbf{\Psi h_{SN}}(t_{ZN})$ and $\mathbf{\Psi p_{SN}}(t_{ZN})$ are given in (4.27) and (4.28), respectively.

$$\mathbf{x_{SN}}(t) = e^{\mathbf{A_{SN}}(t-t_{Z(N-1)})}\mathbf{x_{S(N-1)}}(t_{Z(N-1)}) + \int_{t_{Z(N-1)}}^{t} e^{\mathbf{A_{SN}}(t-\tau)}\mathbf{B_{SN}}\mathbf{u}(\tau)d\tau \tag{4.25}$$

$$\mathbf{x_{SN}}(t_{ZN}) = \mathbf{\Psi h_{SN}}(t_{ZN})\mathbf{x_{S(N-1)}}(t_{Z(N-1)}) + \mathbf{\Psi h_{SN}}(t_{ZN})\mathbf{\Psi p_{SN}}(t_{ZN}) \tag{4.26}$$

$$\mathbf{\Psi h_{SN}}(t_{ZN}) = e^{\mathbf{A_{SN}}(t_{ZN}-t_{Z(N-1)})} \tag{4.27}$$

$$\mathbf{\Psi p_{SN}}(t_{ZN}) = \int_{0}^{t_{ZN}-t_{Z(N-1)}} e^{-\mathbf{A_{SN}}(\zeta)}\mathbf{B_{SN}}\mathbf{u}(\zeta)d\zeta \tag{4.28}$$

From (4.25) and (4.26), $\mathbf{x_{S(N-1)}}(t_{Z(N-1)})$ defines the initial state-vector value at step N, which is given by the state-vector values at the end of step $N-1$. Since $\mathbf{x_{S(N-1)}}(t_{Z(N-1)})$ takes into account the initial state value at time 0 and the state-variables evolves overall steps before N, its general expression is given by (4.29).

$$\mathbf{x_{S(N-1)}}(t_{Z(N-1)}) = \left[\prod_{i=N}^{2} \mathbf{\Psi h_{S(i-1)}}\left(t_{Z(i-1)}\right)\right]\mathbf{x_{S1}}(t_0) + \sum_{k=1}^{N-1}\left[\prod_{i=N}^{k+1} \mathbf{\Psi h_{S(i-1)}}\left(t_{Z(i-1)}\right)\right]\mathbf{\Psi p_{Sk}}(t_{Zk}) \tag{4.29}$$

Finally, to obtain the TD solution of a PWL system, it becomes necessary to compute (4.25), (4.26) and (4.29). However, in order to diminish the computational effort, considering that the input $\mathbf{u}(t)$ is constant over the switching cycle T_S, the matrix exponential integral can be computed by (4.30) for non-singular $\mathbf{A}$.

$$\int_0^t e^{\mathbf{A}t}\mathbf{B}\mathbf{u}(t)dt = \mathbf{A}^{-1}(e^{\mathbf{A}t} - \mathbf{I})\mathbf{B}\mathbf{u} \tag{4.30}$$

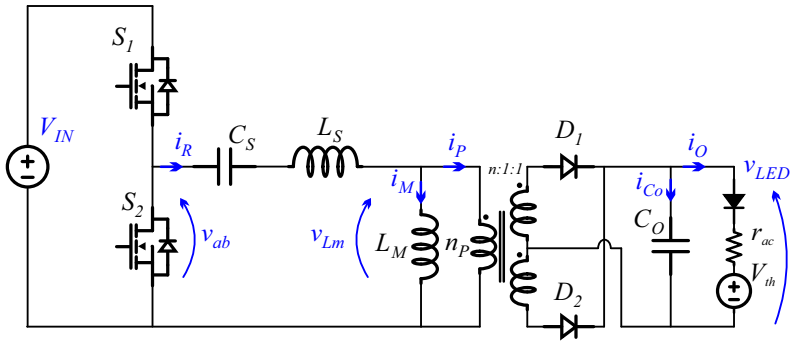
Even that the presented solution is treated in a generic way for N steps over a switching cycle, it is known that power electronics applications present a low number of steps. For instance, PWM converters have mainly two stages in the CCM, and three stages in the DCM. On the other hand, resonant converters can present more steps as a function of the operation condition, converter parameters, and topology. However, because of the symmetrical behavior of resonant converters controlled by variable switching frequency with a 50% duty-cycle, the number of steps that need to be analyzed is reduced to half. Focusing on the DC/DC LLC resonant LED driver, the next section will detail the LLC resonant stages, which are the piece-wise linear structures (Steps N) that the converter can assume over a switching cycle. These stages settled in different sequences will result in several operating modes of the converter, which are analyzed in the sequence.

4.3 RESONANT STAGES OF THE LLC RESONANT LED DRIVER

4.3.1 Ideal LLC resonant LED driver with PFM and 50% duty-cycle

Fig. 40 shows the circuit schematic of the LLC resonant LED driver. As function of the circuit elements (L_S, C_S, L_M, C_O, n), input voltage (V_{IN}), HB switching frequency (f_{sw}) and load conditions (r_{ac}, V_{th}), the LLC converter can operate with multiple resonant stages within T_S (X. FANG, HU, Z. J. SHEN ET AL., 2012). The analysis of the resonant stages for the LLC resonant converter is based on the assessment of all the possible structures that the system can assume throughout its operation. Each structure, which corresponds to a resonant stage, has its own equivalent circuit, differing mainly in the switches and diodes conducting state.

Figure 40 – DC/DC LLC resonant converter schematic diagram.

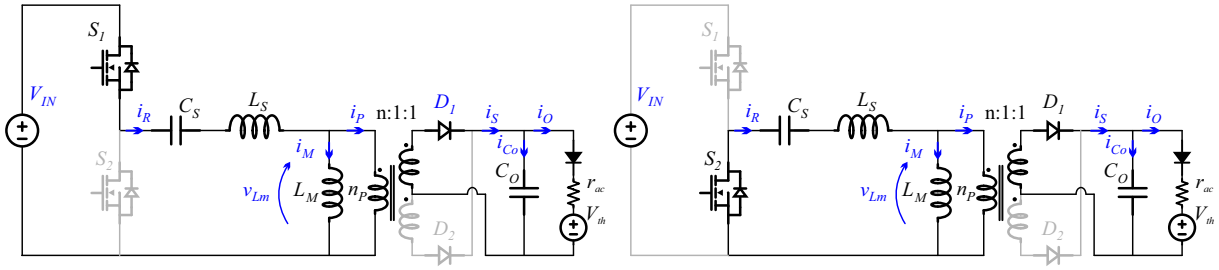


Source: Author.

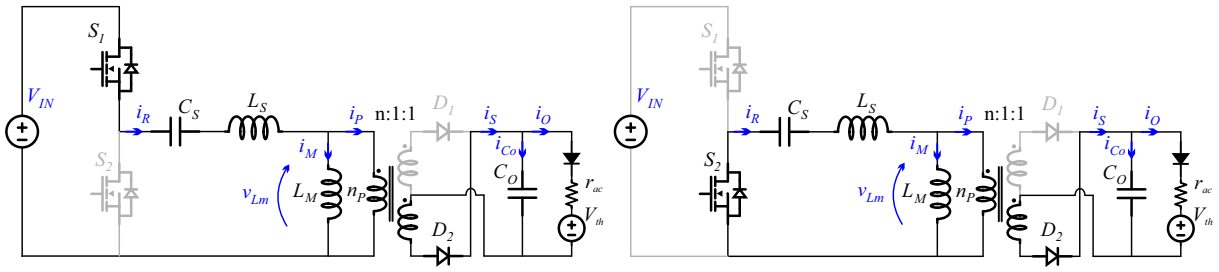
Assuming steady-state operation, neglecting dead-time, and considering all elements as ideal, six possible resonant stages are identified for one switching cycle of the HB LLC resonant LED driver. These stages are classified as a function of L_M voltage (v_{Lm}) and HB switches state (On or Off). Fig. 41 shows the LLC converter equivalent circuit for each identified resonant stage. The resonant stage characterized by L_M positive clamped $v_{Lm}(t) = nv_{Co}(t)$, is named Stage P or P', as a function of the HB switches conducting state, where $v_{Co}(t) = v_{LED}$ is the output capacitor voltage, and n the transformer turns ratio. In the same way, for L_M negative clamped $v_{Lm}(t) = -nv_{Co}(t)$, the resonant stage is named N or N'. Finally, the stage where $|v_{Lm}(t)| \leq nv_{Co}(t)$ is named O or O'. Unlike all the works mentioned above that deal with the LLC converter TD solution, the output voltage is not approximated by its average value V_O. For

Figure 41 – Equivalent circuit of the DC/DC LLC converter linear resonant stages.

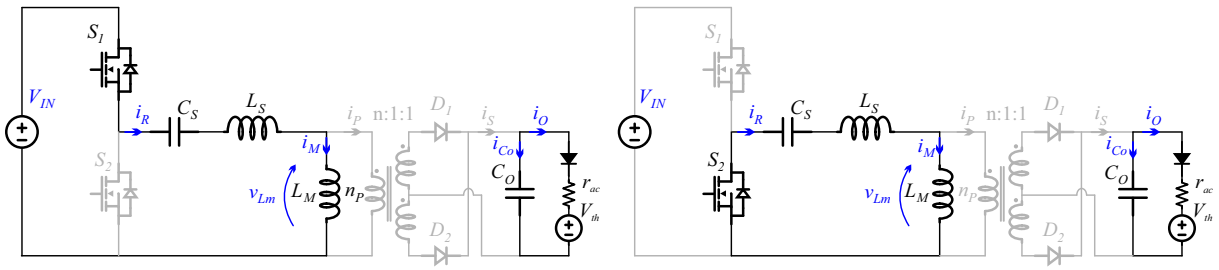
(a) – Left-trace: Stage P; Right-trace: Stage P'.



(b) – Left-trace: Stage N; Right-trace: Stage N'.



(c) – Left-trace: Stage O; Right-trace: Stage O'.



Source: Author.

the sake of clarity, it is worthy of mentioning that the name given to each resonant stage follows (X. FANG, HU, Z. J. SHEN ET AL., 2012), and (DENG ET AL., 2015).

Assuming that the LLC converter employs PFM with 50% duty-cycle to regulate the output, the resonant tank current and voltage waveforms are symmetrical to the other half-switching cycle (X. FANG, HU, Z. J. SHEN ET AL., 2012). Thus, it is possible to simplify the LLC analysis by focusing on the resonant stages that occur during the first half-switching-cycle, defined when S_1 is ON, and S_2 is OFF.

4.3.1.1 Resonant stages state-space equations for the idealized LLC converter

Stage P:

In stage P, since L_M is clamped by nv_{Co}, the magnetizing current i_M will increases according to the integration of $nv_{Co}(t)$. Stage P starts when the resonant current i_R becomes higher than i_M, which implies that the voltage at L_M experimented becoming higher than nv_{Co}, imposing diode D_1 start to conduct. Otherwise, this mode will not start. On the other hand, stage P finishes at the end of a half-switching cycle or due to a condition that enables another resonant stage. Over stage P, since L_M remains clamped by nv_{Co} the current i_M increases its value, and i_R has to be mandatory higher than i_M. However, owing to the natural progress of i_R, its resonant value will converge to i_M. At this moment, a mandatory condition of stage P $(i_R \geq i_M)$ will be transgressed, and as a function of the v_{Lm} the next stage will occur, for instance, N or O. Moreover, it should be noticed that during stage P, L_M does not participate in the resonance, since its voltage is clamped. Besides, the instantaneous difference between i_R and i_M is the current that flows from the primary to the transformer's secondary side, which transfers energy to output.

Applying Kirchhoff's voltage and current laws on the equivalent circuit of the stage P shown in Fig. 41(a), the differential equations that rule the evolve of each state variable are obtained. Considering the state-vector variables shown in (4.31), the obtained state variables differential equations for stage P are given by (4.32). It is worthy of mentioning that the output equation $y(t)$ from the state-space representation can be defined in such a way to correspond to the voltage and current at every single element of the converter. However, this extra computation will not bring further contributions at this point.

$$\mathbf{x}(t) = \begin{bmatrix} i_R(t) \\ v_{Cs}(t) \\ i_M(t) \\ v_{Co}(t) \end{bmatrix} \tag{4.31}$$

$$\frac{di_R(t)}{dt} = \frac{V_{IN}}{L_S} - \frac{v_{C_S}(t)}{L_S} - \frac{nv_{Co}(t)}{L_S} \tag{4.32a}$$

$$\frac{dv_{Cs}(t)}{dt} = \frac{i_R(t)}{L_S} \tag{4.32b}$$

$$\frac{di_M(t)}{dt} = \frac{nv_{Co}(t)}{L_M} \tag{4.32c}$$

$$\frac{dv_{Co}(t)}{dt} = \frac{ni_R(t)}{C_O} - \frac{ni_M(t)}{C_O} - \frac{v_{Co}(t)}{r_{ac}C_O} + \frac{V_{th}}{r_{ac}C_O} \tag{4.32d}$$

Considering $\mathbf{x}(t)$, and state differential equations, each LLC resonant stage can be represented by the equivalent state-space equation, defined by (4.1). For the resonant stage P, the constant matrices are named as $\mathbf{A_P}$ and $\mathbf{B_P}$, shown in (4.33) and (4.34), respectively. Besides, the input signals $\mathbf{u}(t)$ are given by (4.35). It should be noticed that the inputs $\mathbf{u}(t)$ are time independent variables over a switching-cycle T_S.

$$\mathbf{A_P} = \begin{bmatrix} 0 & -\frac{1}{L_S} & 0 & -\frac{n}{L_S} \\ \frac{1}{C_S} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{n}{L_M} \\ \frac{n}{C_O} & 0 & -\frac{n}{C_O} & -\frac{1}{r_{ac}C_O} \end{bmatrix} \tag{4.33}$$

$$\mathbf{B_P} = \begin{bmatrix} \frac{1}{L_S} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & \frac{1}{r_{ac}C_O} \end{bmatrix} \tag{4.34}$$

$$\mathbf{u(t)} = \begin{bmatrix} V_{IN} \\ V_{th} \end{bmatrix} \tag{4.35}$$

Stage N:

Throughout stage N, L_M is clamped by $-nv_{Co}$, diode D_2 conducts current transferring energy to the output, and the i_R current is smaller than i_M. This stage starts when the voltage at L_M tries to become more negative than $-nv_{Co}$, which forces diode D_2 to start to conduct. To maintain the conduction of D_2, the magnitude of i_R current has to be smaller than i_M. Stage N is finished at the end of the half-switching cycle or due to a condition that enables another stage to start. Applying Kirchhoff's voltage and current laws on the equivalent circuit of the stage N shown in Fig. 41(b), the system state-space equations are determined, being the matrices $\mathbf{A_N}$ and $\mathbf{B_N}$, shown in (4.36) and (4.37), respectively.

$$\mathbf{A_N} = \begin{bmatrix} 0 & -\frac{1}{L_S} & 0 & \frac{n}{L_S} \\ \frac{1}{C_S} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{n}{L_M} \\ -\frac{n}{C_O} & 0 & \frac{n}{C_O} & -\frac{1}{r_{ac}C_O} \end{bmatrix} \tag{4.36}$$

$$\mathbf{B_N} = \begin{bmatrix} \frac{1}{L_S} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & \frac{1}{r_{ac}C_O} \end{bmatrix} \tag{4.37}$$

Stage O:

During the resonant stage O, the magnitude of v_{Lm} is not enough to force the conduction of any of the output rectifier diodes (D_1 or D_2). Consequently, the entirely resonant current i_R is flowing through L_M. This stage is mainly characterized by being the only resonant stage in which no power is transferred to the secondary side. Throughout this stage, C_O provides energy to load. Besides, since no current flows through the rectifier's diodes, the LLC operation mode that presents stage O is known as a DCM mode. Considering the equivalent circuit of the stage O shown in Fig. 41(c), the system state-space equations are obtained, being $\mathbf{A_O}$ and $\mathbf{B_O}$ shown in (4.38) and (4.39), respectively.

$$\mathbf{A_O} = \begin{bmatrix} 0 & \frac{-1}{L_S+L_M} & 0 & 0 \\ \frac{1}{C_S} & 0 & 0 & 0 \\ 0 & \frac{-1}{L_S+L_M} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{r_{ac}C_O} \end{bmatrix} \tag{4.38}$$

$$\mathbf{B_O} = \begin{bmatrix} \frac{1}{L_S+L_M} & 0 \\ 0 & 0 \\ \frac{1}{L_S+L_M} & 0 \\ 0 & \frac{1}{r_{ac}C_O} \end{bmatrix} \tag{4.39}$$

At this point, it is important to reinforce that no waveform approximations are taken. Besides, the resonant stages are analyzed considering the LED PWL model equivalent circuit.

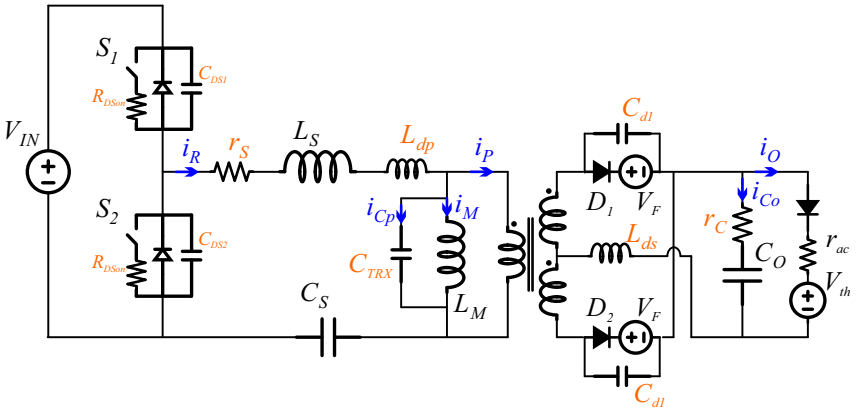
Therefore, a versatile solution is achieved since it can be easily adapted to resistive loads by making $V_{th} = 0$ and $r_{ac} = R_L$, or then employed to analyze LLC based battery charger.

4.3.2 Non-ideal LLC resonant LED driver and hybrid modulation

Fig. 42 shows the LLC schematic where several parasitic elements are considered, which certainly affect the converter behavior. In Fig. 42, r_S refers to the resonant tank series resistance; R_{DSon} is the MOSFET drain-to-source on resistance; C_{DS} is the MOSFET drain-to-source capacitance; L_{dp} and L_{ds} are the transformer leakage inductance; C_{TRX} correspond to the transformer equivalent capacitance, given by winding and layer capacitance; V_F is the diode forward voltage drop; C_d are rectifier diodes capacitance; and r_C is the series equivalent resistance of C_O. With the insertion of these parasitic elements, the LLC resonant stages analysis must be reviewed once new resonant stages arise. On the other hand, to simplify the analysis, each parasitic element's effect could be initially assessed by simulation. Then, the resonant stages should be evaluated, taking into account only the parasitic elements that strongly affect the converter behavior.

On the other hand, as well known, the LLC resonant LED driver is usually modulated by its switching frequency. However, the employment of hybrid modulation, where the inverter duty-cycle is also changed, could excel the converter performance under an extra-wide operating range. Therefore, due to the limitations of the first harmonic approaches, time-domain analysis for pulse width modulated resonant converters began to be seen in the literature. However, to maintain objectivity, this chapter follows, omitting the LLC converter's analysis where parasitic elements are considered and where hybrid modulation is employed. Such kind of analysis is not presented yet in the literature, being therefore here suggested as following developments of the current study. As will be seen at the end of this chapter, this analysis becomes necessary due to issues caused by parasitic components in predicting the converter behavior.

Figure 42 – LLC resonant LED driver schematic diagram considering parasitic elements.



Source: Author.

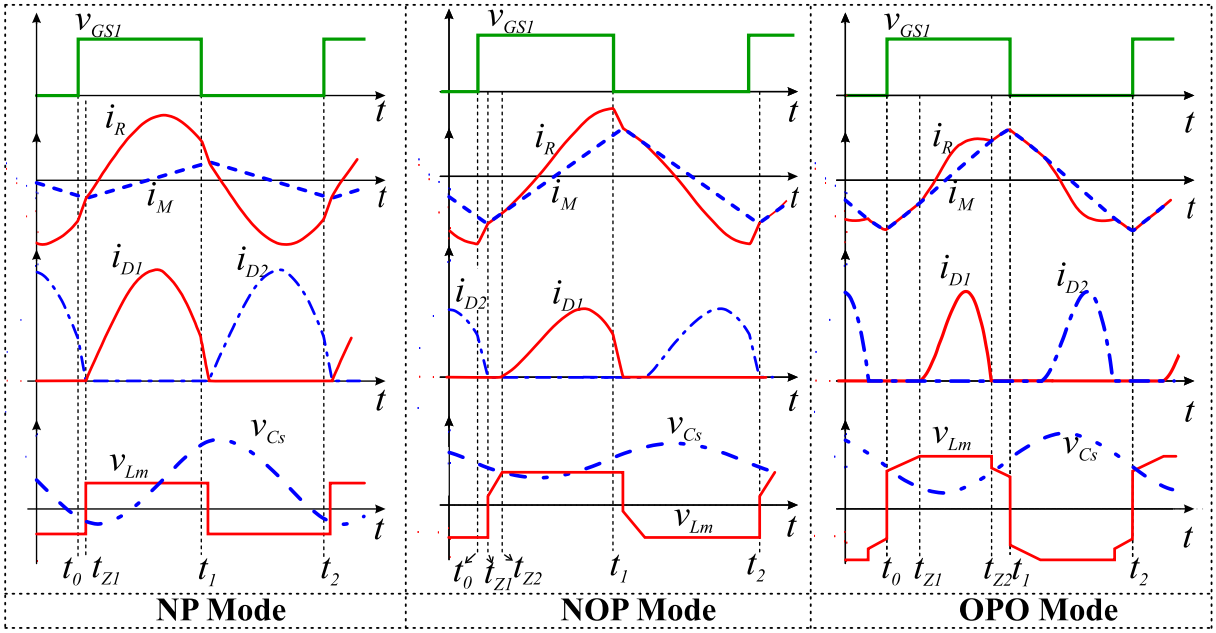
4.4 LLC LED DRIVER OPERATION MODES ANALYSIS

Different successive combinations of the resonant stages define the converter operating mode. For instance, PO mode indicates that in the first step (S1) the LLC operates at stage P and then at the transition time t_{Z1} enters stage O (second step - S2), which is finished at $t_{Z2} = T_S/2$. It should be noticed that due to the symmetrically behavior of a resonant converter with a constant 50% duty-cycle operation, only the resonant stages in the first half-cycle are used to define and analyze each operation mode of the idealized LLC converter with PFM.

For the idealized DC/DC LLC resonant LED driver, there are six main operation modes: PO, PON, PN, NP, NOP, and OPO, also previously recognized in (LAZAR ET AL., 2001), (X. FANG, HU, Z. J. SHEN ET AL., 2012), (Z. FANG, CAI ET AL., 2015) and (DENG ET AL., 2015) for the LLC converter supplying a resistive load. Fig. 43 and Fig. 44 shows the DC/DC LLC resonant LED driver main waveforms for the main different operation modes, where t_0 refers to the time 0, which is in phase with the switch S_1 gate signal v_{GS1}. As shown in Fig. 43 and Fig. 44, each LLC operation mode has its own voltage and current behavior and particular conditions that define the sequence of the stages. Each mode's incidence for a given designed converter (L_S, C_S, L_M, C_O, n) is a function of the f_{sw}, load condition (r_{ac}, V_{th}), and V_{IN}. Thus, all these variables have to be taken into account under the steady-state TD solution and the converter analysis.

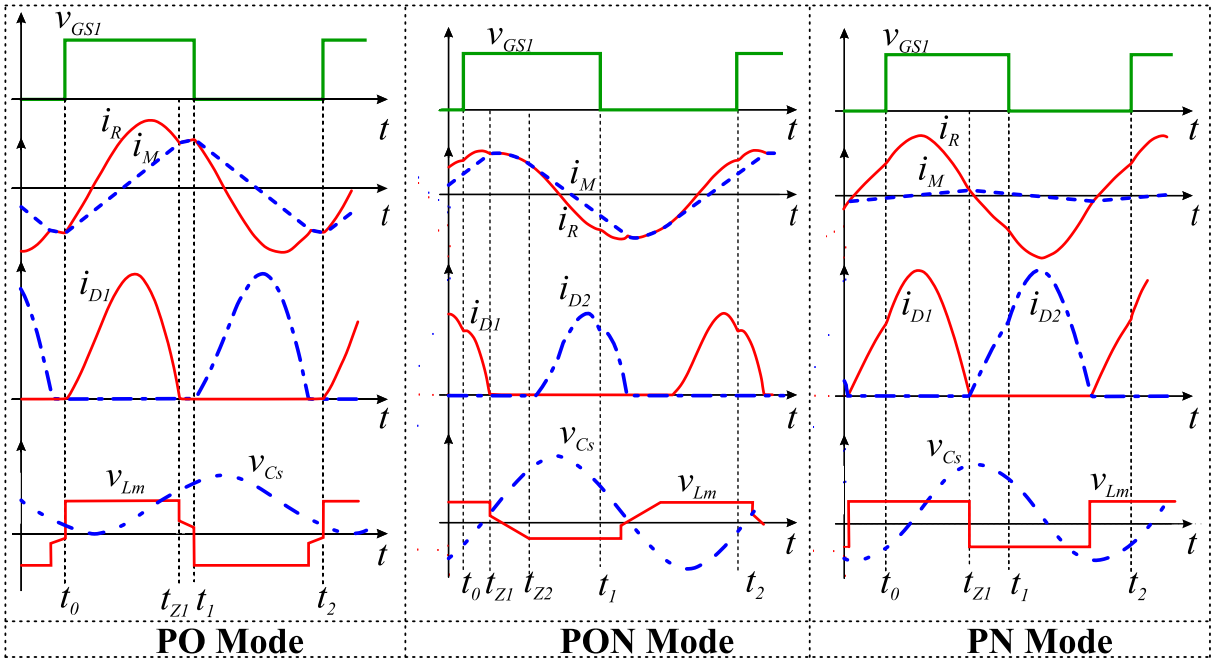
Analyzing Fig. 43 and Fig. 44, it can be seen that whether the LLC operation mode

Figure 43 – LLC resonant LED driver main waveforms for the NP, NOP, and OPO operation modes.



Source: Author.

Figure 44 – LLC resonant LED driver main waveforms for the PO, PON and PN operation modes.



Source: Author.

is given only by two steps, t_{Z2} will be equal to t_1, that correspond to the half-switching cycle $T_S/2$. The time instant t_2 correspond to T_S. Besides, it can be seen that the waveforms present symmetrical behavior related to the first half-switching cycle.

4.5 LLC RESONANT LED DRIVER TIME-DOMAIN SOLUTION

In this section, the procedure to obtain the TD solution of the idealized DC/DC LLC resonant LED driver converter under steady-state operation is described in detail. Under steady-state operation, the transition times t_{Z1}, t_{Z2} and t_{Z3} together with the converter state-vector initial value $\mathbf{x}(0)$ are the unknown variables that have to be initially determined. With these variables defined, knowing the input $\mathbf{u}(t)$ of the converter and the equations that govern the evolve of the state-vector $\mathbf{x}(t)$ over each step in the TD, the problem around the direct TD solution from state-space representation is solved. With the LLC converter behavior known in the TD, several analyses can be performed, including the assessment of current levels at specific times, for instance, during HB switches turn-off, RMS computation for all state variables, and so on.

Assuming that the operation mode (PO, PON, PN, NP, NOP, OPO) and all the parameters C_S, L_S, L_M, n, C_O, $V_{IN} = V_{BUS}$, f_{sw}, r_{ac}, and V_{th} are known, the procedure to obtain the steady-state TD solution of the LLC resonant LED driver is described step by step in the following sections.

4.5.1 Set up the system of equations to be numerically solved

To find out the transition times t_Z and the state-vector initial values $\mathbf{x}(t_0)$, the equations that define the state-vector values at the transition times ($\mathbf{x_{SN}}(t_{ZN})$) are employed to set up a system of equations to be numerically solved. The solution of this system of equations corresponds to the unknown variables.

Considering the symmetrical behavior of the LLC converter, it is possible to see in Fig. 43 and Fig. 44 that the state-vector values at t_1 have a close relationship with their initial condition at time t_0. The state-vector initial value is given by (4.40), where its relationship with the state-vector values at t_1 is defined by (4.41). Recognized this relationship, it is possible to see (4.41) as a system of equations, where the left side of (4.41) is defined employing (4.26)[2].

$$\mathbf{x}(\mathbf{t_0}) = \begin{bmatrix} I_{R0} & V_{CS0} & I_{M0} & V_{CO0} \end{bmatrix}^{\mathbf{T}} \tag{4.40}$$

$$i_R(t_1) = -I_{R0} \tag{4.41a}$$
$$v_{Cs}(t_1) = V_{IN} - V_{CS0} \tag{4.41b}$$
$$i_M(t_1) = -I_{M0} \tag{4.41c}$$
$$v_{Co}(t_1) = V_{CO0} \tag{4.41d}$$

Now, considering for instance the PO mode, there are five unknown variables (I_{R0}, V_{CS0}, I_{M0}, V_{CO0}, and t_{Z1}), however only four equations are presented in (4.41). Thus, to solve this system of equations, a fifth equation has to be defined. Analyzing the PO operation mode main waveforms shown in Fig. 44, it is noticed that i_R at t_{Z1} is equal to i_M, from where the fifth missing equation is defined, given by (4.42).

$$i_R(t_{Z1}) = i_M(t_{Z1}) \tag{4.42}$$

Following the same analysis procedure presented above, the unknown variables and the system of equations that have to be solved for each LLC resonant LED driver operation mode are presented in Table 4. However, based on the analysis being carried out, some variables may become known, which shrinks the systems of equations that need to be solved. On the other hand, for instance, assuming that f_{sw} is unknown or any other parameter, an additional equation is needed, which is also presented in Table 4. In this way, six equations are presented for the PO mode. Finally, defined the system of equations to be solved, any computational mathematical software with embedded algorithms to solve a nonlinear system of equations can be used.

[2] $\mathbf{x_{SN}}(t_{ZN}) = \mathbf{\Psi h_{SN}}(t_{ZN})\mathbf{x_{S(N-1)}}(t_{Z(N-1)}) + \mathbf{\Psi h_{SN}}(t_{ZN})\mathbf{\Psi p_{SN}}(t_{ZN})$

Table 4 – System of equations for each operation mode of the LLC resonant LED driver

Mode	Variables	System of equations
NP	I_{R0}	$i_R(t_{Z2}) = -I_{R0}$
	V_{CS0}	$v_{Cs}(t_{Z2}) = V_{BUS} - V_{CS0}$
	I_{M0}	$i_M(t_{Z2}) = -I_{M0}$
	V_{CO0}	$v_{Co}(t_{Z2}) = V_{CO0}$
	t_{Z1}	$i_R(t_{Z1}) = i_M(t_{Z1})$
	$t_1 = \frac{T_S}{2} = t_{Z2}$	$\frac{L_M}{L_M+L_S}(V_{BUS} - v_{Cs}(t_{Z1})) = nv_{Co}(t_{Z1})$
NOP	I_{R0}	$i_R(t_{Z3}) = -I_{R0}$
	V_{CS0}	$v_{Cs}(t_{Z3}) = V_{BUS} - V_{CS0}$
	I_{M0}	$i_M(t_{Z3}) = -I_{M0}$
	V_{CO0}	$v_{Co}(t_{Z3}) = V_{CO0}$
	t_{Z1}	$i_R(t_{Z1}) = i_M(t_{Z1})$
	$t_1 = \frac{T_S}{2} = t_{Z3}$	$\frac{L_M}{L_M+L_S}(V_{BUS} - v_{Cs}(t_{Z2})) = nv_{Co}(t_{Z2})$
OPO	I_{R0}	$i_R(t_{Z3}) = -I_{R0} = -I_{M0}$
	V_{CS0}	$v_{Cs}(t_{Z3}) = V_{BUS} - V_{CS0}$
	I_{M0}	$i_M(t_{Z3}) = -I_{M0} = -I_{R0}$
	V_{CO0}	$v_{Co}(t_{Z3}) = V_{CO0}$
	t_{Z1}	$i_R(t_{Z2}) = i_M(t_{Z2})$
	$t_1 = \frac{T_S}{2} = t_{Z3}$	$\frac{L_M}{L_M+L_S}(V_{BUS} - v_{Cs}(t_{Z1})) = nv_{Co}(t_{Z1})$
PO	I_{R0}	$i_R(t_{Z2}) = -I_{R0} = -I_{M0}$
	V_{CS0}	$v_{Cs}(t_{Z2}) = V_{BUS} - V_{CS0}$
	I_{M0}	$i_M(t_{Z2}) = -I_{M0} = -I_{R0}$
	V_{CO0}	$v_{Co}(t_{Z2}) = V_{CO0}$
	t_{Z1}	$i_R(t_{Z1}) = i_M(t_{Z1})$
	$t_1 = \frac{T_S}{2} = t_{Z2}$	$\frac{L_M}{L_M+L_S}(V_{BUS} - v_{Cs}(t_{Z1})) = nv_{Co}(t_{Z1})$
PON	I_{R0}	$i_R(t_{Z3}) = -I_{R0}$
	V_{CS0}	$v_{Cs}(t_{Z3}) = V_{BUS} - V_{CS0}$
	I_{M0}	$i_M(t_{Z3}) = -I_{M0}$
	V_{CO0}	$v_{Co}(t_{Z3}) = V_{CO0}$
	t_{Z1}	$i_R(t_{Z1}) = i_M(t_{Z1})$
	$t_1 = \frac{T_S}{2} = t_{Z3}$	$\frac{L_M}{L_M+L_S}(V_{BUS} - v_{Cs}(t_{Z2})) = nv_{Co}(t_{Z2})$
PN	I_{R0}	$i_R(t_{Z2}) = -I_{R0}$
	V_{CS0}	$v_{Cs}(t_{Z2}) = V_{BUS} - V_{CS0}$
	I_{M0}	$i_M(t_{Z2}) = -I_{M0}$
	V_{CO0}	$v_{Co}(t_{Z2}) = V_{CO0}$
	t_{Z1}	$i_R(t_{Z1}) = i_M(t_{Z1})$
	$t_1 = \frac{T_S}{2} = t_{Z2}$	$\frac{L_M}{L_M+L_S}(V_{BUS} - v_{Cs}(t_{Z1})) = nv_{Co}(t_{Z1})$

Source: Author.

4.5.2 Compute the state variables steady-state solution in time-domain

Once defined the state-vector initial values and the transition times for the LLC resonant LED driver under a specific operation condition, the steady-state analysis follows

with the definition of the equation that defines the state-vector behavior under a half-switching cycle. To accomplish these tasks, the equation that dictates the state variables evolve in each step is employed during the related time interval, resulting in a piece-wise defined equation, as given by (4.43) for a three-step operation mode (NOP, OPO, and PON).

$$\mathbf{x}(t) = \begin{cases} \mathbf{x_{S1}}(t) & \text{if} \quad t_0 < t \leq t_{Z1}, \\ \mathbf{x_{S2}}(t) & \text{if} \quad t_{Z1} < t \leq t_{Z2}, \\ \mathbf{x_{S3}}(t) & \text{if} \quad t_{Z2} < t \leq t_{Z3} = T_S/2. \end{cases} \tag{4.43}$$

At this point, employing (4.43) and taking into account the symmetrical operation of the converter, the state-variables waveforms over a T_S can be plotted in the TD. Besides, with proper manipulation, the minimum, maximum, and RMS values for each state-variable can be computed. Furthermore, due to the TD solution, it is possible to obtain further understandings of the LLC resonant LED driver converter and investigate particular conditions. Namely, to mention one, the turn-off current of the HB switches can be evaluated, which analysis is not satisfactorily accurate with the FHA approach and not completely covered in the literature that deals with the TD solution of the LLC converter.

Similarly to the state variables steady-state solution in the TD, if the output equation is defined, the output variables evolve over a half-switching cycle can be directly evaluated by (4.44) for a three-step operation mode.

$$\mathbf{y}(t) = \begin{cases} \mathbf{C_{S1}}\mathbf{x_{S1}}(t) + \mathbf{D_{S1}}\mathbf{u}(t) & \text{if} \quad t_0 < t \leq t_{Z1}, \\ \mathbf{C_{S2}}\mathbf{x_{S2}}(t) + \mathbf{D_{S2}}\mathbf{u}(t) & \text{if} \quad t_{Z1} < t \leq t_{Z2}, \\ \mathbf{C_{S3}}\mathbf{x_{S3}}(t) + \mathbf{D_{S3}}\mathbf{u}(t) & \text{if} \quad t_{Z2} < t \leq t_{Z3}. \end{cases} \tag{4.44}$$

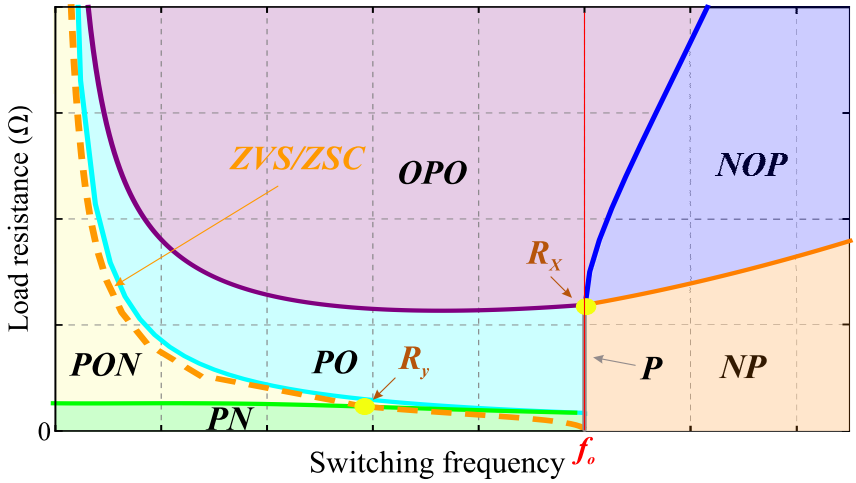
Finally, to elucidate the proposed TD solution procedure, Appendix B presents the script implemented in Wolfram MATHEMATICA to solve the LLC resonant LED driver under PO mode operation. The notebook developed in Wolfram MATHEMATICA to compute the LLC resonant LED driver TD solution can be accessed in the provided supplementary material of this thesis, which is described in Appendix G.

4.6 OPERATION MODE MAPPING

An interesting tool to analyze and obtain better insights into the LLC resonant LED driver converter can be developed by evaluating the boundary conditions of each operation mode, which yields on the so-called operation mode map. The proposed operating modes map relates the converter f_{sw} with the nonlinear equivalent load resistance, which takes into account the LED nonlinear electrical behavior approximated by the PWL equivalent circuit, discussed in Chapter 2.

From a generic point of view, Fig. 45 shows the proposed operation mode map. As can be seen, conditioned to the load resistance, a specific operating mode occurs for a given switching frequency value. The solid lines in this map indicate the boundary between the adjacent modes. After defining the load equivalent resistance, the related output voltage and current are also computed in the boundary condition, allowing further analysis of the converter. For instance, the same map can then be plotted for the output current at the boundary conditions as a switching frequency function.

Figure 45 – LLC resonant LED driver operation modes map.



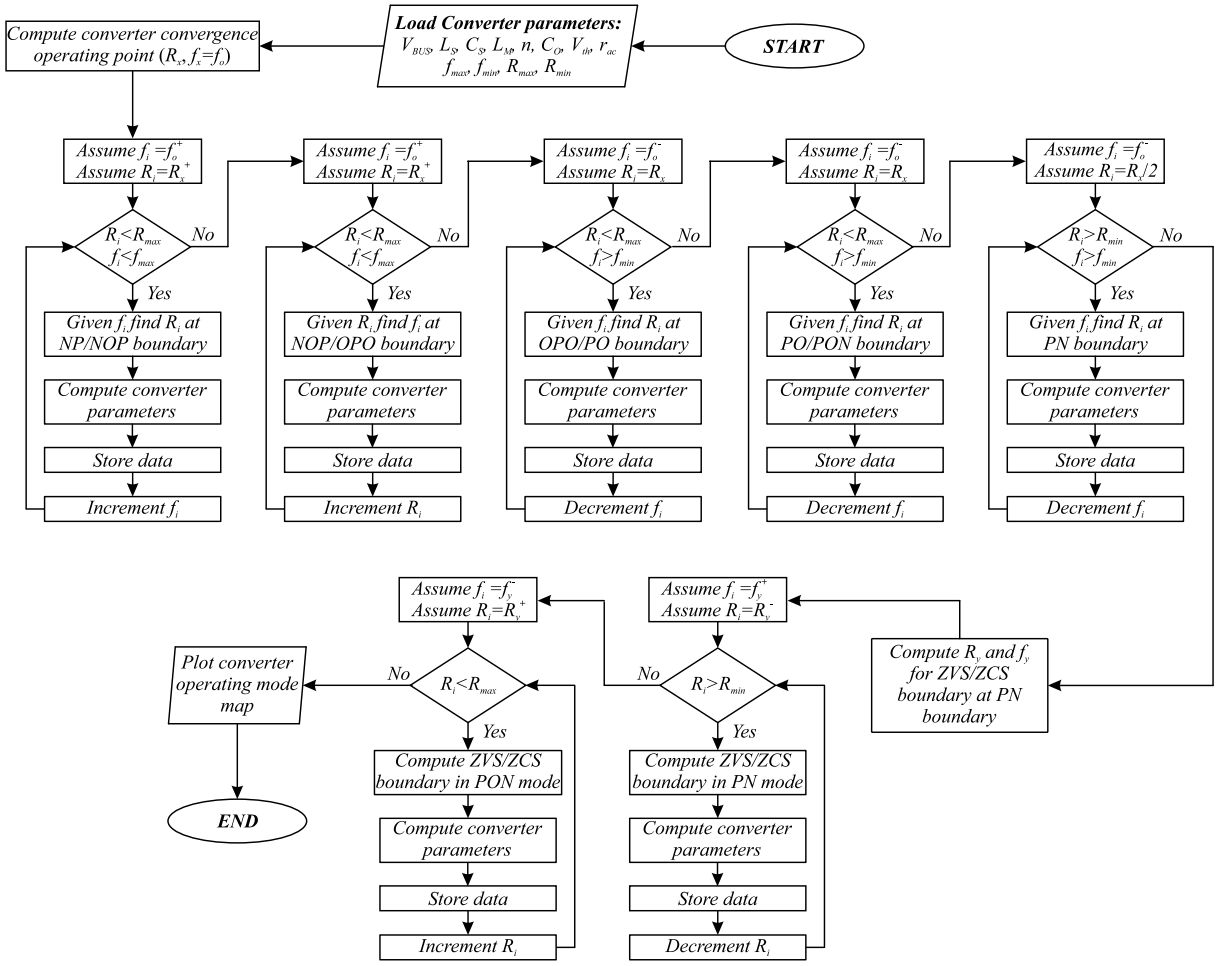
Source: Author.

The operating region for the six (NP, NOP, OPO, PO, PON, PN) main operation modes of the LLC are highlighted in Fig. 45. Besides, the P mode is shown, which occurs only at the resonance f_o for a specific load range $(0 - R_x)$. Analyzing Fig. 45, it is easy to see that NP and NOP modes occur only above f_o, and OPO mode occurs above and below f_o for light load condition. On the other hand, PO, PON, and PN modes are noticed only when the operation is below f_o. In addition, the ZVS/ZCS boundary is also added to the operating mode map. Thus, as can be seen, the ZVS/ZCS boundary is observed solely in PON or PN mode. Finally, it should be noticed that besides the relationship with the frequency, the occurrence of each operating mode depends on the equivalent load resistance.

Fig. 46 presents the flowchart of the proposed operating mode map for the LLC resonant LED driver. The first step inside the operating mode mapping algorithm is to load the LLC converter's real parameters. In the sequence, the minimal load (R_x) condition necessary for the P mode occurrence is computed. Analyzing Fig. 45, it can be seen that the operation point defined by R_x and f_o corresponds to the point where the NP, NOP, OPO, and P mode converge.

In the sequence, the boundary between NP and NOP mode is figured out. Therefore, f_i is defined as slightly higher than f_o for the first iteration. So, for this frequency f_i, the related load condition R_i at NP/NOP boundary is defined. In the sequence, considering the operation at f_i with R_i , the converter main parameters are computed. These main parameters are the output

Figure 46 – Flowchart of the proposed operating mode mapping tool for LLC resonant converter.



Source: Author

current and voltage, and electrical stress in all components, whose values can be employed in the development of further analysis, for instance, obtain the operation mode map relating output current (I_{LED}) and f_{sw}. In the next iteration, the frequency f_i is increased, and a new R_i value is computed. The iteration loop ends when the maximum frequency (f_{max}) or maximum resistance (R_{max}) value is achieved. These two values define the contour of the operating map.

However, to properly track the NP/NOP boundary the right system of equations has to be arranged. To exemplify this case, the NP operation mode is analyzed as follows. To guarantee the NP mode, v_{Lm} value at t_{Z1}, has to be equal nv_{Co}, which force the converter directly enter in stage P at t_{Z1}. Assuming that this condition is not satisfied, it means that $|v_{Lm}(t_{Z1})| \leq nv_{Co}(t_{Z1})$, resulting in the NOP operation mode. Thus it is concluded that NP mode made its boundary with NOP mode. This analysis exemplifies how the adjacent mode can be defined theoretically. Besides, it is useful to define the system of equations that need to be solved at the boundary conditions. Thus, for the NP/NOP boundary, the equations for the NP mode are employed. In this boundary tracking, since f_i is given, it means that t_1 is known. Then, the

unknown parameters are the initial state vector (I_{R0}, V_{CS0}, I_{M0}, V_{CO0}), transition time (t_{Z1}) and load condition R_i. Thus, six equations compose the system of equations to be solved. For the sake of completeness, these equations are given by

$$i_R(t_1) = -I_{R0} \tag{4.45a}$$

$$v_{Cs}(t_1) = V_{IN} - V_{CS0} \tag{4.45b}$$

$$i_M(t_1) = -I_{M0} \tag{4.45c}$$

$$v_{Co}(t_1) = V_{CO0} \tag{4.45d}$$

$$i_R(t_{Z1}) = i_M(t_{Z1}) \tag{4.45e}$$

$$\frac{L_M}{L_M + L_S}(V_{BUS} - v_{Cs}(t_{Z1})) = n v_{Co}(t_{Z1}) \tag{4.45f}$$

Following the operating mode mapping algorithm, the NOP/OPO boundary is assessed. This boundary is given by the OP mode, a particular mode that occurs only at this boundary. Similarly to the NP/NOP boundary, an iteration loop is employed to evaluate the OP mode. In each iteration, the proper system of equations is solved to define the unknown parameters. Further analyzing Fig. 46, it can be seen that a similar procedure is employed for each boundary. Thus, to avoid the recurrence of a similar analysis and discussion, further explanations are omitted. The notebook developed in Wolfram MATHEMATICA to compute the LLC resonant LED driver operation mode map can be accessed in the provided supplementary material of this thesis, which is described in Appendix G.

4.7 MODE SOLVER

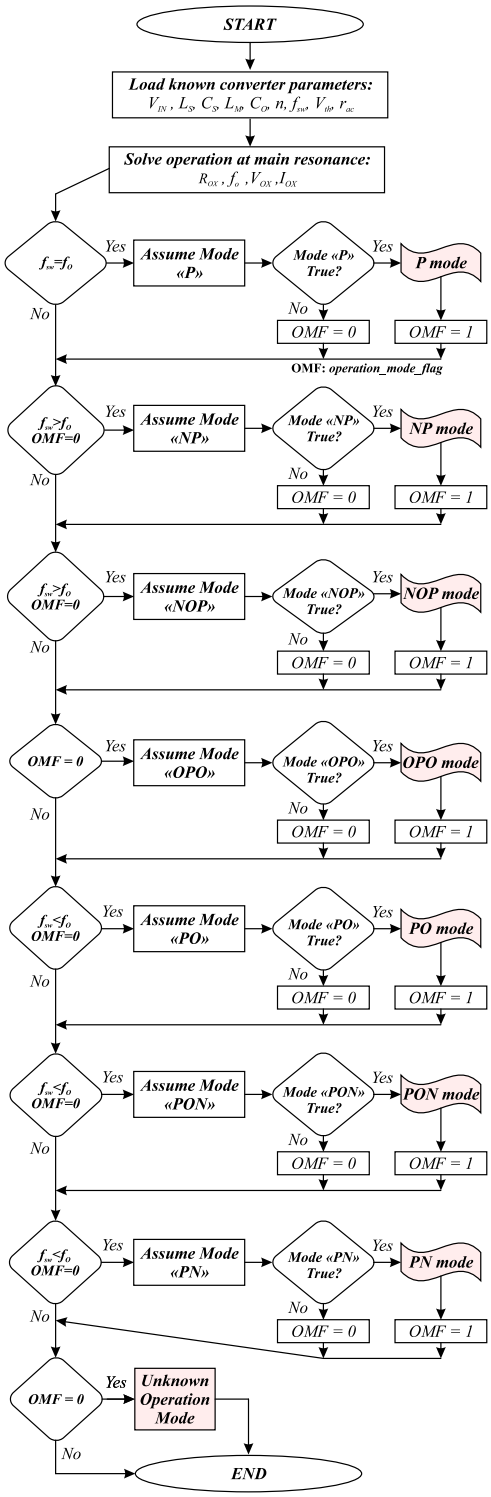
Previously in the steady-state TD solution for the LLC resonant LED driver, it was assumed that the operating mode was known. However, to automatically determine the converter's operating mode, an algorithm named mode solver is proposed. As it will be seen, the proposed mode solver employs some insights that originated from the operating mode map.

The conditions under where it is necessary to find the operation mode can differ as a function of the known or defined variables. For instance, in the simplest case, all parameters would be known, and the mode solver should be used only to define the operation mode. However, if the output current is defined, the algorithm must find f_{sw} and related operation mode. On the other hand, if f_{sw} is known, the mode solver can be employed to find the LED current and the corresponding operation mode under this condition.

The flowchart of the proposed mode-solver is shown in Fig. 47 for the simplest case, where all parameters are known, and the mode solver only defines the operating mode. As it can be seen, after loading the converter parameters, the convergence operating point is computed (R_{OX}). Then, based on the converter f_{sw}, the algorithm assumes an operating mode

and verifies if this assumption is correct. Essentially, an operating mode is assumed, and then several conditions are evaluated to verify if the assumed mode corresponds to the correct mode. If the assumed operating mode is correct, then the operation mode flag (OMF) becomes true, and the search is finished. Otherwise, the next possible operating mode is assumed. If, at

Figure 47 – Flowchart of the proposed mode-solver for the LLC resonant converter.



Source: Author.

the end, the operating mode is not identified, it is possible to perturb the initial guess employed in the numerical solution. Finally, if the mode is not identified, it means that the operating mode is not given by P, NP, NOP, OPO, PO, PON, or PN. There are several other operating modes at very low f_{sw}, which are given by four or even more resonant stages. However, since these modes are out of the ZVS region, they are neglected. Finally, it is important to say that the proposed mode solver, with minor modifications, can be easily adapted to the above mentioned conditions where it is necessary to disclose the LLC operating mode. Appendix G provides the access to the developed notebook in Wolfram MATHEMATICA to automatically define the operation mode.

4.8 SIMULATION AND EXPERIMENTAL RESULTS

Simulation and experimental results are presented in this section in order to assess the accuracy of the proposed TD solution. Several analyses are presented considering two LLC resonant LED driver designs operating over a wide range. A wide operating range is usual in LED drivers applications since average output current I_{LED} is controlled to achieve dimming, and the input voltage (V_{BUS}) can change as a function of the PFC stage, among other scenarios.

4.8.1 Design 1

Table 5 presents the LLC resonant LED driver parameters for *Design* 1. The converter design follows the classical procedure described in Appendix A. Analyzing Table 5, it can be seen that the converter is designed to operate with $V_{BUS} = 400\ V$ and a variable I_{LED} to

Table 5 – LLC resonant LED driver parameters: Design 1

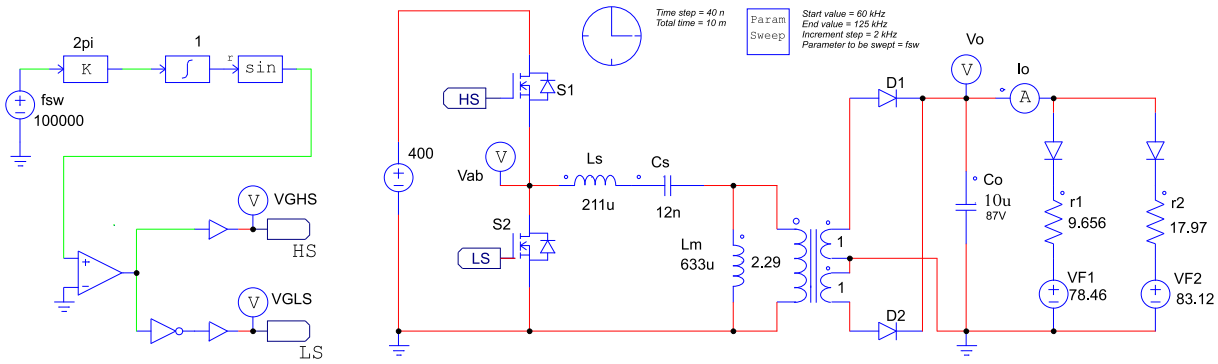
Parameter	**Designator**	**Value**
LLC LED driver design specification		
Nominal input voltage	V_{BUS}	400 V
LLC converter resonant frequency	f_o	100 kHz
Maximum LLC converter output power	P_O	100 W
Minimal LLC converter output power	$P_{O.MIN}$	≈15 W
Designed LLC LED driver resonant converter		
Average LED current range	I_{LED}	$0.2 - 1.15\ A$
Average LED voltage	V_{LED}	$80.4 - 87.3\ V$
Resonant capacitor	C_S	$12\ nF$
Resonant inductor	L_S	$211\ \mu H$
Magnetizing inductance	L_M	$633 \mu H$
Transformer turns ratio (n)	N_P/N_S	2.29
Output capacitor (Film capacitor)	C_O	$10\ \mu F$
Half-bridge switching frequency	f_{sw}	$100 - 114.2\ kHz$

Source: Author.

perform dimming at least between 100% and 20%, which correspond to the reference dimming range for outdoor applications established in (ENERGY STAR, 2019). The LED module is given by three BXRC-50C4000-F-04 devices connected in series (BRIDGELUX, 2014). The multi-branch piece-wise-linear (MBPWL) model described in Chapter 2 is employed during simulations and TD analysis. Actually, in proposed TD solution, the LED electrical behavior is emulated by two single PWL, as shown in Fig. 6.

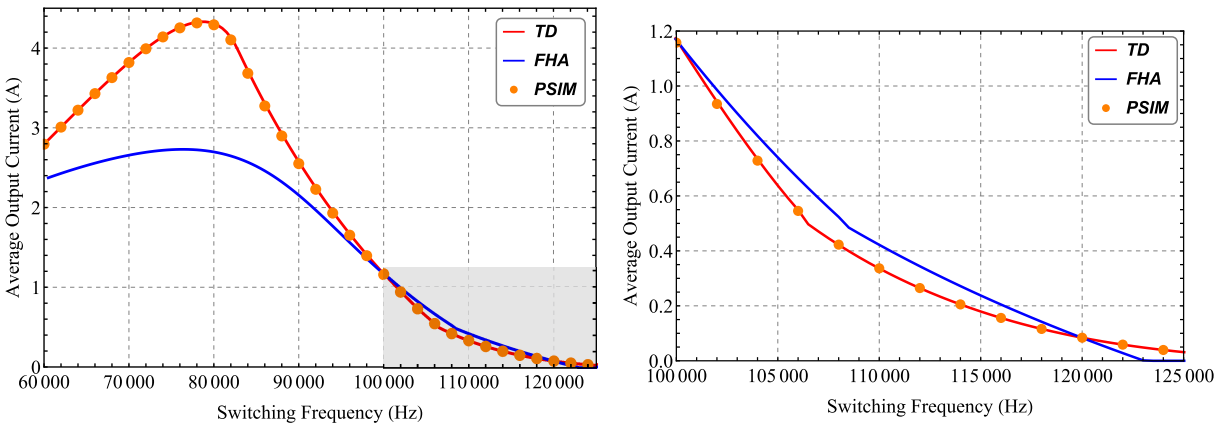
To show the feasibility of the proposed TD solution, the LLC resonant LED driver *Design 1* is analyzed employing PSIM simulation results. For the sake of clarity, Fig. 48 shows the schematic implemented in PSIM, where all the elements are ideal. To evaluate the proposed TD solution accuracy, Fig. 49 shows the LED current I_{LED} as a function of the HB inverter f_{sw} range. These curves are obtained employing the proposed TD procedure, classical FHA approach, and PSIM simulation results. Assuming PSIM results as the converter real

Figure 48 – PSIM schematic for f_{sw} dc-sweep simulation of the LLC resonant LED driver *Design 1*.



Source: Author.

Figure 49 – LLC resonant LED driver current gain obtained by PSIM simulations, classical FHA approach, and proposed time-domain solution for *Design 1*. Left-trace: From 60 kHz to 125 kHz; Right-trace: Zoom in between 100 kHz and 125 kHz.

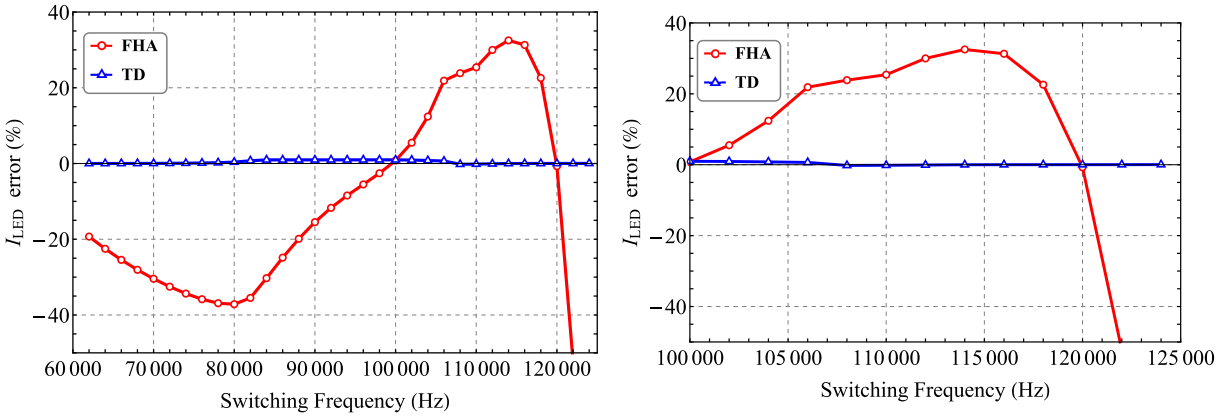


Source: Author.

behavior, it is noticed that the proposed TD approach accurately predicts I_{LED} regardless of f_{sw}. On the other hand, results from the FHA approach predict an unreal converter behavior. To further support this statement, Fig. 50 shows the relative error for both FHA and proposed TD solution in predicting I_{LED}. As can be seen, the error of the proposed TD solution is insignificant. For the FHA approach, the error is irrelevant only when f_{sw} is close to the main resonance $f_o = 100\ kHz$. Within the nominal f_{sw} range $(100 - 114.2\ kHz)$, necessary to modulate the output current, the FHA approach present errors higher than 30%.

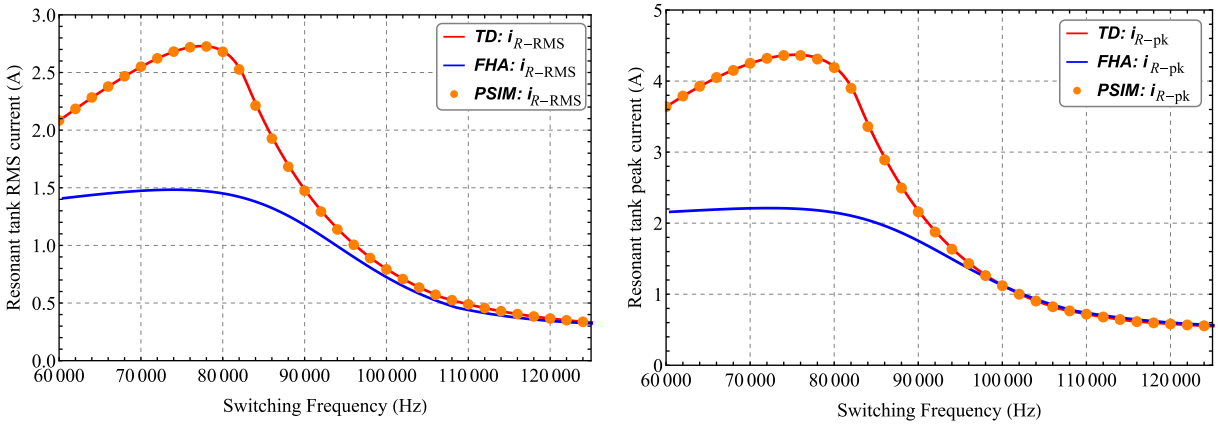
Following with the analysis, Fig. 51 shows the resonant tank RMS (i_{R-RMS}) and peak current (i_{R-pk}) obtained with PSIM simulations, classical FHA approach, and proposed TD solution. Fig. 52 shows the relative error for both FHA and proposed TD approaches in predicting the current of the resonant tank. As shown in these results, the proposed TD

Figure 50 – Comparison of the FHA and TD relative error in predicting the LLC resonant LED driver output current I_{LED} for *Design 1*.



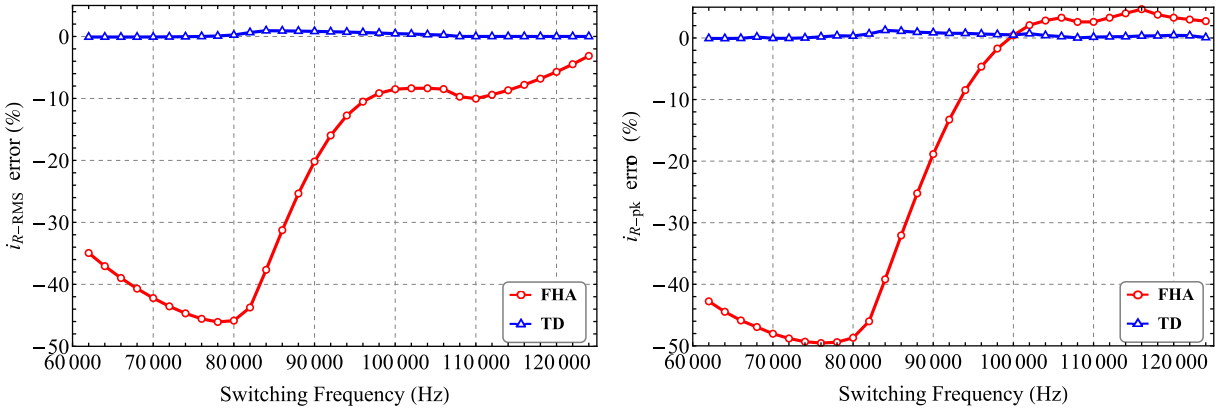
Source: Author.

Figure 51 – Resonant tank current obtained with PSIM simulation, classical FHA approach, and proposed time-domain solution for *Design 1*; Left-trace: i_{R-RMS}; Right-trace: i_{R-pk}.



Source: Author.

Figure 52 – Comparison of FHA and TD relative error in predicting the resonant tank current for *Design 1*; Left-trace: i_{R-RMS}; Right-trace: i_{R-pk}.

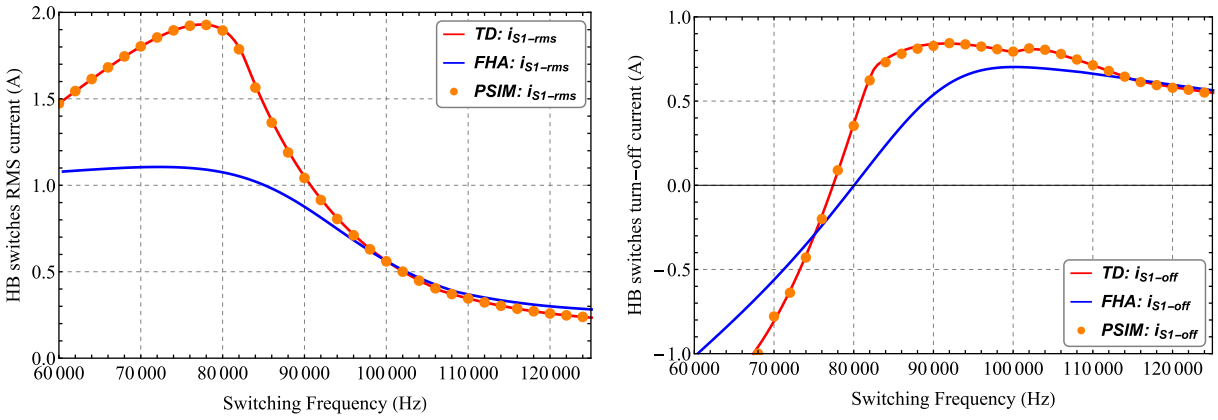


Source: Author.

solution presents outstanding accuracy in predicting i_{R-RMS} and i_{R-pk}. On the other hand, considering the converter nominal operating range, the FHA approach's percent error is less than 10%. However, for conditions beyond the nominal range, the percent error increases significantly.

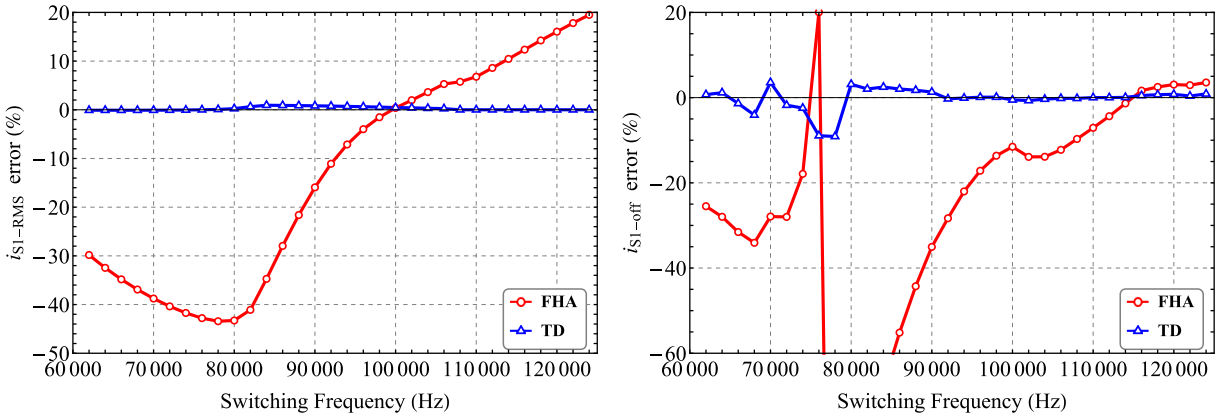
Fig. 53 shows the results for the HB switches RMS ($i_{S1-RMS} = i_{S2-RMS}$) and turn-off ($i_{S1-off} = i_{S2-off}$) currents. The relative error in predicting these currents for both FHA and TD approaches is shown in Fig. 54. As can be seen, the FHA approach presents an unacceptable error in predicting i_{S1-RMS} since it achieves values greater than 10% within the nominal range. Regarding i_{S1-off} prediction, TD results present a slight deviation around the peak gain frequency. However, for the nominal f_{sw} range, the percent error is insignificant. The increased error in prediction i_{S1-off} employing both FHA and TD analysis, occurs around

Figure 53 – HB switches current obtained with PSIM simulation, classical FHA approach, and proposed TD solution for *Design 1*; Left-trace: i_{S1-RMS}; Right-trace: i_{S1-off}.



Source: Author.

Figure 54 – Comparison of FHA and TD relative error in predicting the HB switches current for *Design 1*; Left-trace: i_{S1-RMS}; Right-trace: i_{S1-off}.



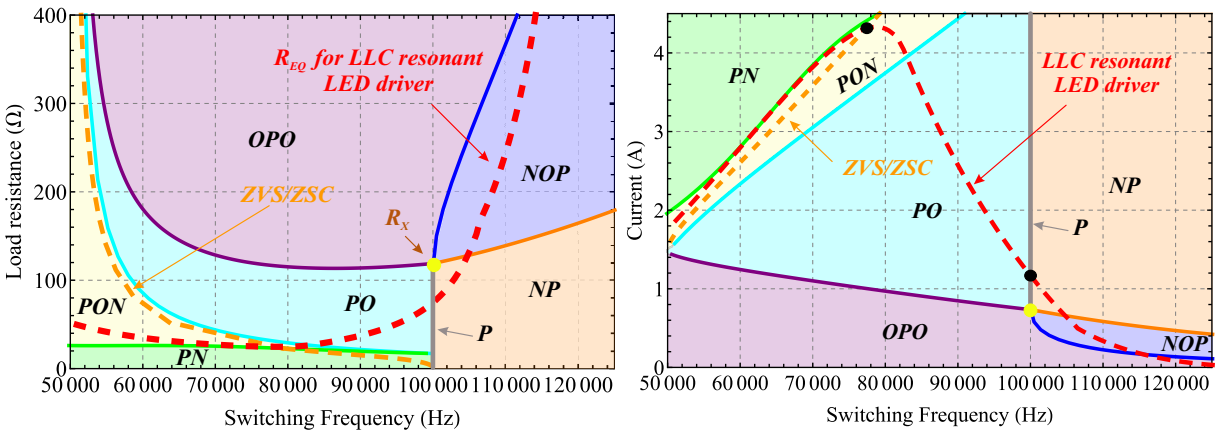
Source: Author.

the point where i_{S1-off} is close to zero. So, any slight error outcome in high relative value.

Besides the quantitative analysis, the converter operation mode map and waveforms examination is an interesting tool that provides further insights. Fig. 55 shows the operating mode map for the LLC resonant LED driver *Design 1*. The red dotted line corresponds to the results from Design 1 current gain analysis. In the right-trace of Fig. 55, the operating mode map is given for I_{LED} instead of the equivalent load resistance. So, the LLC current gain curve is merged to the operating mode map. In the left-trace, the current gain curve is translated to the LED module equivalent resistance variation and merged with the operating mode map.

Employing the proposed TD solution, the resonant tank current i_R, transformer magnetizing current i_M, transformer primary current i_P, output rectified current $i_{D1} + i_{D2}$ and

Figure 55 – LLC resonant LED driver operation modes map for *Design 1*. Left-trace: Delimited by equivalent resistance; Right-trace: Delimited by I_{LED}.

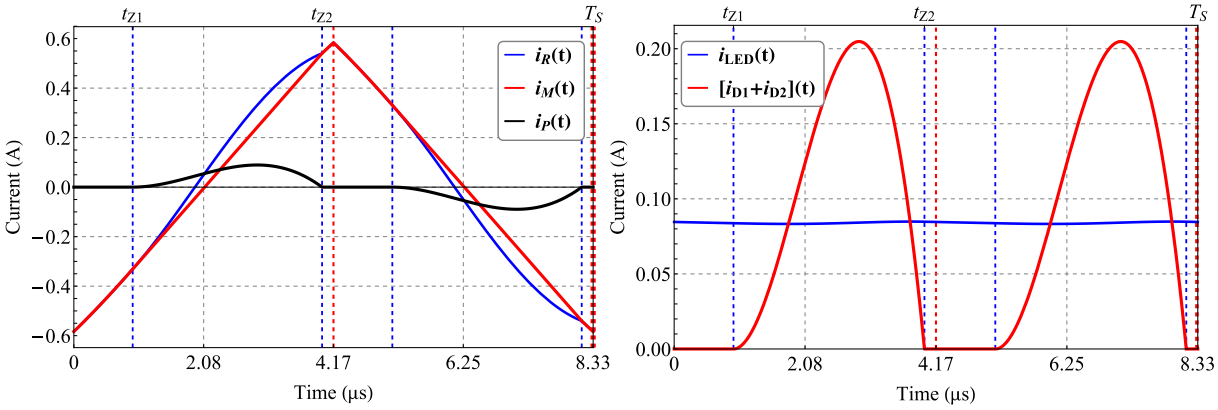


Source: Author.

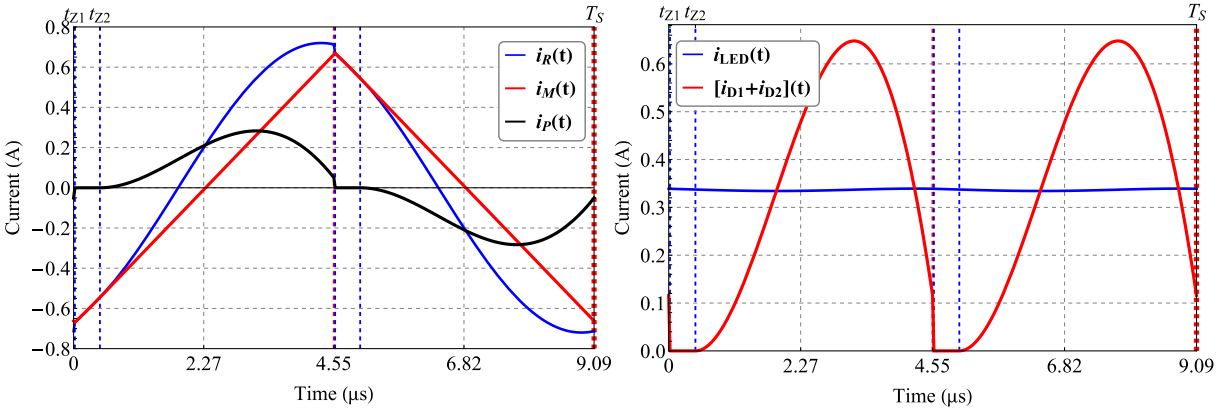
LED current i_{LED} waveforms are plotted for several operating points, above and below f_o. Fig. 56 shows the mentioned waveforms for the operation above f_o. Fig. 56.a shows the waveforms for $f_{sw} = 120\ kHz$, where I_{LED} is around 84 mA, and the operation mode is OPO.

Figure 56 – Predicted TD behavior of the LLC employing the proposed TD solution - $f_{sw} > f_o$.

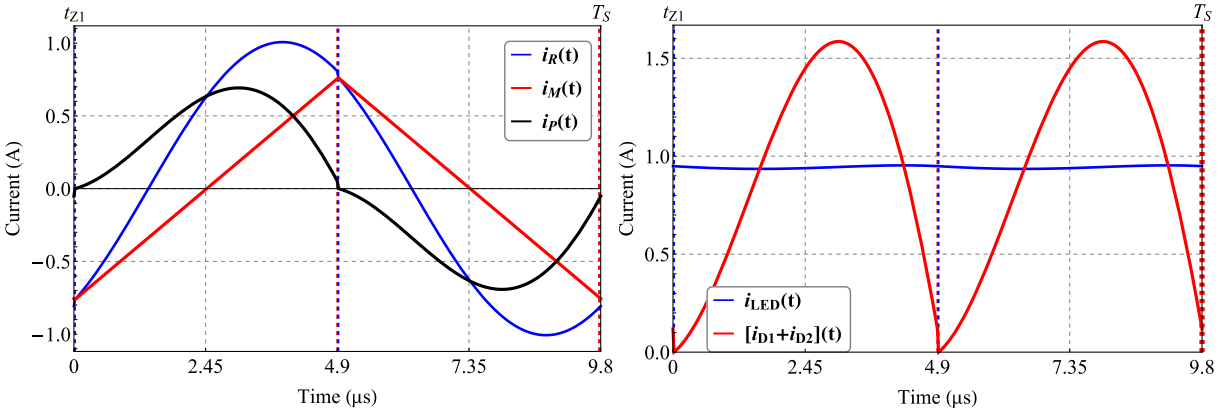
(a) – OPO mode: $f_{sw} = 120\ kHz$, $I_O = 0.084\ A$, $t_{Z1} = 944.3\ ns$, $t_{Z2} = 3.98\ \mu s$.



(b) – NOP mode: $f_{sw} = 110\ kHz$, $I_O = 0.336\ A$, $t_{Z1} = 22.4\ ns$, $t_{Z2} = 460\ ns$.



(c) – NP mode: $f_{sw} = 102\ kHz$, $I_O = 0.943\ A$, $t_{Z1} = 19.83\ ns$.

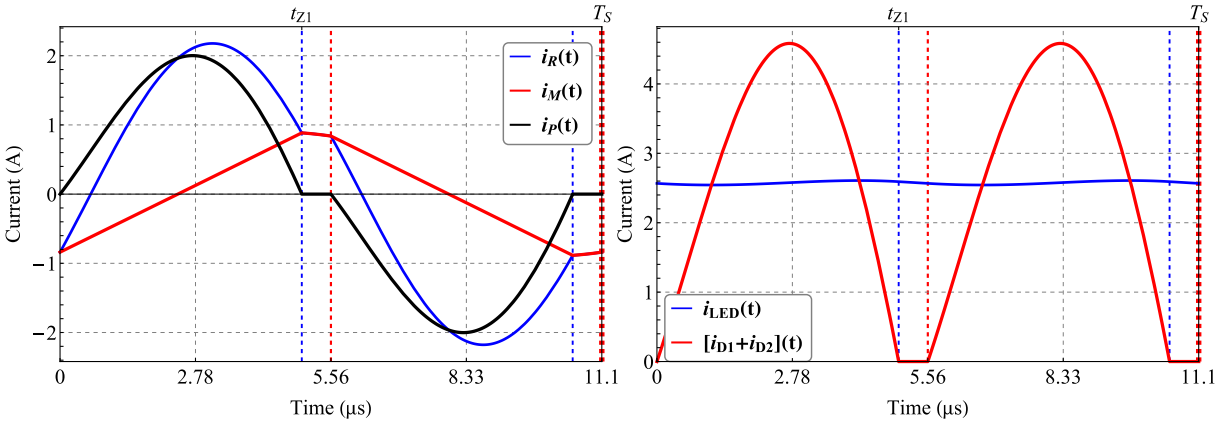


Source: Author.

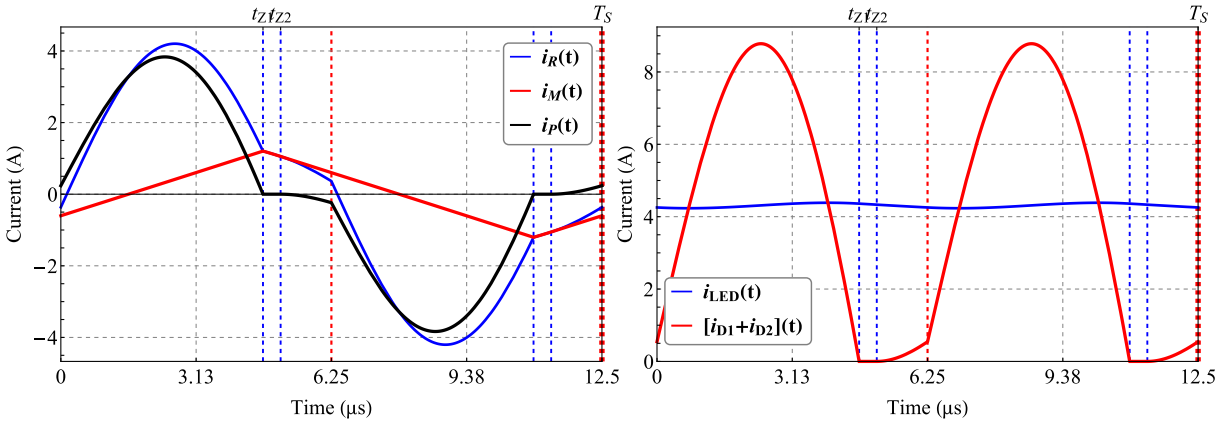
As f_{sw} decrease, becoming closer to f_o, the LED current increases, so the operation modes change from NOP (Fig. 56.b) to NP mode (Fig. 56.c), reducing the time where no energy

Figure 57 – Predicted TD behavior of the LLC employing the proposed TD solution - $f_{sw} < f_o$.

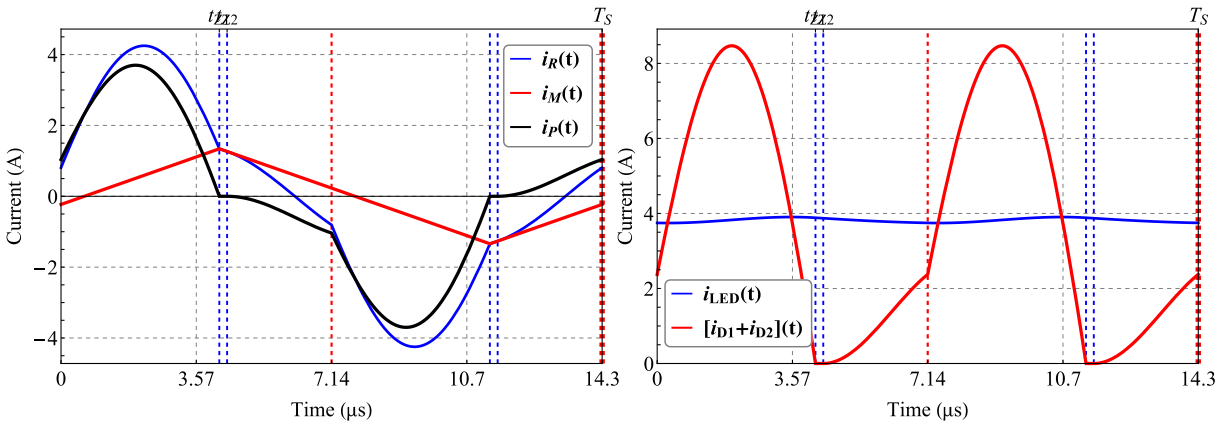
(a) – P0 mode: $f_{sw} = 90\ kHz$, $I_O = 2.57\ A$, $t_{Z1} = 4.96\ \mu s$.



(b) – PON mode: $f_{sw} = 80\ kHz$, $I_O = 4.31\ A$, $t_{Z1} = 4.67\ \mu s$, $t_{Z2} = 5.08\ \mu s$.



(c) – PON mode: $f_{sw} = 70\ kHz$, $I_O = 3.82\ A$, $t_{Z1} = 4.18\ \mu s$, $t_{Z2} = 4.38\ \mu s$.



Source: Author.

is transferred to the secondary side. For the OPO mode (see Fig. 56.a), the output rectifier achieves ZCS, and being i_R between $0 - T_S/2$ equal the current in switch S_1, it is possible to infer that the HB switches operate with ZVS. Analyzing NOP and NP mode, respectively in Fig. 56.b and Fig. 56.c, even achieving ZVS condition for the HB switches, the diodes in the output rectifier lose the ZCS condition.

Similarly, Fig. 57 shows the waveforms for the operation below f_o. In the same way, the switching conditions can be easily assessed. Furthermore, it can be seen that the PON mode occurs above and below the peak gain frequency ($\approx 78\ kHz$), from where it can be inferred that the peak gain occurs at PON mode.

At this point, analyzing Fig. 55, it can be seen that the operating mode map correctly predicts the LLC resonant LED driver operation mode, which is visualized in the time domain in Fig. 56 and Fig. 57.

Based on the analysis presented up to this point, regardless the f_{sw}, it can be noticed a high accuracy for the predicted behavior when the proposed TD solution procedure is employed. However, to further assesses the feasibility of the proposed solution, in the next section a different resonant tank is analyzed employing experimental results.

4.8.2 Design 2

The *design 2* follows the procedure described in the next chapter, previously reported in (MENKE, DURANTI ET AL., 2020). The LLC resonant LED driver parameters of the second design are presented in Table 6. For this design, experimental results are also provided. The

Table 6 – LLC resonant LED driver parameters: *Design 2*

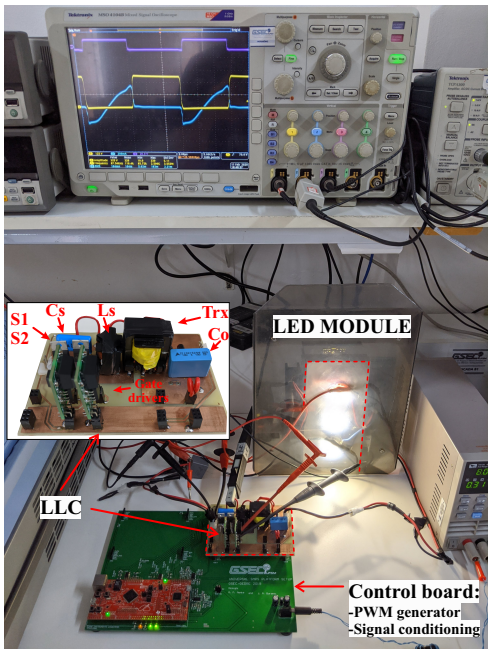
Parameter	**Designator**	**Value**
LLC LED driver design specification		
Nominal input voltage	V_{IN}	$400\ V$
Input voltage range	V_{IN}	$320 - 420\ V$
LLC converter resonant frequency	f_o	$100\ kHz$
Maximum LLC converter output power	P_O	$100\ W$
Minimal LLC converter output power	$P_{O.MIN}$	≈15 W
Designed LLC LED driver resonant converter		
Average LED current range	I_{LED}	$0.25 - 1.15\ A$
Average LED voltage	V_{LED}	$80.9 - 87.3\ V$
Resonant capacitor	C_S	$6.8\ nF$
Resonant inductor EE 25/10/05; 30 turns; 2#AWG27	L_S	$372\ \mu H$
Magnetizing inductance	L_M	$1117 \mu H$
Transformer turns ratio (n) EE 30/15/14; $n_P = 39$ (2#AWG27); $n_S = 17$ (3#AWG27)	N_P/N_S	2.29
Output capacitor (Film capacitor)	C_O	$10\ \mu F$
Half-bridge switching frequency	f_{sw}	$86.7 - 106.3\ kHz$

Source: Author.

prototype setup is shown in Fig. 58. Further details of the Setup are found in Appendix E. In this second design, besides output current variation to perform dimming, the LLC is subjected to a wide input voltage (V_{IN}) range.

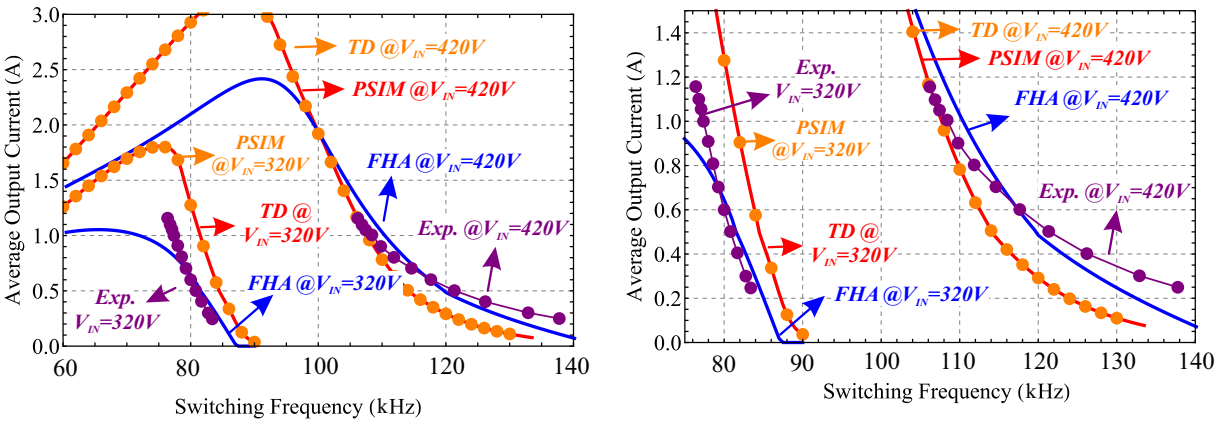
Fig. 59 shows LED current as a function of f_{sw}, wherein experimental, PSIM, TD and FHA results are presented for $V_{IN} = 320\ V$ and $V_{IN} = 420\ V$. As can be seen, TD and PSIM results are interchangeable. In addition, comparing experimental and TD results for $V_{IN} = 320\ V$, there is a difference between the results given by an almost constant value, which

Figure 58 – LLC resonant LED driver experimental setup for *Design 2*.



Source: Author.

Figure 59 – LLC resonant LED driver current gain obtained with PSIM simulations, classical FHA approach, proposed TD solution procedure, and Experimental Result for *Design 2*. Left-trace: From 60 kHz to 140 kHz; Right-trace: Zooom in between 75 kHz and 140 kHz.



Source: Author.

shifts the curves. However, both experimental and TD curves present the same inclination, which cannot be observed in the results predicted by the FHA approach. On the other hand, for $V_{IN} = 420\ V$, the experimental curve has its shape deviated from the predicted one by TD and FHA analyses. These errors between experimental and TD-based results are given by parasitic components, neglected in the TD analysis, as well as the influence of the elements tolerance.

Employing the proposed TD analysis, Table 7 presented the predicted operation mode and required f_{sw} to obtain the specific I_{LED} when operating at different input voltages. As can be seen, for *design 2*, PO and OPO modes dominate the converter at $V_{IN} = 320\ V$, which means that the LLC is running below the main resonance and imply in ZCS for the output rectifier. For $V_{IN} = 420\ V$, NOP and NP modes predominate. For these modes, diode ZCS is lost. This analysis is only possible under the TD analysis by inspecting the operation mode. The information that the operation is above the resonance is not enough since OPO can also occur in this condition, so achieving ZCS for output rectifier.

Besides the quantified current levels evaluation, a powerful tool corresponds to waveform assessments, which provide further insights into the converter, revealing its operation mode and switches and diodes commutation characteristics (ZVS and ZCS). In this context, Fig. 60 shows the theoretically predicted waveform of the LLC LED driver compared to the experimental measurement for the operation at $V_{IN} = 320\ V$ with nominal and minimum I_{LED}. As it can be seen, the predicted waveforms are similar to the measured waveforms. In this case, the operation mode is easily identified.

For the case where $V_{IN} = 420\ V$, the waveforms are shown in Fig. 61. The predicted waveforms are similar to the experimental ones. However, the transition times are not easily identified in the experimental results due to the small value. Moreover, due to the operation above the resonance, parasitic components strongly affect the current waveforms, which impair the experimental identification of the transition times.

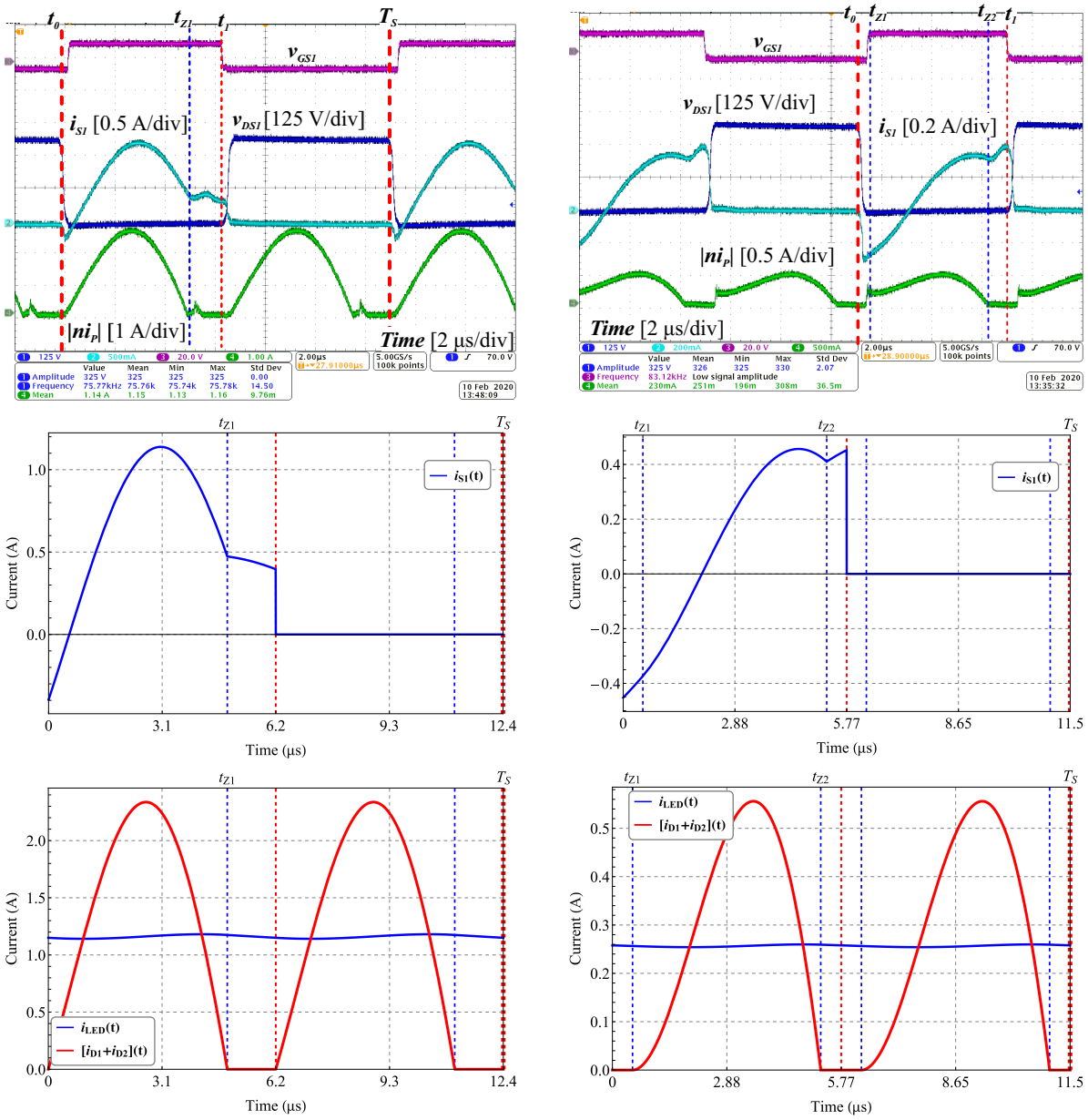
At this point, it is worthy of mentioning that results from simulation software like PSIM are accepted to be very accurate and can be easily employed to get the converter

Table 7 – Operation modes and f_{sw} for the LLC resonant converter *Design 2*.

I_O	$V_{IN} = 320\ V$		$V_{IN} = 420\ V$	
	Mode	$f_{sw}\ (kHz)$	Mode	$f_{sw}\ (kHz)$
0.25	OPO	86.7	NOP	121.6
0.35	OPO	85.8	NP	118.1
0.45	PO	84.9	NP	115.3
0.55	PO	84.2	NP	113.4
0.65	PO	83.7	NP	119.0
0.75	PO	82.9	NP	110.6
0.80	PO	82.6	NP	109.9
0.95	PO	81.7	NP	108.3
1.15	PO	80.7	NP	106.3

Source: Author.

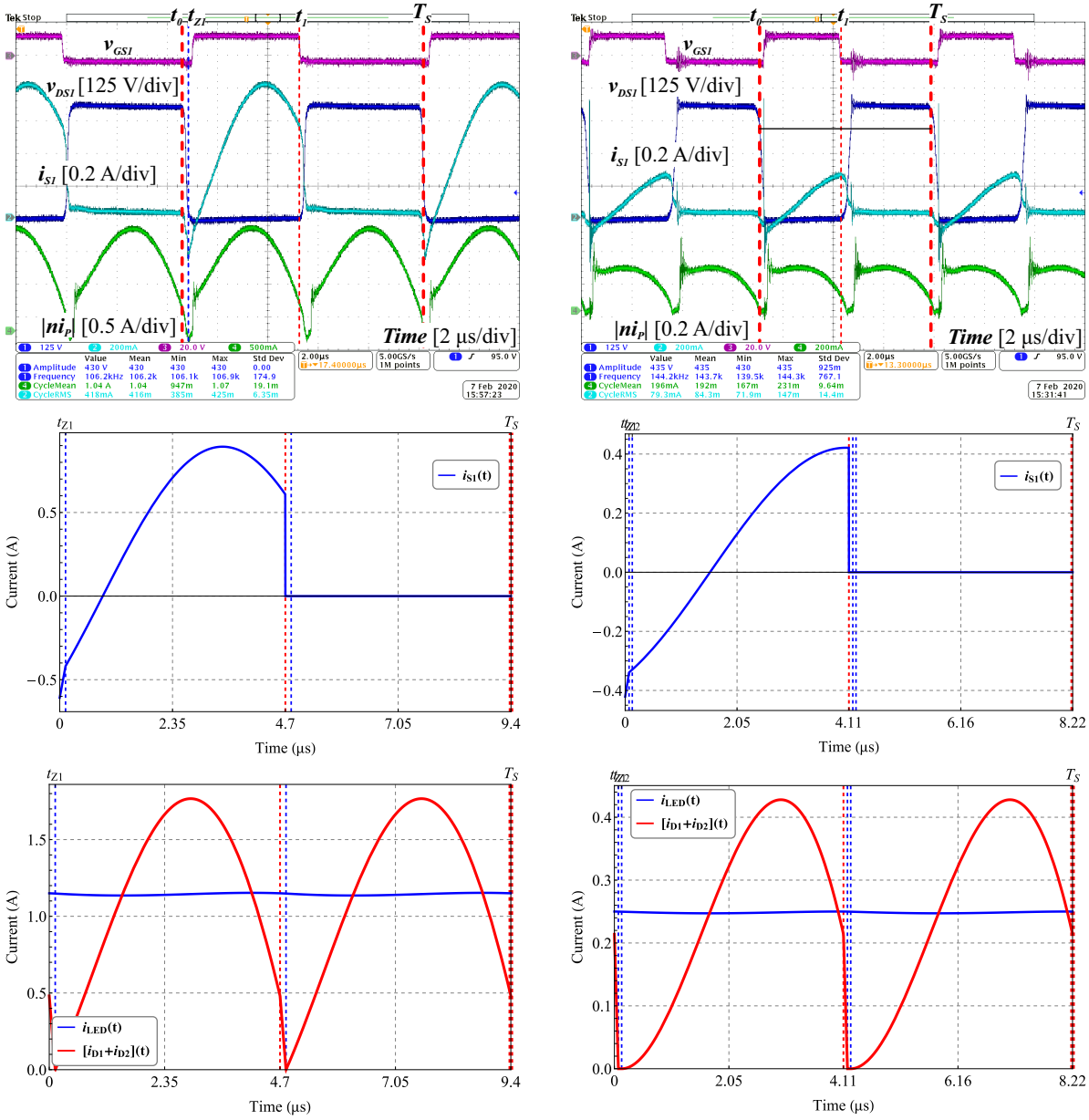
Figure 60 – LLC resonant LED driver main waveforms comparison between predicted TD results and experimental measurements for $V_{IN} = 320\,V$. Top-Left: Experimental result at nominal LED current; Middle-left and Bottom-left: TD predicted waveforms at nominal LED current; Top-right: Experimental result at minimum LED current; Middle-Right and Bottom-Right: TD predicted waveforms at minimum LED current.



Source: Author.

waveform. However, to obtain the simulation results, it is required to numerically solve the ODE with a given initial condition from period to period and update the initial conditions at the beginning of each period until they reach the steady state condition, which demands cumbersome numerical methods and are inconvenient once usually the main interest is the steady-state operation. Unlike, the proposed TD procedure relies on the steady-state operation outcoming in results as accurate as PSIM without the expense of transient period computation.

Figure 61 – LLC resonant LED driver main waveforms comparison between predicted TD results and experimental measurements for $V_{IN} = 420\,V$. Top-Left: Experimental result at nominal LED current; Middle-left and Bottom-left: TD predicted waveforms at nominal LED current; Top-right: Experimental result at minimum LED current; Middle-Right and Bottom-Right: TD predicted waveforms at minimum LED current.



Source: Author.

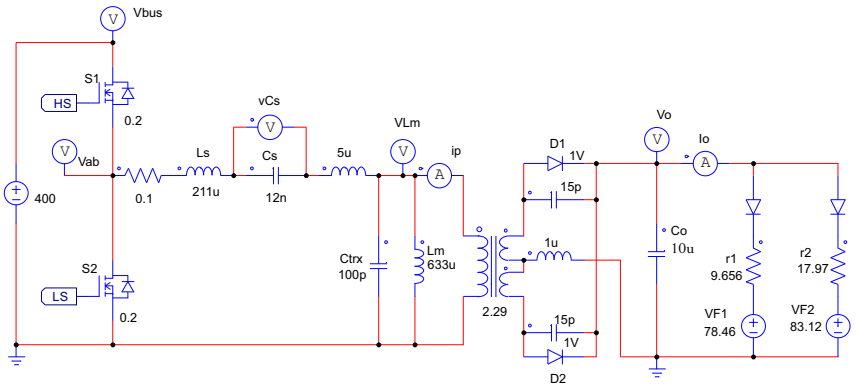
Furthermore, once the converter is solved in a mathematical environment, several analyses can be developed, going from the exhaustive converter analysis to an optimized converter design procedure.

4.8.3 LLC parasitic components influence

To better understand the parasitic components' influence in the LLC resonant LED driver current gain, simulation results are systemically developed. Fig. 62 shows the schematic of the LLC resonant LED driver employed in PSIM to perform this analysis. In this circuit, several parasitic elements are added to the idealized circuit. Dead-time and HB switches output capacitance are not included in this analysis. Design 1 is employed in this analysis.

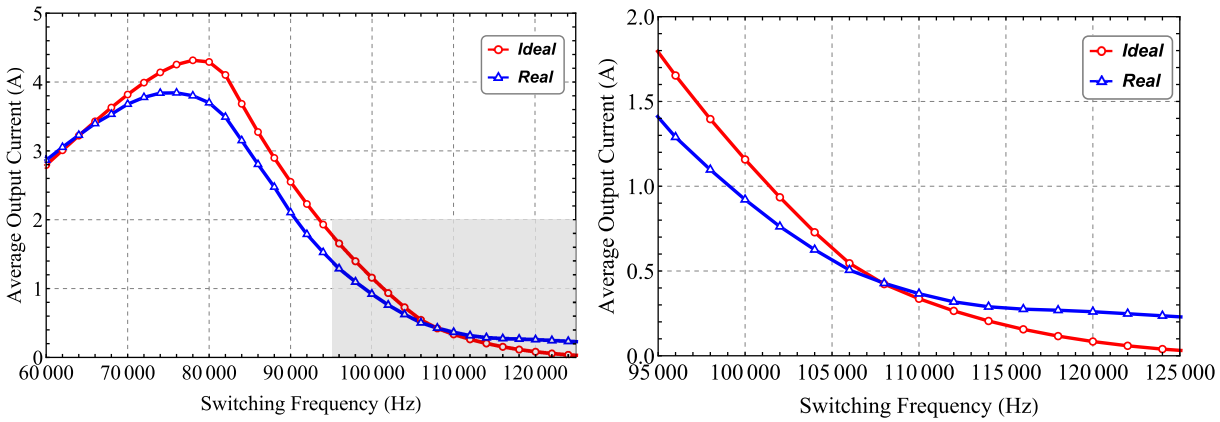
Fig. 63 shows the current gain for the ideal case and for the condition where the parasitic elements are considered, named as Real. For almost the entire range, as expected, the real output current is lower than for the ideal case once there are losses and voltage drops over the circuit. However, when f_{sw} increases, this behavior changes, where the output current for the real case is higher than the ideal one. The same observation was done in (B. H. LEE ET AL., 2009), wherein this behavior is associated with the parasitic capacitance in the circuit.

Figure 62 – LLC resonant LED driver schematic with parasitic elements for simulation purpose.



Source: Author.

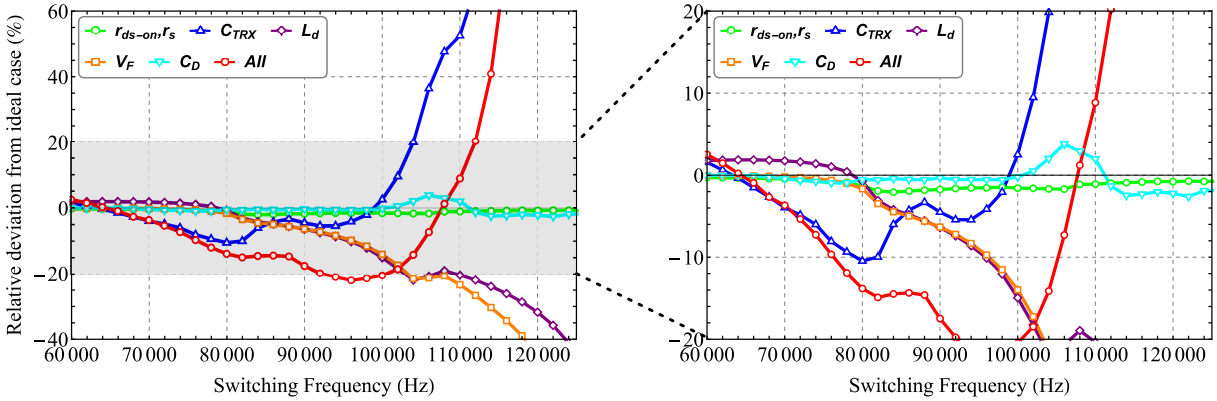
Figure 63 – LLC resonant LED driver Design 1 current gain for the ideal converter compared to the case where parasitic elements are taken into account.



Source: Author.

In this way, to assess the impact of every single parasitic element, the current gain curve is obtained considering in each curve only one parasitic element. In the sequence, the deviation from the ideal case is computed. These results are shown in Fig. 64. As can be seen, the three elements that mainly impact the converter are the transformer leakage inductance L_d, output rectifier diode forward voltage V_F, and transformer intra-winding capacitance C_{TRX}. Therefore, to achieve an improved TD solution, it is necessary to consider the parasitic converter elements, being this analysis suggested as the future developments of this thesis.

Figure 64 – Analysis of the impact of the parasitic elements in the output current of the LLC resonant LED driver.



Source: Author.

4.9 SUMMARY

This chapter presented the proposed TD analysis for the LLC resonant LED driver, derived from the system state-space representation direct TD solution. Therefore, the LLC converter was analyzed as a piece-wise linear system, where each linear system corresponds to a resonant stage. In the sequence, the LLC operating modes, successive occurrence of the resonant stages, are analyzed. To obtain the converter TD solution, the state-vector initial conditions and converter transition times are initially computed throughout a system of equations solved numerically. In the sequence, a piece-wise equation is defined by merging the resonant stages in different sequences as a function of the operating mode.

In comparison to the FHA approach, outstanding accuracy is achieved employing the proposed TD solution procedure. Compared to the preceding TD analysis, the proposed solution presents extended flexibility. It can be easily applied to even more complex systems without requiring the analytical solution of differential equations. Actually, numerical solutions are employed to solve the equations that describe the converter operation. Nevertheless, the procedure based on the state-space representation direct TD solution is not very friendly. On the other hand, with the disclosed procedure, its potentialities are eminent

and could be employed to analyze any power converter very precisely, mainly to develop an optimized design procedure.

Beyond the converter's TD solution, the proposed mode solver algorithm develops a fundamental task inside the TD analysis. The mode solver allows the development of further analyses, for instance, the current gain curve computation. On the other hand, the proposed operating mode mapping also demonstrates to be an impressive tool. With the operating mode map, it is possible to see the converter operating mode in advance. So, one can infer, for instance, if the converter operates with ZVS and ZCS conditions.

Regarding the LLC resonant LED driver TD behavior, even achieving accurate results with the proposed solution, it is noticed that parasitic components, neglected in the analysis, strongly impact the converter voltage and current levels. Therefore, new analyses are required where the parasitic components of the converter have to be taken into account. Besides, the developed solution employs real converter parameters, which is a drawback in comparison to normalized analysis where generic analysis can be developed.

5 LLC LED DRIVER DESIGN

In this chapter, a new design procedure for the LLC resonant LED driver is proposed. This design procedure relies on the estimated converter efficiency, which is computed, taking into account the converter current and voltages levels predicted by the proposed TD analysis. However, as usual in offline LED drivers, the dc/dc stage will be submitted to input voltage variations and different load conditions. Therefore, to contemplate this universe of operating points, the design procedure is guided by the weighted-average-efficiency concept. Besides, different constraints and approaches are assessed to ensure zero voltage switching (ZVS), zero current switching (ZCS), enough power gain, and practical switching frequency range over a wide operating window. Experimental results show the feasibility of the proposed design procedure.[1]

5.1 INTRODUCTION

A well-designed LLC resonant LED driver converter ensure ZVS for the HB switches, ZCS for the output rectifier, feasible switching frequency range Δf_{sw}, and enough gain peak to keep under control the output current I_{LED} over the whole operating window while maintaining a good efficiency without compromising the converter power density. Besides, the design procedure must be reliable, which means that the real behavior of the converter must be taken into account.

Regardless of the LLC resonant converter application, the usually employed design methodology is based on the FHA analysis. In this procedure, to achieve ZVS, ZCS, enough gain peak, and practical Δf_{sw}, solely the converter gain curves are analyzed. To improve the converter efficiency, some procedures assess the resonant components' influence on the current levels, where the LC components that result in the lowest resonant and switches current levels for the nominal operating point are selected. Nevertheless, even being a simple and widely employed design procedure, several issues do not allow a reliable and well-designed converter. These issues are related to the FHA lack of accuracy, assessment of only the gain curves, and focus at the nominal operating point. Besides, converter power density is seldom directly evaluated.

Therefore, to overcome these drawbacks for the LLC applied to power an LED load, a

[1] Portions of this chapter have been published in (MENKE, DURANTI ET AL., 2020).

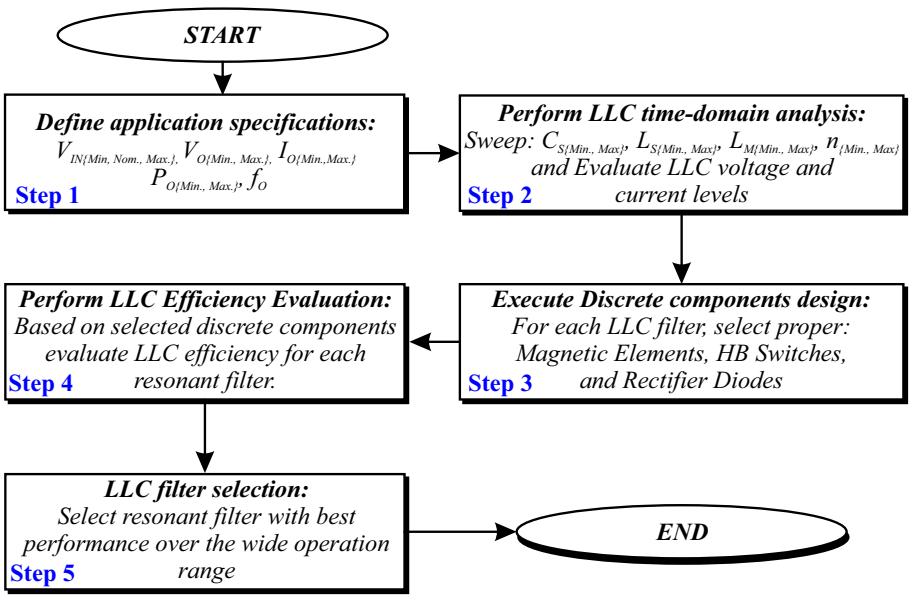
new design procedure is proposed considering the wide operating range of the converter, where instead of current and voltage levels, the estimated converter efficiency is used to guide the design. Nevertheless, to consider the converter efficiency under different operating points, instead of only the nominal conditions, a figure of merit based on the weighted average efficiency is employed, which considers in its definition the efficiency at different loads and operation cases that the converter will be submitted. Different operation cases are understood as the variation of input voltage and load configuration or the combination of both. Besides, to ensure ZVS, enough current gain, and feasible Δf_{sw}, the design is supported by constraints that add these features to the final converter designed. Besides, the converter's power density is also assessed before concluding the design with the resonant tank parameters definitions. Last but not least, to outcome with a reliable and well-designed converter, the proposed state-space-based TD procedure is employed, which guarantees that current and voltage levels in the LLC resonant LED driver converter are considered with high accuracy.

The remaining of this chapter presents in detail the proposed design procedure, being a design example shown in the sequence. Finally, in order to show the feasibility of the proposed design procedure, experimental results are presented.

5.2 LLC RESONANT LED DRIVER DESIGN PROPOSAL

Fig. 65 shows the proposed design procedure algorithm flowchart, whose steps are described as follows.

Figure 65 – LLC resonant LED driver proposed design procedure algorithm flowchart.



Source: Author.

5.2.1 Step 1: Electrical specifications of the application

The design procedure starts by defining the specifications that delimit the LLC resonant LED driver operating range. In this way, the input voltage $V_{IN} = V_{BUS}$, output voltage $V_O = V_{LED}$, output current $I_O = I_{LED}$ and output power P_O range $\{min, max\}$ are defined. Furthermore, the main resonant frequency (f_o) of the system has to be determined. From a general point of view, Step 1 consists of design input parameters knowledge.

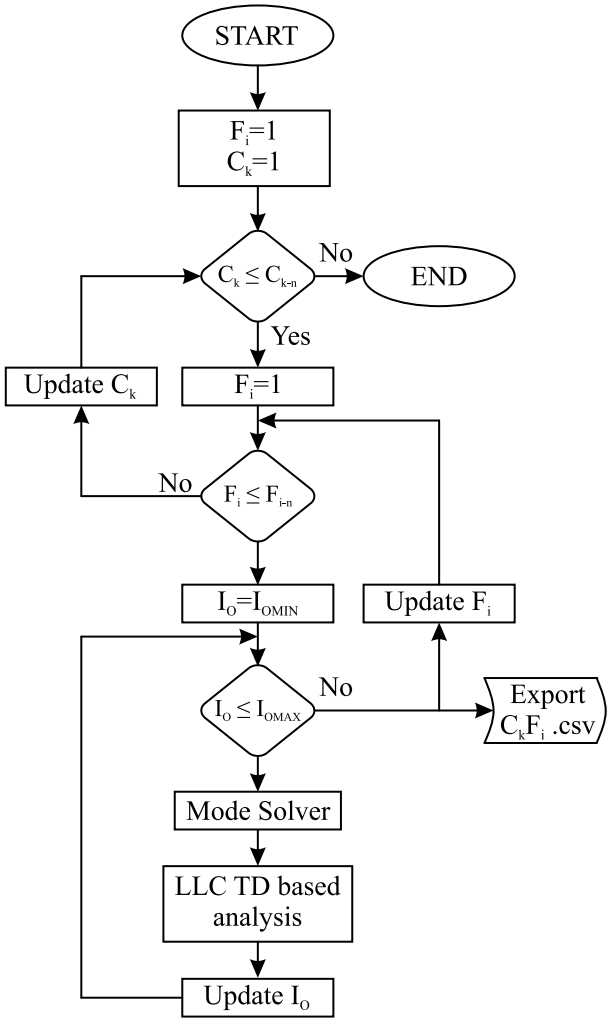
5.2.2 Step 2: LLC TD based analysis

Considering a set of resonant tank elements (C_S, L_S, L_M, n), the second step of the design procedure accurately analyzes each LLC filter from the set in the TD employing the state-space based solution proposed in the previous chapter. Therefore, the algorithm sketched in Fig. 66 is implemented. In which, from the application specifications, the combinations of V_{IN} and V_O defines different operation cases (C_1, C_2,..., C_k), and the possible combinations among L_S, C_S, n, L_M define different LLC filters (F_1, F_2,..., F_n). Finally, for each case C_k the same set of resonant tanks F_i is evaluated considering the load variation ($I_{OMIN} - I_{OMAX}$). Analyzing Fig. 66, it can be seen that for each filter, case, and load condition, the LLC mode-solver is employed to predict the converter operation mode (PN, PON, PO, P, OPO, NOP, or NP). Afterward, the current and voltage levels in the main LLC elements are calculated employing the TD analysis.

Gathering the outcomes over load sweep for each filter F_i and operating case C_k, an array of data is exported, which is used by the next design procedure step. To maintain clarity, each array carries in its variable name the information of the current case and filter evaluated. For example, $C1F1$ stands for "Case 1"and "Filter 1", and so on for all cases (C_k) and filters (F_i) analyzed. Each row of this array correspond to a specific output current I_O, and the columns bring the related V_{IN}, V_O, f_{sw}, R_L, C_S, L_S, L_M, resonant RMS ($i_{R.rms}$) and peak ($i_{R.pk}$) current, RMS C_S voltage ($v_{Cs.rms}$), peak C_S voltage ($v_{Cs.pk}$), HB switches RMS ($i_{S1.rms}$) and turn-off ($i_{S1.off}$) current, secondary RMS current ($i_{Sec.rms}$), rectifier average current ($i_{D1.avg}$), and resonant filter input current phase expressed in the time domain as the HB duty-cycle window t_{Dwin}.

Summarizing the second step, it performs the TD analysis of several LLC filters sweeping over different output currents and input voltage. The set of resonant filters employed under this analysis can be defined taking as reference the filter F_i designed by the classical FHA approach. Then, making variations in each component of the LLC around this reference design, yields in a set of several LLC filters. From this set of filters, the most prominent one will be selected at the end of the design procedure.

Figure 66 – LLC Design procedure step 2 flowchart.



Source: Author.

5.2.3 Step 3: Discrete components design

The data generated by step 2 are now employed to design the proper semiconductors and magnetic elements for each filter F_i. In this way, for each F_i filter evaluated, the critical operation point is identified among all the operating cases (C_k) that this filter would be submitted if employed. The critical operation point corresponds to the condition where the highest current and voltages levels are noted. In sequence, the critical operating point condition is employed to select the semiconductor and design the magnetic elements for each filter. With the critical operating condition identified for each filter F_i, the magnetic elements (series inductor and transformer) are designed following the area product procedure. Power semiconductor devices are selected to withstand the estimated voltage and current stress. For further details, Appendix C presents the procedure employed to design the discrete components.

Designing the proper magnetic elements for each evaluated filter F_i allows a fair comparison, which differs from the methodologies that first define the magnetic element size employed and then design the resonant tank. It is worth mentioning that the magnetic element size impacts the converter power losses and power density; therefore, the proper magnetic elements selection for each filter, besides a fair comparison, could bring the converter to higher efficiency and power density.

5.2.4 Step 4: LLC power losses and efficiency computation

At this point, current and voltage levels for each F_i, operating overall C_k with a variable load, are known and available on the $C_kF_i.csv$ file (Step 2 result), as well as the employed semiconductors and magnetic elements in each F_i (Step 3 result), which allows the converter efficiency to be estimated (Step 4 duty). Hence, the converter power losses are calculated for each filter F_i operating with a variable load under all the cases C_k considered. With the losses calculated, the efficiency is estimated by (5.1). The procedure employed to estimate the LLC power losses is described in Appendix D. Auxiliary voltage sources, and gate-driver power losses are neglected. Besides, the power loss model assumes that the HB operates under ZVS. Thus, HB switching losses are given only by the turn-off losses.

$$\eta = \frac{\text{Output Power}}{\text{Power Losses} + \text{Output Power}} \tag{5.1}$$

5.2.5 Step 5: LLC resonant filter F_i selection

The final step of the proposed design procedure aims to select one LLC filter among the several LLC filters F_i evaluated. Unlike the conventional approaches where the resonant tank elements are designed based only on gain curves and current levels, the proposed design relies on several analyses that come out with a reliable and well-designed converter.

5.2.5.1 Peak gain evaluation

The first step inside the LLC resonant filter selection deals with the peak gain analysis. Thus, the filter F_i whose peak gain is not enough to supply the load over the specified operating range is excluded from the set of the possible solution. This task is done by evaluating $C_kF_i.csv$ for each filter and checking if the maximum output power/current is reached under all operating cases.

5.2.5.2 Efficiency evaluation

Since the converter is submitted to a wide operating range considering input and output voltage and current variation, a metric related to the average efficiency is proposed to compare different filter performances. In this way, for each LLC filter F_i considering the operation at a specific output power (P_j), the average efficiency ($\langle\eta\rangle_{@P_j}$) is calculated among the assessed operating cases C_k, given by (5.2).

$$\langle\eta\rangle_{@P_j} = \frac{1}{k}\sum_{C_1}^{C_k}\eta_{C_k@P_j} \tag{5.2}$$

Considering that the converter operates with variable output power, the average efficiency calculated by (5.2) does not outcome in a single efficiency performance index for each filter. Therefore, to rank the LLC filters efficiency performance, the evaluated $\langle\eta\rangle_{@P_j}$ is summed with different weights. The weight employed is a function of the output power (P_j) related to the nominal one (P_{Nom}). Finally, this summation is normalized by the summation of the weights. The normalized efficiency rank ($\langle\eta_{rank}\rangle$) index is then numerically determined by (5.3), which correspond to a dimensionless value for each filter, closely related to its efficiency.

$$\langle\eta_{rank}\rangle = \frac{\sum_{P_1}^{P_j}\left[\left(\frac{1}{k}\sum_{C_1}^{C_k}\eta_{C_k@P_j}\right)\frac{P_j}{P_{Nom}}\right]}{\sum_{P_1}^{P_j}\left[\frac{P_j}{P_{Nom}}\right]} \tag{5.3}$$

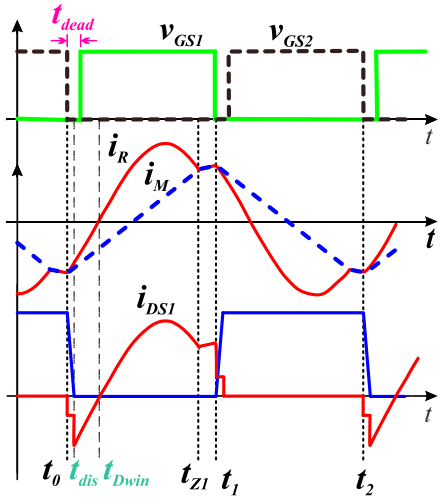
As can be noted, this step does not exclude any filter from the possible solution. Instead, it allows to sort the filters by $\langle\eta_{rank}\rangle$.

5.2.5.3 ZVS constraint

This step evaluates the ZVS condition, a mandatory constraint that must be accomplished throughout the whole converter operating range. Therefore, if one LLC filter from the set does not fill this requirement, it will be excluded from the set of possible solutions. Fig. 67 shows the HB main waveforms and time instants definitions employed to analyze the true ZVS condition for the LLC resonant converter. Wherein, t_{dis} corresponds to the time required to deplete HB MOSFETs drain-source capacitance C_{DS}; t_{dead} is the HB gate-driver dead-time; and, t_{Dwin} is the duty-cycle window time (or dead-time window), which is the maximum dead-time that can be employed to achieve ZVS considering that $t_{dead} \geq t_{dis}$.

Mathematically, the true ZVS is achieved if the condition in (5.4.a) and (5.4.b) are true. Which correspond to a system with inductive characteristic and enough dead-time to discharge C_{DS}. The assumption that converter operate inside the inductive region is only a necessary

Figure 67 – DC/DC LLC resonant converter main waveform to assess the true ZVS conditions.



Source: Author.

condition for the ZVS, but not sufficient. With a good accuracy, t_{dis} can be estimated by (5.4.c), which can be rewritten by (5.4.d) in order to express the minimum tank current necessary at the end of the first half cycle ($i_{DS1.off}$) to deplete C_{DS} within t_{dead} interval. Throughout this analysis, to sidestep the C_{DS} non-linear behavior, the value employed for C_{DS} is actually given by $C_{oss.ef}$, which is defined in the MOSFET datasheet as the effective capacitance of MOSFET that gives the same charging time as a fixed capacitor while V_{DS} is rising from 0 to 80% of V_{DS}.

$$t_{dis} \leq t_{dead} \leq t_{Dwin} \tag{5.4a}$$

$$i_{DS1.on} = i_{DS1}(t_0) \leq 0 \tag{5.4b}$$

$$t_{dis} = \frac{2V_{IN}C_{DS}}{i_{S1.off}} \tag{5.4c}$$

$$i_{DS1.off} \geq \frac{2V_{IN}C_{DS}}{t_{dead}} = i_{S1.off.min} \tag{5.4d}$$

It is worth mentioning that the time-domain analysis discloses the exact current level at the switching instant, which is not possible employing the FHA approach. Therefore, a trustful and reliable design is going to be accomplished. Nevertheless, once ideal elements are considered, a safe margin should be taken into account.

5.2.5.4 Switching frequency operating range

As a function of the LLC filter elements, the converter will need a different switching frequency range ($\Delta f_{sw} = f_{max} - f_{min}$) in order to supply the load from the minimum to nominal

output power overall operating cases, here given by different bus voltage conditions. Since the ZVS condition is evaluated in the last step, the remaining critical condition is related to the admissible maximum switching frequency ($f_{ad.sw.max}$), which is limited by the employed gate-driver circuit, usually a dedicated integrated circuit. Therefore, if a specific filter requires a f_{sw} higher than $f_{ad.sw.max}$, it will be excluded from the possible solutions. Besides, extra wide Δf_{sw} are also avoided.

5.2.5.5 Magnetic elements volume

The proposed design procedure does not aim to optimize the converter power density; however, to give the designer a view of the power density, the volume of the magnetic elements can be analyzed before the final filter selection. This task is easily accomplished by inspecting the employed magnetic core size in each filter F_i.

5.2.5.6 Series resonant capacitor electrical stress

The series resonant capacitor C_S is subjected to the resonant tank current i_R and high RMS voltage stress $v_{Cs.rms}$. Considering the Metallized Polypropylene Film Capacitors, usually employed in resonant circuits, its volume is directly linked to the maximum RMS voltage. Therefore, the series resonant capacitor voltage must be as low as possible. Besides, to enhance the reliability, the $v_{Cs.rms}$ must be lower than the maximum permissible voltage of the selected device. This analysis is then completed by inspecting the maximum electrical stress in C_S.

5.2.5.7 Extra possible analysis

The ZCS for the output rectifier is achieved when the LLC operates in PO or OPO mode. Therefore, analyzing the LLC filter F_i operation mode allows one to infer the output rectifier's switching condition.

On the other hand, once the power loss for each component in the LLC converter is computed, thermal management can be easily incorporated into the design. So, if the maximum operating temperature is higher than the device limit, the necessity of a heat-sink could be seen in advance.

5.2.5.8 Final filter F_i selection

The main results and data from step 5 are compressed into a table to support the final filter selection and avoid a tedious data analysis. This table presents the filters sorted by the

$\langle \eta_{rank} \rangle$ index, together with the ZVS condition (YES or NOT), minimum and maximum f_{sw}, f_{sw} range, maximum t_{dis}, transformer and inductor magnetic core size, maximum C_S RMS voltage, and maximum resonant tank current.

5.3 DESIGN EXAMPLE

In order to elucidate the proposed design procedure and show its feasibility, the LLC converter is designed to supply an LED-based load over a wide operating range. This wide operating range occurs due to the bus voltage variation and current load regulation to achieve dimming. Wolfram MATHEMATICA v.12 software is employed to implement the design procedure algorithms. Therefore, two scripts are developed, where the first script implements Step 1 and Step 2, being the remaining steps finally implemented on the second script. Appendix G provides access to the mentioned scripts developed to perform the LLC resonant LED driver design.

5.3.1 Step 1: Electrical specification of the application

Serving as the first step of the proposed design procedure, Table 8 presents the LED driver electrical specifications. These specifications are discussed in Section 2.2, including the LED module details. As can be seen in Table 8, the DC/DC LLC resonant converter has to supply the LED module with different current levels considering a wide input voltage (V_{IN}) variation. A variable output current is required to achieve dimming capability.

To show the feasibility of the proposed design, the value for $f_o = 100\ kHz$ is adopted in order to maintain f_{sw} below the EMI test's lower boundary (150 kHz). Besides, in this range the circuit components are well-developed, more available, and less expensive (HUANG, 2010). However, to outcome with a competitive state-of-the-art design employing modern semiconductors devices, such as SiC and GaN, the LLC f_{sw} has to be in the range of some hundred to thousands of kHz.

Table 8 – LLC resonant LED driver electrical specifications

Application Parameters	Designator	Nominal	Min	Max
Half-bridge input voltage	V_{IN} or V_{BUS}	400 V	360 V	420 V
Average output current	I_O or I_{LED}	1.15 A	0.20 A	1.15 A
Outcome power	P_O	100 W	16 W	100 W
Outcome output voltage	V_O or V_{LED}	87.31 V	80.39 V	87.31 V
Main resonant frequency	f_o	100 kHz		

Source: Author.

5.3.2 Step 2: LLC time-domain analysis

The system electrical specifications and the values of C_S, L_S, L_M, and n must be known to perform the LLC converter TD analysis. The specifications are defined in the last step. Thus, the second step's initial task is to define the values of the resonant tank elements that will be employed in the TD analysis. In this way, each component in the LLC filter is swept over a bounded range in order to analyze different LLC resonant tank filters

The employed values for the transformer turns ratio n are defined in (5.5). The turns ratio determines the LLC converter unit gain, which is achieved when f_{sw} is equal to f_o. Considering n_1, the LLC supplies the LED with its nominal power when $V_{IN} = 400\ V$, and $f_{sw} = f_o$. Considering the input voltage variation and dimming range, the LLC converter implemented with n_1 operates around the main resonance. On the other hand, for n_2, the LLC supplies the LED with its minimum current when $V_{IN} = 420\ V$ and $f_{sw} = f_o$. In this way, considering the specified bus voltage variation and dimming, employing n_2, the LLC operates only below f_o. At this point it is important highlight that the turns ratio defined by n_1 is the classical approach employed to design the LLC. On the hand, new design methodologies define the turns ratio similarly to n_2, usually considering the converter-rated power instead of the minimum. In a general way, the transformer turns ratio is a decisive parameter in the converter operation region.

$$n_1 = \frac{V_{IN.NOM}}{2V_{O.NOM}} = \frac{400\ V}{2(87.31)\ V} = 2.29 \tag{5.5a}$$

$$n_2 = \frac{V_{IN.MAX}}{2V_{O.MIN}} = \frac{420\ V}{2(80.39)\ V} = 2.61 \tag{5.5b}$$

To define the C_S range, initially the base value is taken from the classical design based on FHA approach, detailed in Appendix A, from where, for the same specifications, the design outcomes with $C_S = 12\ nF$. Then, taking into account commercial values for capacitance, the capacitance range is defined selecting the commercial values around $C_S = 12\ nF$. In this way, selecting the B32672L series of the Metallized Polypropylene Film Capacitors from EPCOS (EPCOS, 2018), the employed range is given by (5.6). If the final selected filter is given by one of the extreme values for C_S, it is suggested to expand the search range.

$$C_s = [3.3,\ 5.6,\ 6.8,\ 8.2,\ 10,\ 12,\ 15,\ 22]\ nF \tag{5.6}$$

The series resonant inductance L_S can be determined by (5.7), whose definitions ensure the same f_o for all LLC resonant filters F_i. Then, for each specified C_S, being $f_o = 100\ kHz$, the value of L_S is computed by (5.7), yielding in (5.8).

$$L_s = \frac{1}{4\pi^2 C_S f_o} \tag{5.7}$$

$$L_s = [768,\ 452,\ 373,\ 309,\ 253,\ 211,\ 169,\ 115]\ \mu H \tag{5.8}$$

The L_M value is defined by (5.9), where L_n is the inductance ratio. Thus, considering the L_n values given in (5.10), the magnetizing inductance for each filter is easily computed.

$$L_M = L_S L_n \tag{5.9}$$

$$L_n = [2,\ 2.5,\ 3,\ 3.5,\ 4,\ 4.5,\ 5,\ 5.5] \tag{5.10}$$

Each single combination of L_S, C_S, L_M and n correspond to one LLC filter F_i. Thus, for the presented ranges, the outcome set of F_i is given in Table 9, yielding in 128 filters. It is worth mentioning that employing the same design specifications, the filter F_{43} correspond to the classically designed LLC resonant LED driver, described in Appendix A.

With the LLC set of filters defined, the TD analysis can be computed. Therefore, based on the LED driver electrical specifications, three operating cases are considered $C_1 : V_{IN} = 360\ V$, $C_2 : V_{IN} = 400\ V$, and $C_3 : V_{IN} = 420\ V$. In this way, for each case C_k the 128 LLC filters (F_1, F_2,..., F_{128}) are analyzed in the TD assuming load current variation ($I_O = 0.20,\ 0.30, ..., 1.10, 1.15\ A$). As shown in Fig. 66, for each case C_k and filter F_i combination, the implemented script exports a "$C_k F_i.csv$"file. This file carries the parameters needed to evaluate the LLC converter components voltage and current stress, ZVS condition, compute the power loss, and design the LLC magnetic and semiconductors components.

Employing Wolfram MATHEMATICA v.12, running in a laptop equipped with i7-9750H core and 16 GB RAM, the scrip implementing Step 1 and Step 2 took 82 minutes to be computed, giving up to 384 $C_k F_i.csv$ files, where a total of 4194 LLC steady-state operating points are solved. It means that on average, in 1.17 seconds, the mode-solver identify the correct operation mode to achieve the desired output current and performs the analysis calculating: Average output voltage; Average output current; HB switches turn-off current; HB switches RMS current; Resonant tank RMS current; Resonant tank peak current; Series resonant capacitor RMS voltage; Series resonant capacitor peak voltage; Secondary side RMS current; Output capacitor RMS current; Rectifier average current; Rectifier peak current; and Duty-cycle window time.

Table 9 – LLC resonant LED driver resonant tank set of filters F_i

n	C_S	L_S	L_M							
			$L_n = 2.0$	$L_n = 2.5$	$L_n = 3.0$	$L_n = 3.5$	$L_n = 4.0$	$L_n = 4.5$	$L_n = 5.0$	$L_n = 5.5$
2.29	3.3 nF	768 μH	$\mathbf{F_1}$	$\mathbf{F_2}$	$\mathbf{F_3}$	$\mathbf{F_4}$	$\mathbf{F_5}$	$\mathbf{F_6}$	$\mathbf{F_7}$	$\mathbf{F_8}$
			1535 μH	1919 μH	2303 μH	2687 μH	3070 μH	3454 μH	3838 μH	4222 μH
2.29	5.6nF	452 μH	$\mathbf{F_9}$	$\mathbf{F_{10}}$	$\mathbf{F_{11}}$	$\mathbf{F_{12}}$	$\mathbf{F_{13}}$	$\mathbf{F_{14}}$	$\mathbf{F_{15}}$	$\mathbf{F_{16}}$
			905 μH	1131 μH	1357 μH	1583 μH	1809 μH	2035 μH	2262 μH	2488 μH
2.29	6.8 nF	373 μH	$\mathbf{F_{17}}$	$\mathbf{F_{18}}$	$\mathbf{F_{19}}$	$\mathbf{F_{20}}$	$\mathbf{F_{21}}$	$\mathbf{F_{22}}$	$\mathbf{F_{23}}$	$\mathbf{F_{24}}$
			745 μH	931 μH	1118 μH	1304 μH	1490 μH	1676 μH	1863 μH	2049 μH
2.29	8.2 nF	309 μH	$\mathbf{F_{25}}$	$\mathbf{F_{26}}$	$\mathbf{F_{27}}$	$\mathbf{F_{28}}$	$\mathbf{F_{29}}$	$\mathbf{F_{30}}$	$\mathbf{F_{31}}$	$\mathbf{F_{32}}$
			618 μH	772 μH	927 μH	1081 μH	1236 μH	1390 μH	1545 μH	1699 μH
2.29	10 nF	253 μH	$\mathbf{F_{33}}$	$\mathbf{F_{34}}$	$\mathbf{F_{35}}$	$\mathbf{F_{36}}$	$\mathbf{F_{37}}$	$\mathbf{F_{38}}$	$\mathbf{F_{39}}$	$\mathbf{F_{40}}$
			507 μH	633 μH	760 μH	887 μH	1013 μH	1140 μH	1267 μH	1393 μH
2.29	12 nF	211 μH	$\mathbf{F_{41}}$	$\mathbf{F_{42}}$	$\mathbf{F_{43}}$	$\mathbf{F_{44}}$	$\mathbf{F_{45}}$	$\mathbf{F_{46}}$	$\mathbf{F_{47}}$	$\mathbf{F_{48}}$
			422 μH	528 μH	633 μH	739 μH	844 μH	950 μH	1055 μH	1161 μH
2.29	15 nF	169 μH	$\mathbf{F_{49}}$	$\mathbf{F_{50}}$	$\mathbf{F_{51}}$	$\mathbf{F_{52}}$	$\mathbf{F_{53}}$	$\mathbf{F_{54}}$	$\mathbf{F_{55}}$	$\mathbf{F_{56}}$
			338 μH	422 μH	507 μH	591 μH	675 μH	760 μH	844 μH	929 μH
2.29	22 nF	115 μH	$\mathbf{F_{57}}$	$\mathbf{F_{58}}$	$\mathbf{F_{59}}$	$\mathbf{F_{60}}$	$\mathbf{F_{61}}$	$\mathbf{F_{62}}$	$\mathbf{F_{63}}$	$\mathbf{F_{64}}$
			230 μH	288 μH	345 μH	403 μH	461 μH	518 μH	576 μH	633 μH
2.61	3.3 nF	768 μH	$\mathbf{F_{65}}$	$\mathbf{F_{66}}$	$\mathbf{F_{67}}$	$\mathbf{F_{68}}$	$\mathbf{F_{69}}$	$\mathbf{F_{70}}$	$\mathbf{F_{71}}$	$\mathbf{F_{72}}$
			1535 μH	1919 μH	2303 μH	2687 μH	3070 μH	3454 μH	3838 μH	4222 μH
2.61	5.6 nF	452 μH	$\mathbf{F_{73}}$	$\mathbf{F_{74}}$	$\mathbf{F_{75}}$	$\mathbf{F_{76}}$	$\mathbf{F_{77}}$	$\mathbf{F_{78}}$	$\mathbf{F_{79}}$	$\mathbf{F_{80}}$
			905 μH	1131 μH	1357 μH	1583 μH	1809 μH	2035 μH	2262 μH	2488 μH
2.61	6.8 nF	373 μH	$\mathbf{F_{81}}$	$\mathbf{F_{82}}$	$\mathbf{F_{83}}$	$\mathbf{F_{84}}$	$\mathbf{F_{85}}$	$\mathbf{F_{86}}$	$\mathbf{F_{87}}$	$\mathbf{F_{88}}$
			745 μH	931 μH	1118 μH	1304 μH	1490 μH	1676 μH	1863 μH	2049 μH
2.61	8.2 nF	309 μH	$\mathbf{F_{89}}$	$\mathbf{F_{90}}$	$\mathbf{F_{91}}$	$\mathbf{F_{92}}$	$\mathbf{F_{93}}$	$\mathbf{F_{94}}$	$\mathbf{F_{95}}$	$\mathbf{F_{96}}$
			618 μH	772 μH	927 μH	1081 μH	1236 μH	1390 μH	1545 μH	1699 μH
2.61	10 nF	253 μH	$\mathbf{F_{97}}$	$\mathbf{F_{98}}$	$\mathbf{F_{99}}$	$\mathbf{F_{100}}$	$\mathbf{F_{101}}$	$\mathbf{F_{102}}$	$\mathbf{F_{103}}$	$\mathbf{F_{104}}$
			507 μH	633 μH	760 μH	887 μH	1013 μH	1140 μH	1267 μH	1393 μH
2.61	12 nF	211 μH	$\mathbf{F_{105}}$	$\mathbf{F_{106}}$	$\mathbf{F_{107}}$	$\mathbf{F_{108}}$	$\mathbf{F_{109}}$	$\mathbf{F_{110}}$	$\mathbf{F_{111}}$	$\mathbf{F_{112}}$
			422 μH	528 μH	633 μH	739 μH	844 μH	950 μH	1055 μH	1161 μH
2.61	15 nF	169 μH	$\mathbf{F_{113}}$	$\mathbf{F_{114}}$	$\mathbf{F_{115}}$	$\mathbf{F_{116}}$	$\mathbf{F_{117}}$	$\mathbf{F_{118}}$	$\mathbf{F_{119}}$	$\mathbf{F_{120}}$
			338 μH	422 μH	507 μH	591 μH	675 μH	760 μH	844 μH	929 μH
2.61	22 nF	115 μH	$\mathbf{F_{121}}$	$\mathbf{F_{122}}$	$\mathbf{F_{123}}$	$\mathbf{F_{124}}$	$\mathbf{F_{125}}$	$\mathbf{F_{126}}$	$\mathbf{F_{127}}$	$\mathbf{F_{128}}$
			230 μH	288 μH	345 μH	403 μH	461 μH	518 μH	576 μH	633 μH

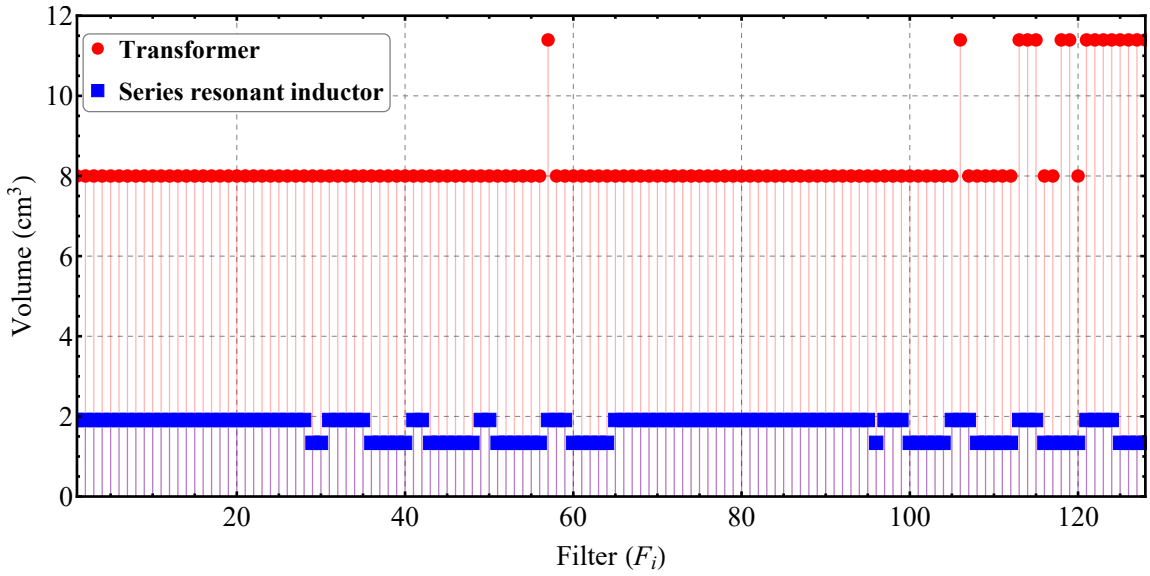
Source: Author.

5.3.3 Step 3: Discrete components design

Considering each filter F_i operating at the extreme input voltages ($V_{IN} = 360\ V$ and $V_{IN} = 420\ V$), the third step of the design procedure starts defining the critical operating point for each filter, which correspond to the condition where the maximum voltage and current stress is noticed. Identified this critical operating point, the design procedure follows with the magnetic elements and power semiconductors selection. To avoid magnetic element saturation and power semiconductors damage, the identified critical voltage and current levels are increased by 20% and then utilized to design the magnetic and power semiconductors.

The procedure employed to design the magnetic and power semiconductors devices is presented in Appendix C. To illustrate the outcome for the design of the magnetic components, Fig. 68 shows for each filter F_i the magnetic core volume of the transformer and the series

Figure 68 – LLC converter magnetic cores volume.



Source: Author.

resonant inductor. As can be seen, for most filters, the EE core EE30/15/14, with volume of 8 cm^3 is employed to assemble the transformer. The core employed for the inductor changes between 25/10/06 (1.9 cm^3) and 20/10/05 (1.34 cm^3).

The HB switches and output rectifier diodes are designed to withstand the maximum voltage and current stress. Since all filters F_i are submitted to similar electrical stress, the same power semiconductors are selected. For the HB switches, the MOSFET model STP10NM60N from STMicroelectronics was selected. The rectifier diode employs the Schottky diode SB3200.

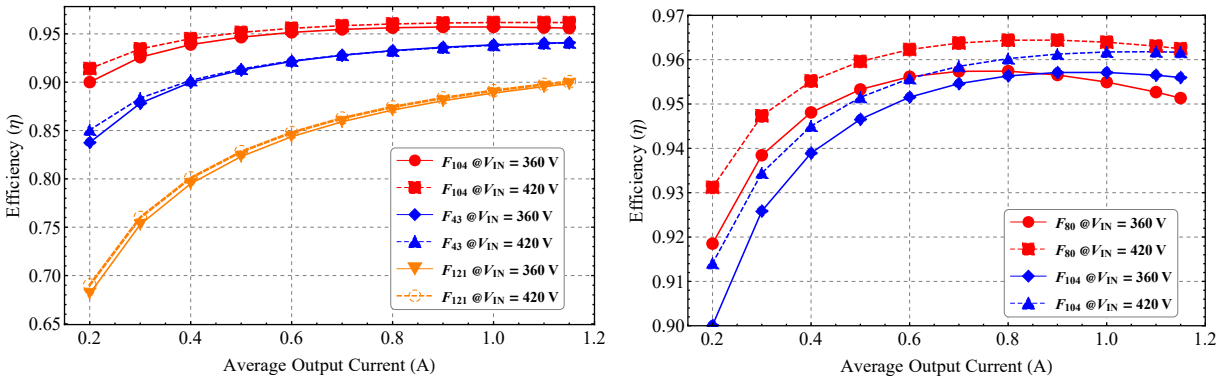
5.3.4 Step 4: LLC power losses and efficiency computation

At this moment, the power semiconductor devices and magnetic elements employed in each filter F_i are known. The LLC converter's current and voltage levels are already computed for each filter F_i operating at different input voltages and load conditions. Thus, it is now possible to estimate the LLC resonant converter components' power losses and, consequently, estimate the converter efficiency. The procedure employed to estimate the LLC components' power losses is detailed in Appendix D. In the sequence, for each filter F_i, case C_k, and output current I_O the LLC converter efficiency is estimated by (5.1).

To exemplify this fourth step outcomes, Fig. 69 shows the theoretical computed efficiency for filters F_{104}, F_{43}, F_{121}, and F_{80} operating at different input voltages and with output current variation between 0.2 A and 1.15 A. Analyzing Fig. 69 it can be noticed a considerable efficiency variation among these filters. In this way, the use of the estimated efficiency as a parameter to guide the LLC design shows to be an interesting approach.

Figure 69 – LLC resonant filters F_i estimated efficiency under different input voltage and load conditions.

(a) – F_{104}, F_{43}, F_{121} (b) – F_{80}, F_{104}



Source: Author.

5.3.5 Step 5: LLC resonant filter F_i selection

The last step in the design procedure deals with the selection of the most prominent LLC filter F_i among the initial set of filters (F_1, F_2,...,F_{128}). Therefore, several characteristics are examined to achieve a reliable and well-designed LLC resonant LED driver.

5.3.5.1 Peak gain evaluation

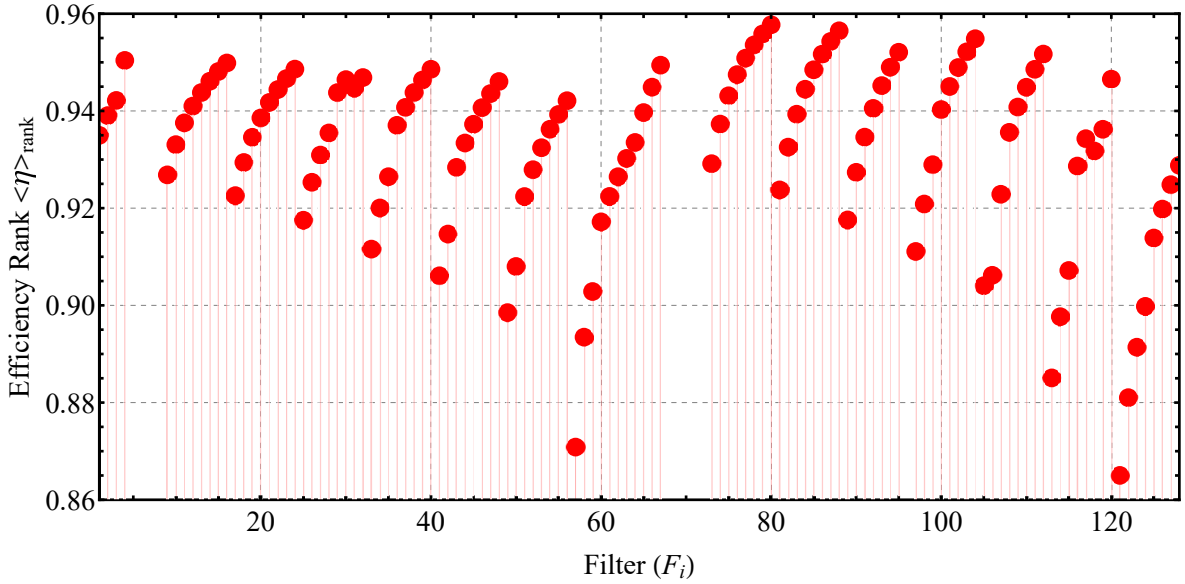
The LLC filter selection starts with the current gain analysis. Thus, the LLC filter F_i whose current peak gain is insufficient to supply the LED load with its nominal current under the minimum input voltage is excluded from the set of the possible solution. This task is automatically performed in the second script by testing if the maximum output current $I_O = 1.15\ A$ is achieved under the minimum input voltage.

Running this test, filters F_5, F_6, F_7, F_8 , F_{68}, F_{69}, F_{70}, F_{71}, F_{72}, and F_{96} are excluded from the set of possible solutions because they do not present the required current gain.

5.3.5.2 Efficiency evaluation

Fig. 70 shows the computed efficiency rank $\langle \eta_{rank} \rangle$ for each filter F_i that present enough current gain to supply the LED load, being P_j the power related to each evaluated I_O in LLC TD analysis. Analyzing Fig. 70, it is noticed that the filters F_{80}, F_{88}, F_{79}, F_{104}, F_{87}, F_{78}, F_{103}, F_{95}, F_{112}, and F_{86} present the highest values for the efficiency rank $\langle \eta_{rank} \rangle$, respectively. Comparing the efficiency of filters F_{104} and F_{121} shown in Fig. 69 with the $\langle \eta_{rank} \rangle$ of this filters presented in

Figure 70 – The $\langle \eta_{rank} \rangle$ of each filter F_i that present enough current gain to supply the LED load.



Source: Author.

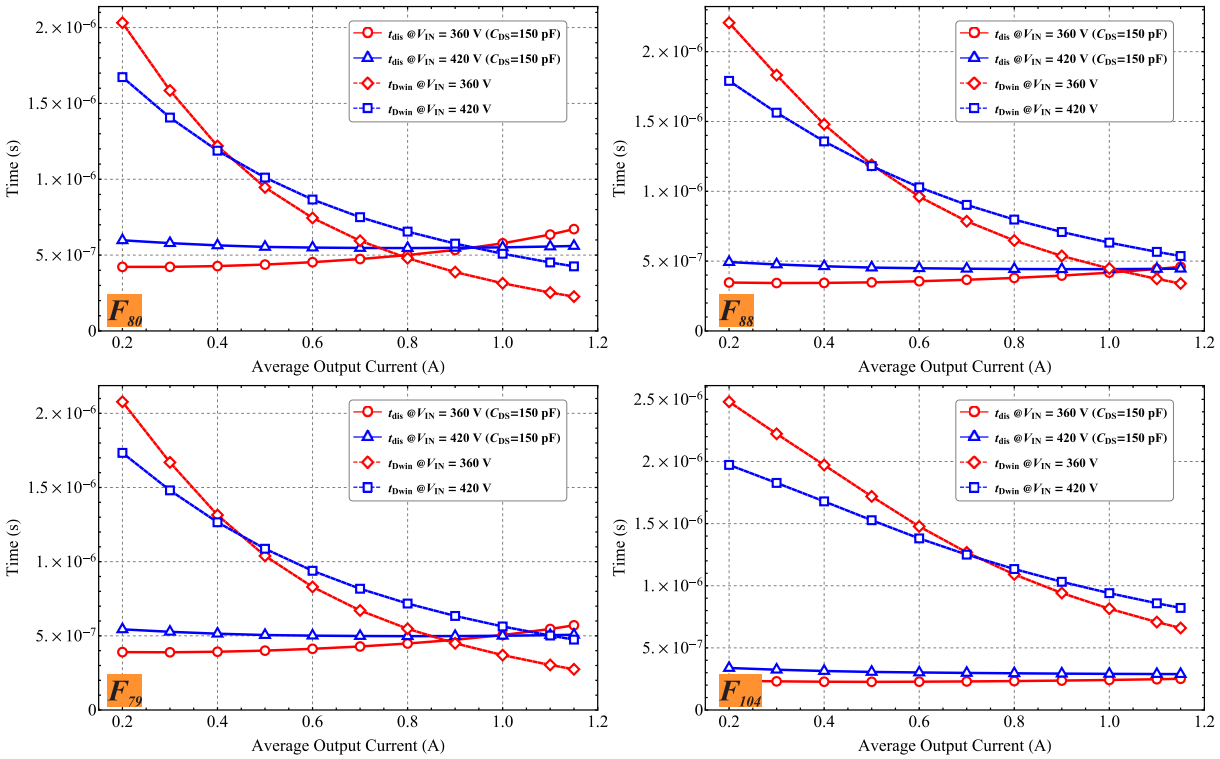
Fig. 70, it is noticed a flat relationship between $\langle \eta_{rank} \rangle$ and the efficiency performance over the whole operation range. In this way, the $\langle \eta_{rank} \rangle$ performance index shows to be an interesting metric to sort the filters from the initial set.

On the other hand, the weight for each power level considered in the computation of $\langle \eta_{rank} \rangle$ could be changed to meet other design requirements. For instance, zeroing the weights for any power level below the rated power, i.e., computing the $\langle \eta_{rank} \rangle$ only for the nominal power, the highest $\langle \eta_{rank} \rangle$ values are obtained respectively by filters F_{104}, F_{80}, F_{112}, F_{103}, F_{88}, F_{79}, F_{111}, F_{87}.

5.3.5.3 ZVS constraint

The filter F_i selected at the end should not violate the constraint imposed by (5.4). To elucidate how the ZVS condition is verified, Fig. 71 shows for the filters F_{80}, F_{88}, F_{79}, and F_{104} the time required to deplete C_{DS}, which is t_{dis}, and the maximum allowed dead-time t_{Dwin}. As can be seen, F_{80}, F_{88}, and F_{79} violate the constraint given by (5.4.a), once t_{dis} becomes greater than the available t_{Dwin}. Therefore, these filters should not be selected as the final solution. On the other hand, for F_{104} it can be seen that $t_{Dwin} > t_{dis}$, thus by defining the dead-time t_{dead} in accordance to $t_{dis} < t_{dead} < t_{Dwin}$ the ZVS condition is achieved over the whole operating range. To evaluate the ZVS condition automatically in the second script, for each filter the difference given by $t_{Dwin} - t_{dis}$ is calculated for each load condition under the same input voltage. In sequence the minimum value from this computation is inspected, where if the $Min\,[t_{Dwin} - t_{dis}]$ becomes negative, means that (5.4.a) is violated for this filter.

Figure 71 – Filters F_{80}, F_{88}, F_{79}, and F_{104} ZVS constraint evaluation.



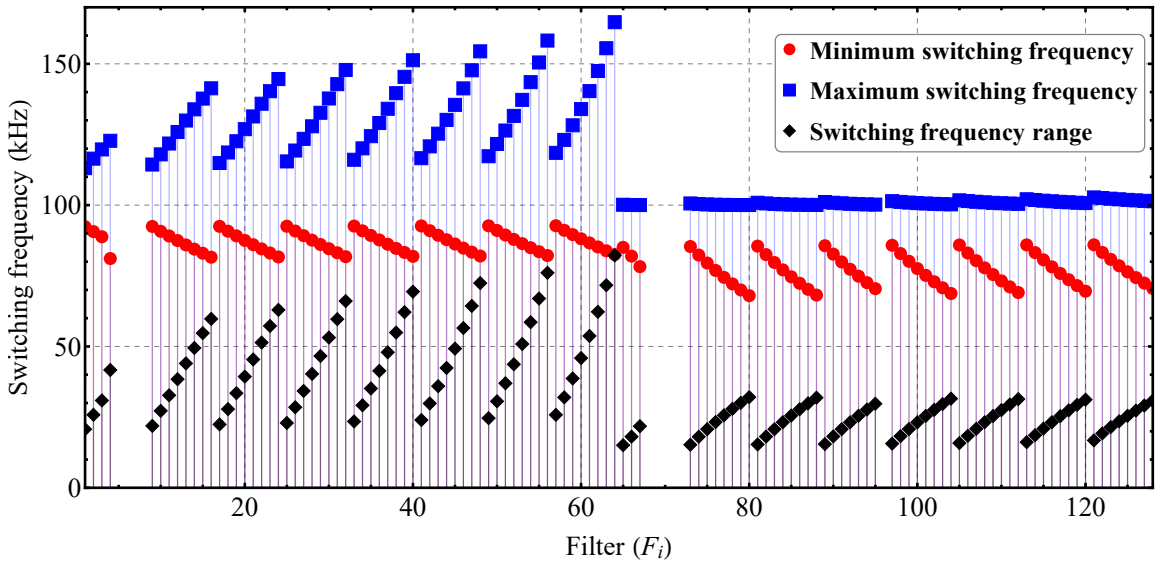
Source: Author.

Finally, if (5.4.a) is not infringed, the maximum t_{dis} among the cases is employed to design the gate-drive t_{dead}. Thus, the gate-driver dead-time is defined by making $t_{dead} \geq \text{Max}[t_{dis}]$. To assess (5.4.b), the converter symmetric behavior in relation to the half-switching cycle is consider, which outcome in $i_{DS1.off} = -i_{DS1.on}$.

5.3.5.4 Switching frequency operating range

In the LLC resonant LED driver the f_{sw} is modulated to maintain I_{LED} regulated. Therefore, each filter F_i presents a specific value for the maximum f_{sw}, minimum f_{sw} and Δf_{sw}. To exemplify this statement, Fig. 72 shows the f_{sw} values for each filter that presents enough current gain to supply the LED. As can be seen, each filter needs a specific Δf_{sw} to maintain output current controlled. Small Δf_{sw} will present issues related to the high sensibility of the output current variation. On the other hand, extra wide Δf_{sw} is limited by the gate-driver capability. Besides, wide f_{sw} variation increase the complexity related to EMI filters design. Thus, filters with a moderate Δf_{sw} should have priority in the final selection.

Figure 72 – Switching frequency range for each filter F_i that presents enough current gain to supply the LED load.

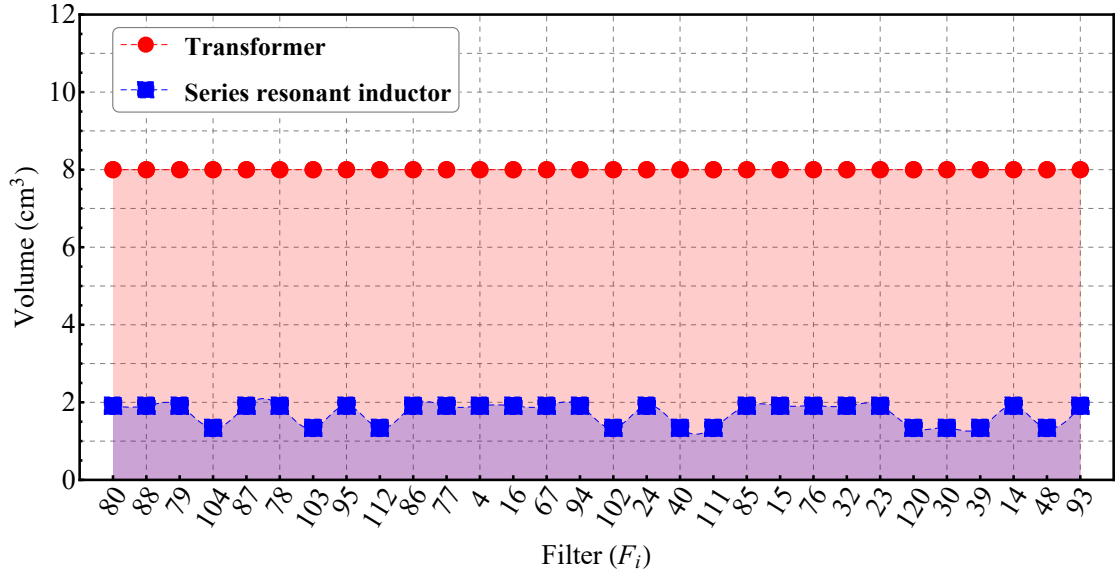


Source: Author.

5.3.5.5 Magnetic elements volume

Previously, Fig. 68 showed the volume of the transformer and series resonant inductor magnetic cores for each filter F_i . On the other hand, Fig. 73 shows the magnetic core volume of the transformer and the series resonant inductor L_S for the thirty filters with the highest $\langle \eta_{rank} \rangle$.

Figure 73 – Magnetic volume of the transformer and the L_S for the thirty filters with the highest $\langle \eta_{rank} \rangle$.



Source: Author.

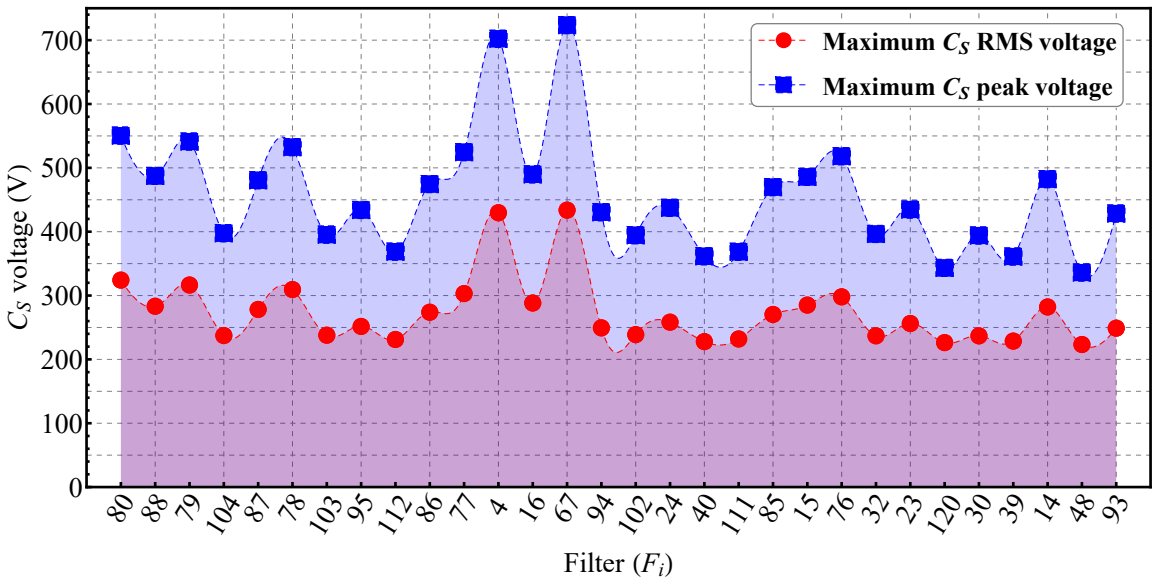
In this way, before culminating with the selection of the filter, the the designer can assess the LLC converter power density.

5.3.5.6 Series resonant capacitor electrical stress

Fig. 74 shows the C_S maximum RMS and peak voltage for the thirty filters with the highest $\langle \eta_{rank} \rangle$. As can be seen, each F_i filter presents a specific value. Thus, as a function of the selected filter, the appropriate capacitor must be picked. Similarly, Fig. 75 shows C_S maximum RMS and peak current, whose value does not change significantly among the filters F_i.

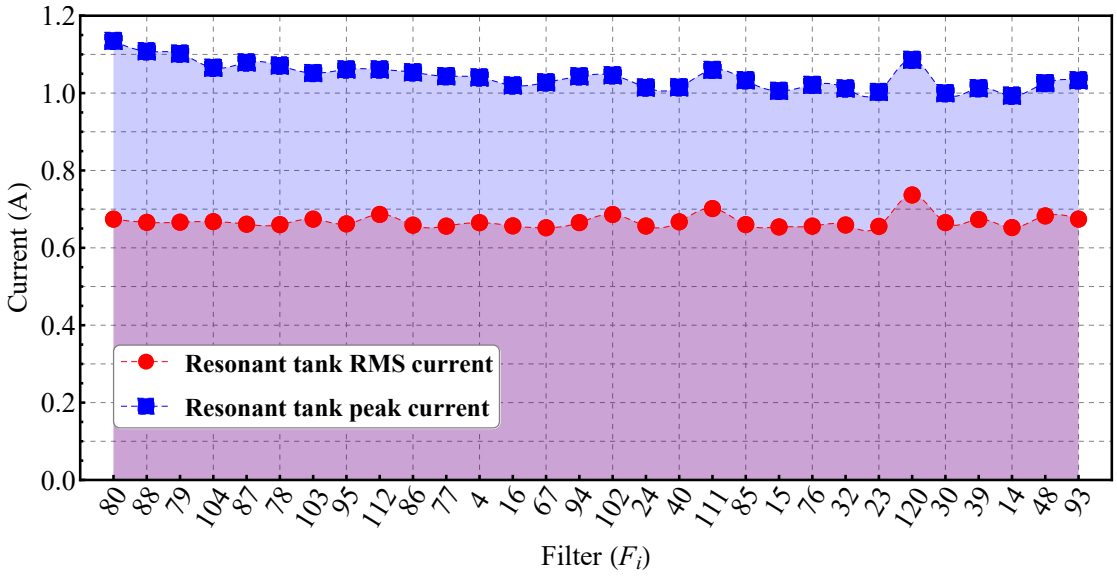
In the third step of the design procedure, the B32672L series from the EPCOS Metallized Polypropylene Film Capacitors was selected for the series resonant capacitor C_S. The B32672L series presents several capacitances values and different maximum voltage and current ratings. Fig. 76 shows the maximum permissible AC voltage and current derating versus frequency for the B32672L series specified by 2000 VDC/700 VAC. Then, to finally select the series resonant capacitor, the capacitor's maximum permissible AC voltage must be higher than the maximum RMS value.

Figure 74 – Maximum C_S RMS and peak voltage for the thirty filters with the highest $\langle \eta_{rank} \rangle$.



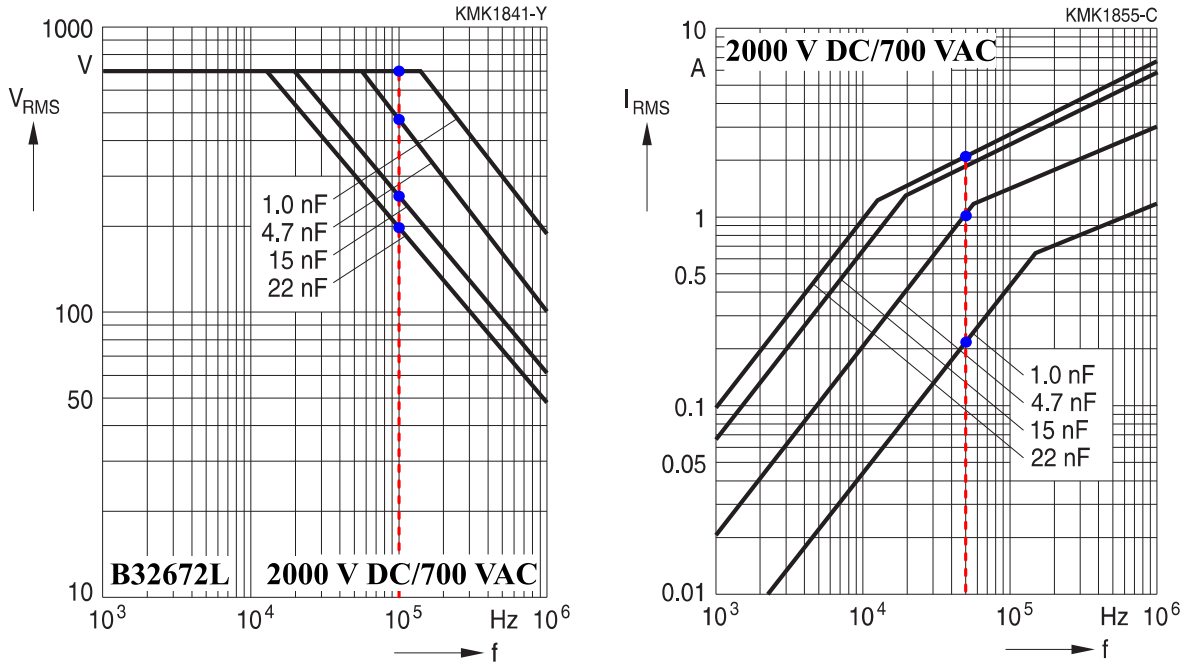
Source: Author.

Figure 75 – Maximum resonant tank RMS and peak current for the thirty filters with the highest $\langle \eta_{rank} \rangle$.



Source: Author.

Figure 76 – Metallized Polypropylene Film Capacitors maximum permissible AC voltage and current derating versus frequency for the B32672L series - 2000 VDC/700 VAC.



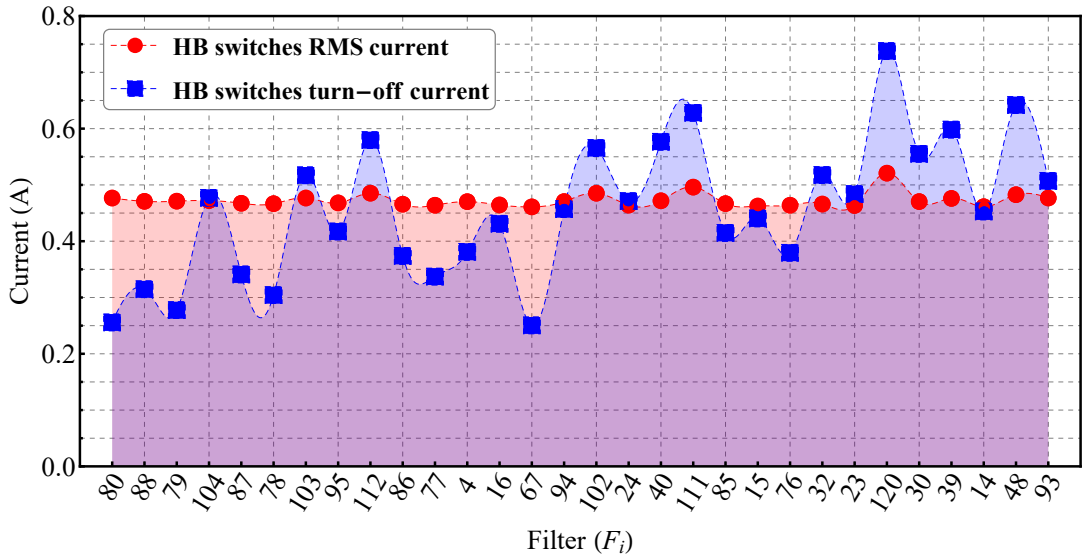
Source: Adapted from (EPCOS, 2018).

5.3.5.7 Extra possible analysis

Several other features could be analyzed under the design procedure. However, these analyses rarely will change the final decision since the mandatory constraint have already been considered. To exemplify this possible extra analysis, Fig. 77 shows maximum HB switches RMS and turn-off current for the thirty filters with the highest $\langle \eta_{rank} \rangle$. As can be seen, the RMS current is quite similar among the filters F_i. On the other hand, the maximum value of the HB switches turn-off current changes considerably among the filters. The turn-off current influence the switching loss as well as the ZVS condition.

The LLC converter operation mode can be employed to assess the switching condition of the output rectifier. Thus, to evaluate this condition, Table 10 shows the operation modes for filter F_{104} and F_{43}. As expected, F_{104} that employs n_2, operates only below f_o, where the PO and OPO modes occur. PO and OPO modes provide ZCS for output rectifier.

Figure 77 – Maximum HB switches RMS and turn-off current for the 30 filters with the highest $\langle \eta_{rank} \rangle$.



Source: Author.

Table 10 – LLC converter operation modes.

$\mathbf{I_O}$	Filter F_{104}				Filter F_{43}			
	$V_{IN} = 360\ V$		$V_{IN} = 420\ V$		$V_{IN} = 360\ V$		$V_{IN} = 420\ V$	
	Mode	$f_{sw}\ (kHz)$	Mode	$f_{sw}\ (kHz)$	Mode	$f_{sw}\ (kHz)$	Mode	$f_{sw}\ (kHz)$
0.2	OPO	77.7	OPO	100.3	OPO	97.9	NOP	125.3
0.4	OPO	75.5	OPO	95.2	OPO	94.8	NOP	117.1
0.6	PO	73.3	PO	91.9	OPO	93.1	NP	112.9
1.0	PO	69.8	PO	86.9	PO	90.3	NP	107.8
1.15	PO	68.7	PO	85.3	PO	89.4	NP	106.2

Source: Author.

5.3.5.8 Final filter F_i selection

In order to support the final filter selection and avoid a tedious data analysis, the leading data computed in step 5 are consolidated into a table. This table presents the filters sorted by the $\langle \eta_{rank} \rangle$, together with the ZVS condition (YES or NOT), minimum and maximum f_{sw}, f_{sw} range, maximum t_{dis}, transformer and inductor magnetic core size, maximum C_S RMS voltage, maximum C_S peak voltage, and maximum resonant tank current.

Table 11 presents the data for the 50 filters with highest efficiency rank. From this table, it is clear to see that filter F_{80}, F_{88}, and F_{79}, even presenting the highest $\langle \eta_{rank} \rangle$, are not reliable solutions due to the absence of ZVS. For the filters that do not present ZVS, the computed $\langle \eta_{rank} \rangle$ is not the real one due to the LLC power loss model employed to compute the LLC efficiency. In this power loss model, the HB ZVS is assumed, and so only switching turn-off power loss is considered. Consequently, if the filter F_i does not present ZVS the associated $\langle \eta_{rank} \rangle$ is not the correct one.

Analyzing Table 11, filters F_{104}, F_{103}, F_{95}, F_{112} and F_{86} are the first five filters that present ZVS over the whole operating range. Filter F_{95} presents a larger magnetic core size for the inductor compared to the other four mentioned filters. Carefully analyzing F_{104}, F_{103}, F_{112} and F_{86}, no significant difference is noticed that justify the selection for one or another. Nevertheless, respecting the efficiency rank index, the filter F_{104} is the selected one. Table 12 summarize the design parameters and the components of the selected filter F_{104}.

Table 11 presents the condensed data for the selected filter F_{104}, filter F_{43} that is the outcome when the classical designed procedure is employed, and filter F_{121} that is the worst solution from the initial set of filters. As can be seen, filters F_{104} and F_{103} utilize equal magnetic core sizes and have similar voltage stress in the series resonant capacitor. However, they differ in the efficiency rank, resonant tank current i_R, and f_{sw} range. Therefore, it is expected a superior performance for the selected filter when compared to the conventional one. Besides, analyzing the resonant tank components, it is noticed that F_{104} presents a higher L_M value compared to F_{43}, which follows a common trend noticed on design procedures that try to optimized the LLC performance. In the classical design procedure, the trade-off between enough turn-off current for HB switches to achieve ZVS and the resonant tank current RMS value to reduce the conduction power losses is optimized by the L_M design. So the highest possible L_M value that allows ZVS is selected. However, the estimated current levels in the classical design is not the real one due to the FHA lack of accuracy for the operation beyond f_o. Thus, an unreliable design is achieved when employing the classical design. On the other hand, the proposed design procedure outcomes in a superior design since the real behavior of the converter is considered due to the employed TD analysis. Consequently, F_{104} presents a reliable optimized L_M value.

Finally, it is worth mentioning that, even being discussed step by step, the second implemented script performs all these assessments automatically, yielding on Table 11. The

Table 11 – Final LLC filter selection support data

$\mathbf{F_i}$	η_{rank}	$Min[t_{Dwin} - t_{dis}]$ 360 V	420 V	ZVS	$Max[t_{dis}]$ (ns)	f_{min} (kHz)	f_{max} (kHz)	Δf_{sw} (kHz)	**Trx**	L_S	V_{CsRMS} (V)	$Max[i_R]$ (A)
80	0.958	-445	-134	NO	671	67.9	100.0	32.1	EE.30/15/14	EE.25/10/6	324	0.674
88	0.956	-119	91	NO	493	68.2	100.1	31.9	EE.30/15/14	EE.25/10/6	283	0.665
79	0.956	-296	-33	NO	570	69.9	100.0	30.1	EE.30/15/14	EE.25/10/6	316	0.666
104	0.955	409	532	YES	338	68.7	100.3	31.6	EE.30/15/14	EE.20/10/5	237	0.667
87	0.954	-3.3	189	NO	449	70.2	100.1	29.9	EE.30/15/14	EE.25/10/6	278	0.661
78	0.953	-152	78	NO	490	72.1	100.1	28.0	EE.30/15/14	EE.25/10/6	309	0.659
103	0.952	518	632	YES	308	70.7	100.3	29.6	EE.30/15/14	EE.20/10/5	237	0.674
95	0.952	249	401	YES	374	70.4	100.2	29.8	EE.30/15/14	EE.25/10/6	251	0.661
112	0.952	668	749	YES	283	69.1	100.5	31.4	EE.30/15/14	EE.20/10/5	231	0.686
86	0.952	119	298	YES	405	72.3	100.1	27.8	EE.30/15/14	EE.25/10/6	273	0.658
77	0.951	-5.4	201	NO	436	74.4	100.1	25.7	EE.30/15/14	EE.25/10/6	303	0.656
4	0.950	-506	233	NO	753	81.1	122.8	41.7	EE.30/15/14	EE.25/10/6	429	0.665
16	0.950	-333	268	NO	610	81.6	141.3	59.7	EE.30/15/14	EE.25/10/6	288	0.656
67	0.949	-841	-97	NO	1007	78.2	100.0	21.8	EE.30/15/14	EE.25/10/6	433	0.651
94	0.949	368	511	YES	337	72.6	100.3	27.7	EE.30/15/14	EE.25/10/6	249	0.665
102	0.949	641	744	YES	278	72.9	100.5	27.6	EE.30/15/14	EE.20/10/5	238	0.686
24	0.949	-106	344	NO	492	81.7	144.6	62.9	EE.30/15/14	EE.25/10/6	258	0.656
40	0.948	303	533	YES	389	81.9	151.3	69.4	EE.30/15/14	EE.20/10/5	227	0.667
111	0.948	782	849	YES	258	71.1	100.5	29.4	EE.30/15/14	EE.20/10/5	231	0.701
85	0.948	254	420	YES	361	74.6	100.2	25.6	EE.30/15/14	EE.25/10/6	270	0.660
15	0.948	-229	303	NO	544	83.0	137.7	54.7	EE.30/15/14	EE.25/10/6	285	0.654
76	0.947	151	340	YES	383	76.9	100.1	23.2	EE.30/15/14	EE.25/10/6	297	0.656
32	0.947	95	430	YES	440	81.8	147.8	66.0	EE.30/15/14	EE.25/10/6	236	0.659
23	0.947	-13	386	NO	464	83.1	140.3	57.2	EE.30/15/14	EE.25/10/6	256	0.655
120	0.946	1013	1022	YES	228	69.5	100.7	31.2	EE.30/15/14	EE.20/10/5	226	0.736
30	0.946	284	539	YES	380	84.6	137.7	53.1	EE.30/15/14	EE.20/10/5	236	0.665
39	0.946	394	591	YES	360	83.3	145.4	62.1	EE.30/15/14	EE.20/10/5	228	0.673
14	0.946	-120	346	NO	491	84.4	133.9	49.5	EE.30/15/14	EE.25/10/6	282	0.652
48	0.946	501	639	YES	346	82.0	154.4	72.4	EE.30/15/14	EE.20/10/5	223	0.682
93	0.945	502	634	YES	301	74.9	100.4	25.5	EE.30/15/14	EE.25/10/6	248	0.674
101	0.945	779	866	YES	249	75.1	100.6	25.5	EE.30/15/14	EE.20/10/5	240	0.706
66	0.9445	-175	101	NO	514	81.9	100.1	18.2	EE.30/15/14	EE.25/10/6	417	0.647
110	0.945	908	960	YES	233	73.2	100.7	27.5	EE.30/15/14	EE.20/10/5	233	0.724
31	0.944	184	479	YES	412	83.2	142.8	59.6	EE.30/15/14	EE.25/10/6	235	0.660
84	0.944	405	559	YES	318	77.1	100.3	23.2	EE.30/15/14	EE.25/10/6	268	0.667
22	0.944	88	438	YES	432	84.5	135.9	51.4	EE.30/15/14	EE.25/10/6	254	0.656
38	0.944	496	659	YES	330	84.7	139.6	54.9	EE.30/15/14	EE.20/10/5	229	0.682
13	0.944	-3.2	400	NO	454	85.9	129.9	44.0	EE.30/15/14	EE.25/10/6	279	0.652
29	0.944	397	612	YES	345	86.1	132.8	46.7	EE.30/15/14	EE.20/10/5	238	0.673
47	0.943	594	703	YES	318	83.4	147.7	64.3	EE.30/15/14	EE.20/10/5	224	0.693
75	0.943	327	501	YES	331	79.2	100.2	21.0	EE.30/15/14	EE.25/10/6	294	0.662
3	0.942	-354	289	NO	637	88.8	119.7	30.9	EE.30/15/14	EE.25/10/6	391	0.643
56	0.942	756	781	YES	297	82.2	158.2	76.0	EE.30/15/14	EE.20/10/5	219	0.716
21	0.942	200	502	YES	396	86.0	131.4	45.4	EE.30/15/14	EE.25/10/6	253	0.660
12	0.941	126	469	YES	412	87.5	125.9	38.4	EE.30/15/14	EE.25/10/6	277	0.655
109	0.941	1048	1082	YES	208	75.4	100.8	25.4	EE.30/15/14	EE.20/10/5	235	0.750
37	0.941	612	741	YES	298	86.2	134.1	47.9	EE.30/15/14	EE.20/10/5	231	0.698
46	0.941	700	779	YES	288	84.8	141.3	56.5	EE.30/15/14	EE.20/10/5	225	0.710
92	0.940	656	775	YES	265	77.3	100.5	23.2	EE.30/15/14	EE.25/10/6	250	0.691
100	0.940	936	1006	YES	219	77.6	100.7	23.1	EE.30/15/14	EE.20/10/5	242	0.738

Source: Author.

Table 12 – LLC resonant LED driver parameters

Parameter	**Designator**	**Value**
LLC resonant LED driver design specification		
Nominal DC input voltage	V_{BUS}	400 V
Minimum DC input	$V_{BUS.MIN}$	360 V
Maximum DC input voltage	$V_{BUS.MAX}$	420 V
LLC converter resonant frequency	f_o	100 kHz
Maximum LLC converter output power	P_O	100 W
Minimal LLC converter output power	$P_{O.MIN}$	≈15 W
Designed LLC LED driver resonant converter - F_{104}		
Average LED current range	I_{LED}	$0.2 - 1.15$ A
Average LED voltage	V_{LED}	$80.4 - 87.3$ V
Resonant capacitor B32672L series - 2000 VDC/700 VAC	C_S	10 nF
Resonant inductor EE 20/10/05; 27 turns; 2#AWG27	L_S	253μ H
Magnetizing inductance	L_M	1393 μ H
Output capacitor (Film capacitor)	C_O	10 $\mu F/100$ V
Transformer turns ratio (n) EE 30/15/14; $n_P = 40$ (2#AWG27); $n_S = 15.5$ (3#AWG27)	N_P/N_S	2.61
Half-bridge power MOSFETs	S_1-S_2	STP10NM60N
Output rectifier diodes	D_1-D_2	SB3200TA

Source: Author.

Table 13 – Filter F_{104}, F_{43}, and F_{121} comparison

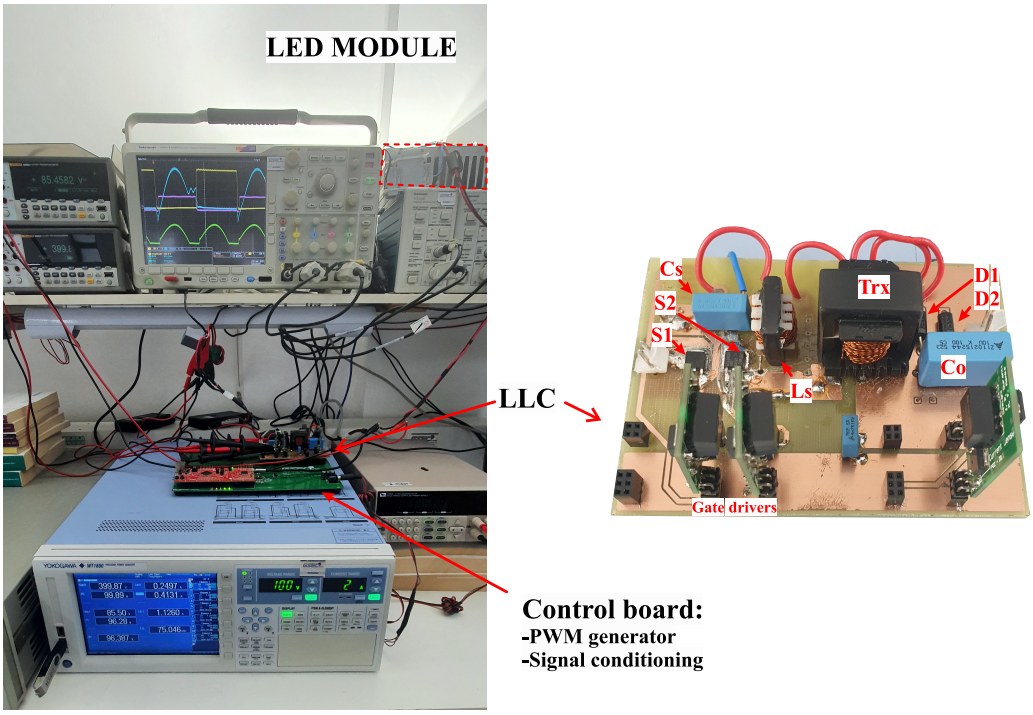
F$_i$	η_{rank}	$Min[t_{Dwin} - t_{dis}]$ 360 V	420 V	ZVS	$Max[t_{dis}]$ (ns)	f_{min} (kHz)	f_{max} (kHz)	Δf_{sw} (kHz)	**Trx**	L_S	V_{CsRMS} (V)	$Max[i_R]$ (A)
104	0.955	409	532	YES	338	68.7	100.3	31.6	EE.30/15/14	EE.20/10/5	237	0.667
43	0.928	1110	1098	YES	201	89.3	125.3	36.0	EE.30/15/14	EE.20/10/5	231	0.823
121	0.865	2204	2119	YES	61	86.0	102.7	16.7	EE.40/17/12	EE.25/10/6	250	1.88

time spent to compute the second script is less than 1 minute, since only data are analyzed and simple calculations performed.

5.4 EXPERIMENTAL RESULTS

Experimental results are presented in this section to verify the proposed design procedure of the LLC resonant LED driver. Table 12 presents the employed parameters, which are related to filter F_{104}. The laboratory prototype is shown in Fig. 78. In the experimental verification, the ZVS condition is initially evaluated. In the sequence, the f_{sw} range required to maintain output controlled is analyzed. Afterward, the converter efficiency is measured and compared to the classical design one. Finally, additional results are presented to show further aspects of the designed converter.

Figure 78 – Photograph of the laboratory prototype



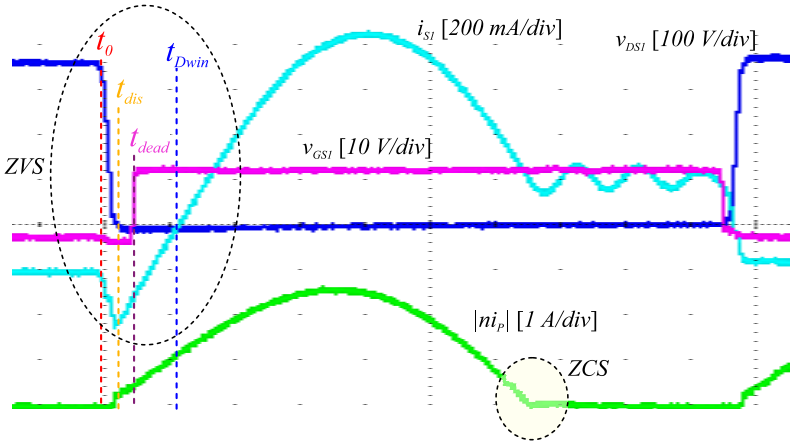
Source: Author.

5.4.0.1 ZVS constraint evaluation

To achieve true ZVS it is mandatory to address the constraints given in (5.4), which states that $t_{dis} \leq t_{dead} \leq t_{Dwin}$ and $i_{DS1.on} = i_{DS1}(t_0) \leq 0$. Therefore, in order to evaluate these conditions experimentally, Fig. 79 shows HB inverter and output rectifier main waveforms during the operation at minimum input voltage ($V_{IN} = 360\ V$) and nominal output current ($I_O = 1.15\ A$), which correspond to the worst scenario to achieve ZVS (see Fig. 71). Analyzing Fig. 79, it can be seen that the ZVS constraints are respected, since $t_{dis} \leq t_{dead} \leq t_{Dwin}$. Furthermore, the ZCS condition for the diodes in the output rectifier is also evident in Fig. 79.

During the final filter selection, it is recommended to consider a conservative margin under (5.4.a) evaluation. Several issues affect this condition, for instance, C_{DS} are nonlinear capacitors, and their value is a function of the drain-to-source voltage. Furthermore, at the resonant tank input point, the total capacitance is the sum of the output MOSFET capacitors C_{DS} and the parasitic capacitance C_{stray} of the power MOSFET cases, the heat sink, the intra-winding capacitance of the resonant inductor, etc. On the other hand, MOSFETs and gate-driver turn-off and turn-on delay also impact this constraint assessment.

Figure 79 – ZVS assessment for the LLC resonant filter F_{104} operating at minimum input voltage $V_{IN} = 360\ V$ and nominal output current $I_O = 1.15\ A$.

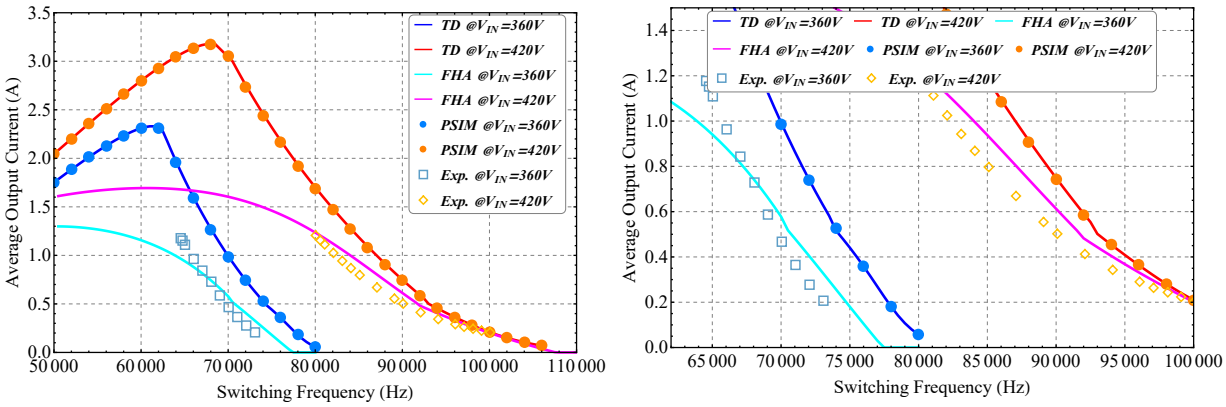


Source: Author

5.4.0.2 Switching frequency range

The f_{sw} range required by the filter F_{104} to maintain the output current controlled over the wide input voltage range and load variation is shown in Fig. 80. In this figure, experimental results are presented simultaneously with simulation results, and the the results predicted by FHA and the proposed TD procedure. As it can be seen, comparing experimental with TD, there is a difference between the results given by an almost constant value, which shifts the curves. However, the both experimental and TD curve presents the same inclination or tendency, which can not be observed in the results predicted by the FHA approach. The error between

Figure 80 – Experimental (Exp), simulation (PSIM), time-domain (TD), and FHA results for the LLC resonant filter F_{104} current gain as a function of the f_{sw}: Left-trace: Wide switching frequency range; Right-trace: Zoom in the operational range.



Source: Author

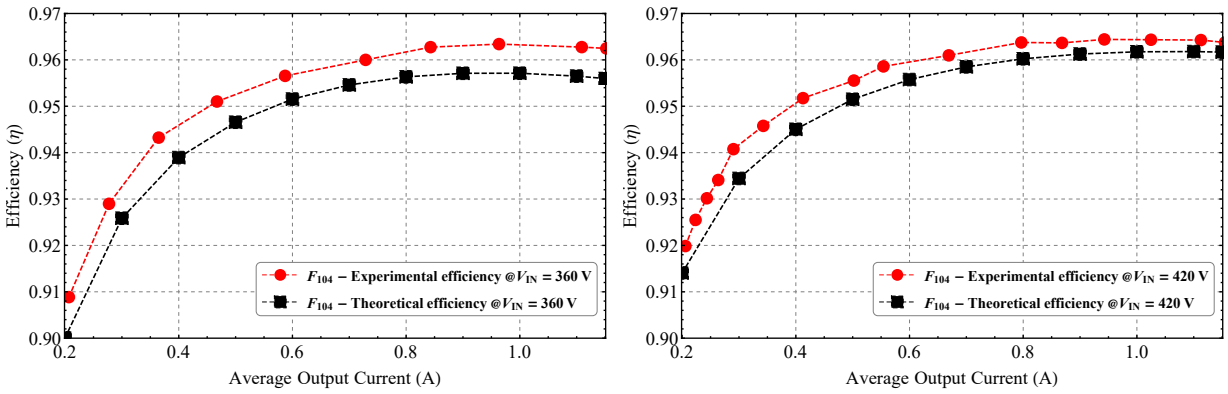
experimental and TD based results are given by parasitic components, neglected in the TD analysis, as well as the elements tolerance.

From the converter design perspective, the selected filter F_{104} requires a small f_{sw} range, easily achieved by commercial gate-driver dedicated integrated circuits. In addition, it can be noted that the operation is below the main resonance of the LLC resonant tank, which is expected due to the employed transformer turns ratio.

5.4.0.3 Efficiency curve evaluation

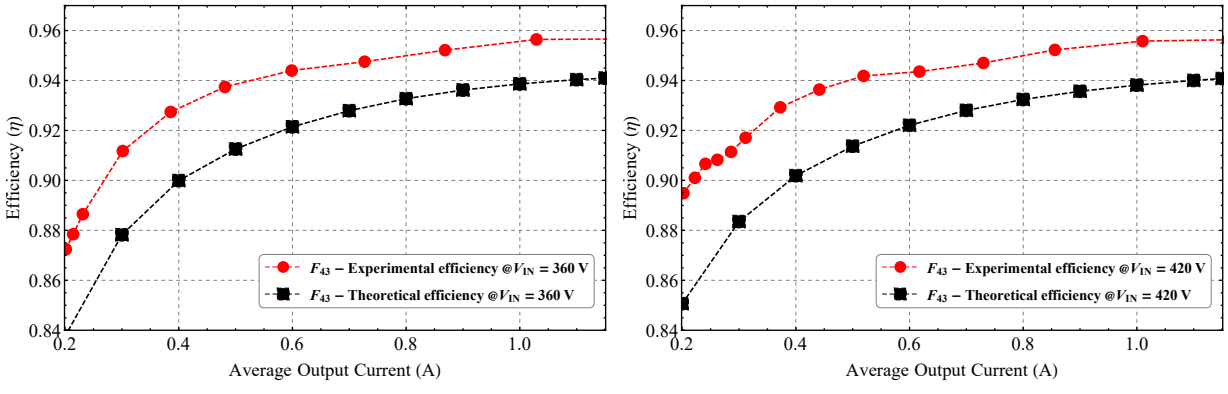
Fig. 81 shows the experimental and theoretical efficiency comparison for the LLC resonant filter F_{104} operating at different V_{IN} an under LED current variation to perform dimming. The peak efficiency of 96.44% is achieved when $V_{IN} = 420\ V$ and $I_O = 0.94\ A$. The

Figure 81 – Experimental and theoretical efficiency comparison for the LLC resonant filter F_{104} operating at different V_{IN} and load conditions; Left-trace: $V_{IN} = 360\ V$; Right-trace: $V_{IN} = 420\ V$.



Source: Author.

Figure 82 – Experimental and theoretical efficiency comparison for the LLC resonant filter F_{43} operating at different V_{IN} and load conditions; Left-trace:$V_{IN} = 360\ V$; Right-trace: $V_{IN} = 420\ V$.



Source: Author.

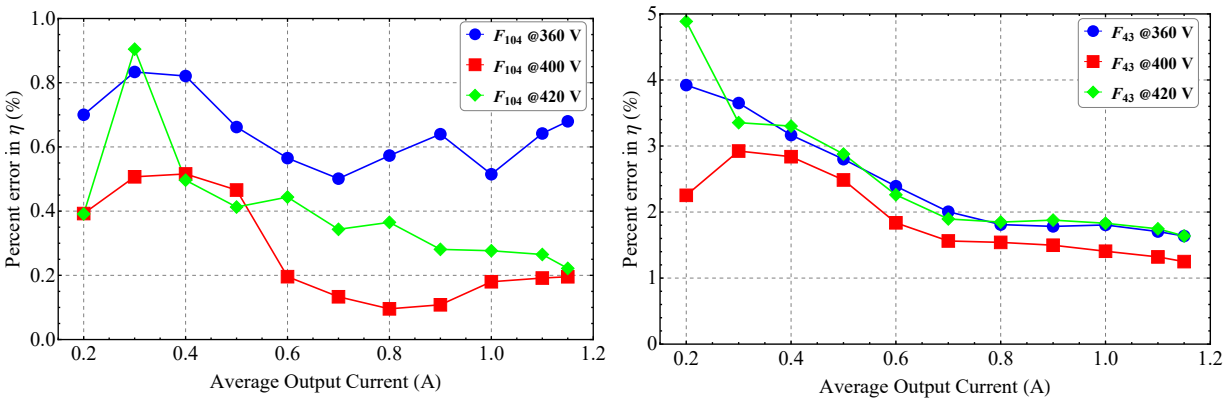
minimal efficiency of 90.88% is achieved when $V_{IN} = 360\ V$ and $I_O = 0.20\ A$. Similarly, Fig. 82 shows the same analysis for the LLC resonant filter F_{43}. The peak efficiency of 95.66% is achieved when $V_{IN} = 360\ V$ and $I_O = 1.15\ A$. The minimal efficiency of 87.24% is achieved when $V_{IN} = 360\ V$ and $I_O = 0.20\ A$. Thus, employing the proposed design procedure, higher peak efficiency and higher minimum efficiency are achieved. It is worth to mention, that in both cases the auxiliary voltage sources and gate-driver power loss are not included.

To verify the accuracy of the estimated efficiency, Fig. 83 shows the percent error ($\varepsilon_\eta\%$) in predicting the efficiency for filter F_{104} and F_{43}. As can be seen, the error is less than 1% for filter F_{104}, and less than 5% for filter F_{43}. For the sake of clarity, $\varepsilon_\eta\%$ is computed by $\varepsilon_\eta\% = |Experimental - Theoretical|/Experimental$. The precision power analyzer, model WT1800 from Yokogawa, is employed to obtain the experimental results. However, it should be carried in mind that the experimental measurement presents uncertainties, which are omitted in this analysis. Theses uncertainties in addition to the low power level can explain the $\varepsilon_\eta\%$ for F_{104} at $I_{LED} = 0.3\ A$ which does not follows the tendency.

Finally, Fig. 84 shows the experimental efficiency of the proposed design F_{104} and classical design F_{43} operating at different V_{IN}. As it can be seen, F_{104} presents a higher efficiency over the whole operating range in comparison to F_{43}. To highlight this outcome, Fig. 84(d) presents the efficiency gain when F_{104} is employed. As it can be seen, for low power levels, the efficiency can be increased up to 4.3%, and about 1% around the converter rated power.

Advancing with the evaluation of the proposed design, Fig. 85 shows the theoretical power loss in the LLC resonant converter. As can be seen, the proposed design's power loss is diminished compared to the classical design. Furthermore, it can be seen that for both designs, the more considerable power loss occurs in the transformer and inductor core, rectifier diodes, and HB switching. Therefore, to further improve the converter efficiency, it goes over selecting

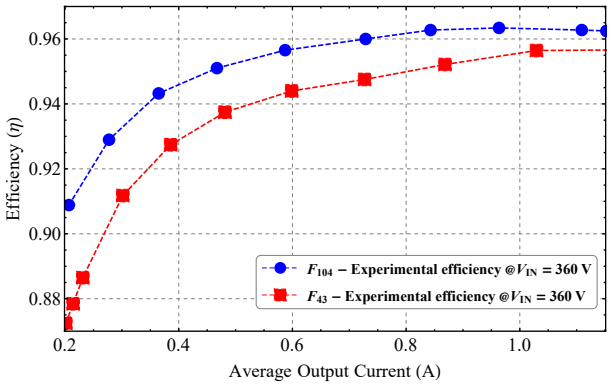
Figure 83 – Percent error in predicting the LLC filter efficiency. Left-trace: F_{104}; Right-trace: F_{43}.



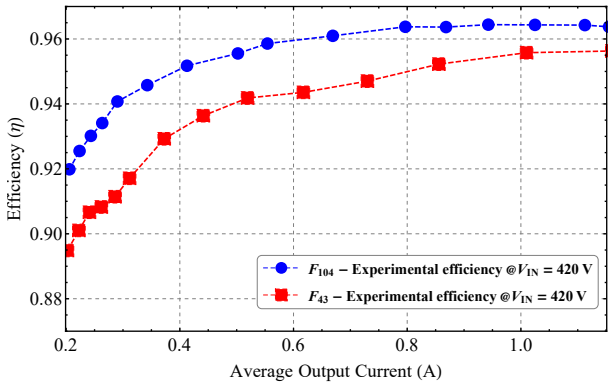
Source: Author.

Figure 84 – Experimental efficiency comparison between proposed (F_{104}) and classical (F_{43}) designs.

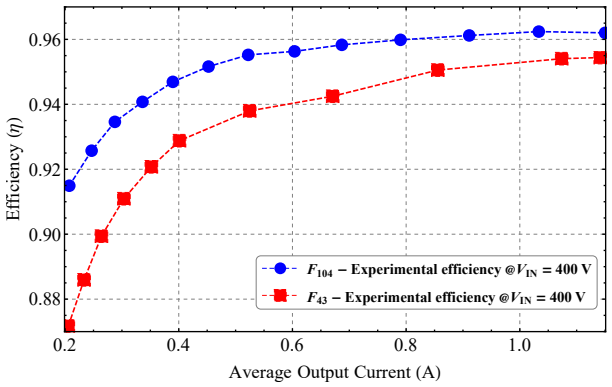
(a) – $V_{IN} = 360\ V$



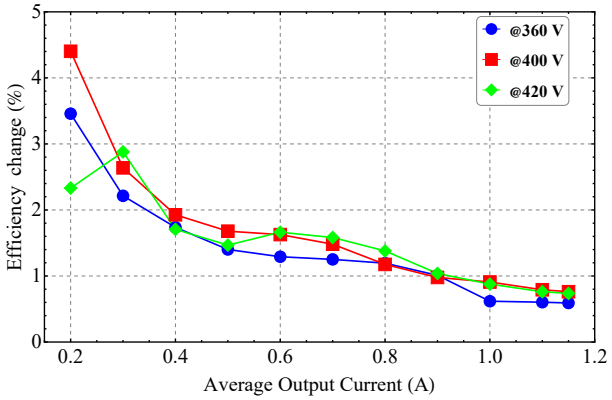
(b) – $V_{IN} = 420\ V$



(c) – $V_{IN} = 400\ V$



(d) – F_{104} efficiency gain in comparison to F_{43}.

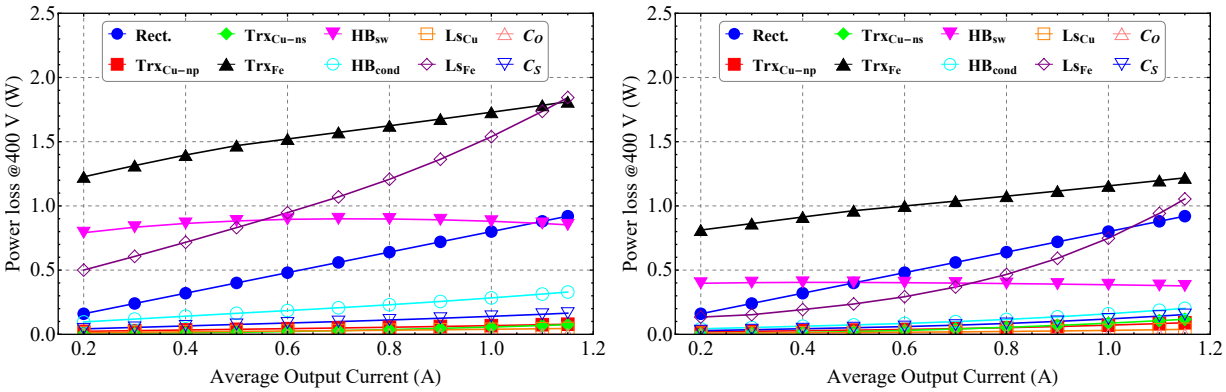


Source: Author.

magnetic core materials with reduced volumetric losses, synchronous rectifier employment, and reduction of switching loss.

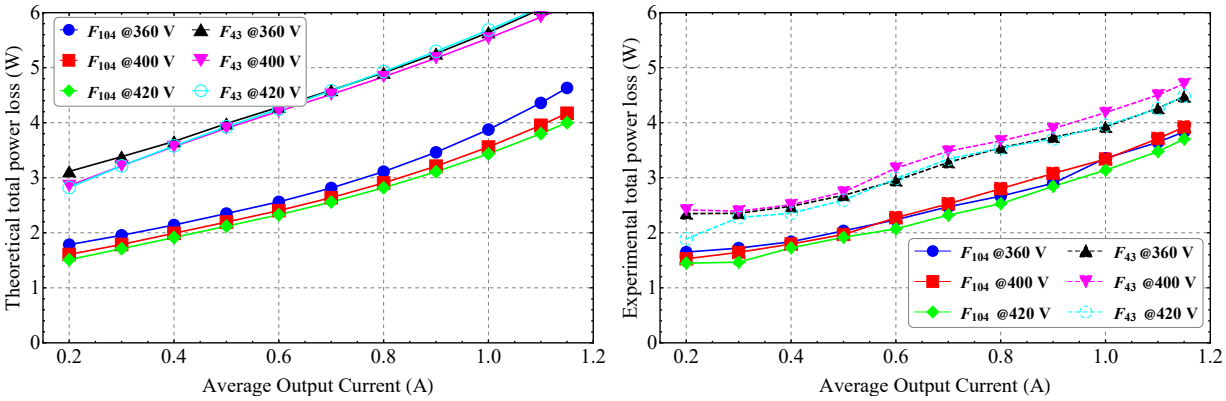
To finish the efficiency and power loss analysis, Fig. 86 shows the total power for the LLC resonant LED driver, wherein theoretical and experimental results are presented for filters F_{104} and F_{43}. Complementing, Fig. 87 shows the percent error in predicting the converter total power loss. As can be seen, the error in predicting the total power loss is significant. The error is considerable since the involved values are low, so mili Watts of difference corresponds to some units and even a dozen for the percent error. Nevertheless, it reveals one issue of the proposed design procedure.

Figure 85 – Theoretical power loss in the LLC resonant converter at $V_{IN} = 400\ V$; Left-trace:Classical design - Filter F_{43}; Right-trace: Proposed design - Filter F_{104}.



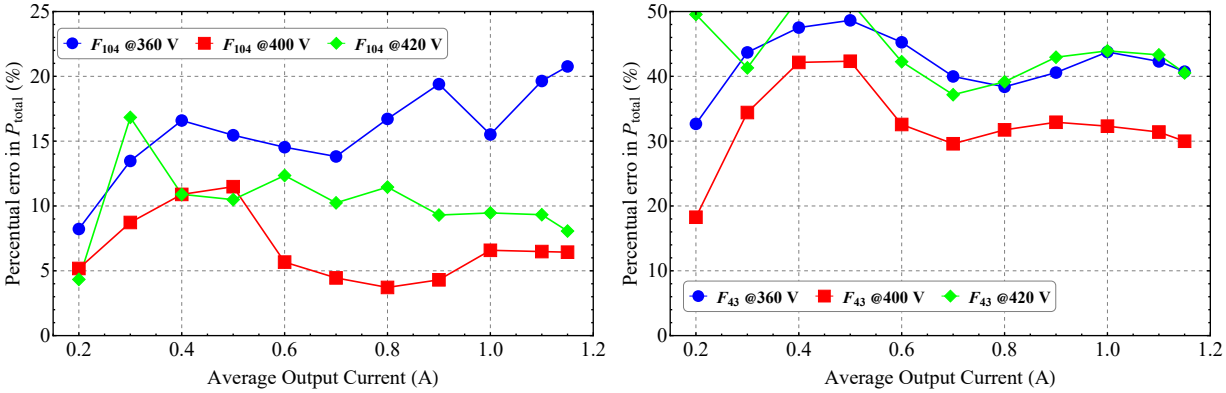
Source: Author.

Figure 86 – Comparison between theoretical and experimental total power loss in the LLC resonant converter; Left-trace: Theoretical results; Right-trace: Experimental results.



Source: Author.

Figure 87 – Error in predicting the LLC converter total power loss; Left-trace: F_{104}; Right-trace: F_{43}.

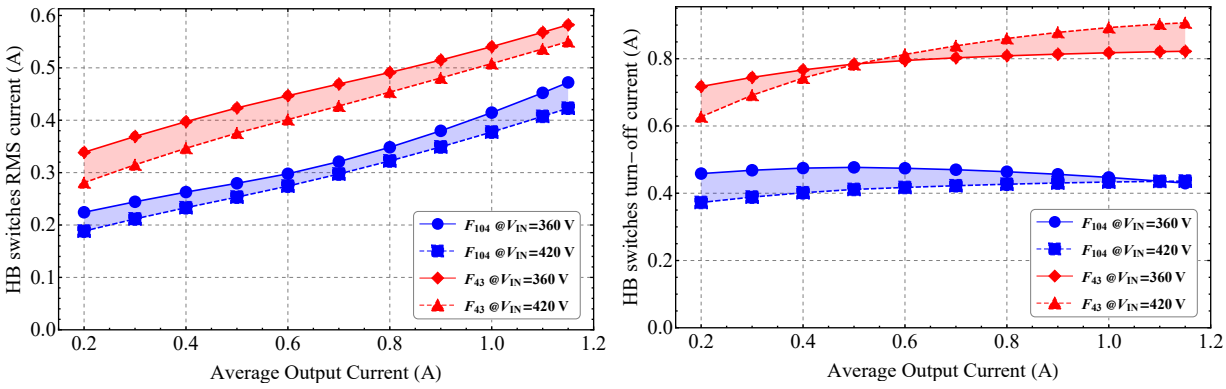


Source: Author.

5.4.1 Current stress analysis

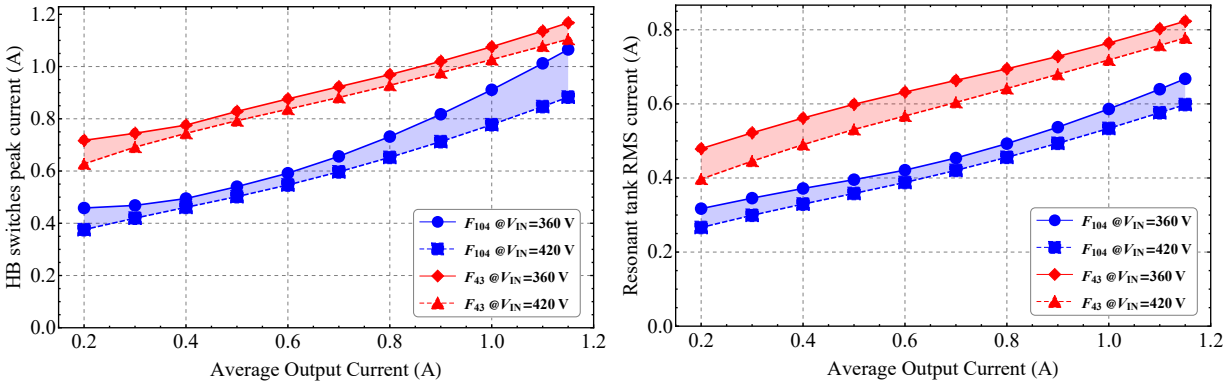
Fig. 88 shows the HB switches RMS ($i_{S1.RMS}$) and turn-off current ($i_{S1.off}$) for F_{104} and F_{43}. This comparison considers the extreme input voltage and the output current variation range. Besides, Fig. 89 presents the HB switches peak current ($i_{S1.pk}$) and the resonant tank RMS current ($i_{R.RMS}$). As can be seen in these results, the filter F_{104} (proposed design) presents a reduced current in comparison to the filter F_{43} (classical design). These reduced currents justify why the proposed design presents higher efficiencies in comparison to the classical design. Nevertheless, using only the current levels to guide the design is not suitable since several other parameters directly (or indirectly) affect the LLC converter performance.

Figure 88 – Proposed and classical design Half-bridge switches current comparison; Left-trace: HB swiches RMS current; Right-trace: Half-bridge switches turn-off current.



Source: Author.

Figure 89 – Proposed and classical design current comparison; Left-trace: HB switches RMS current; Rigt-trace: Resonant tank RMS current.

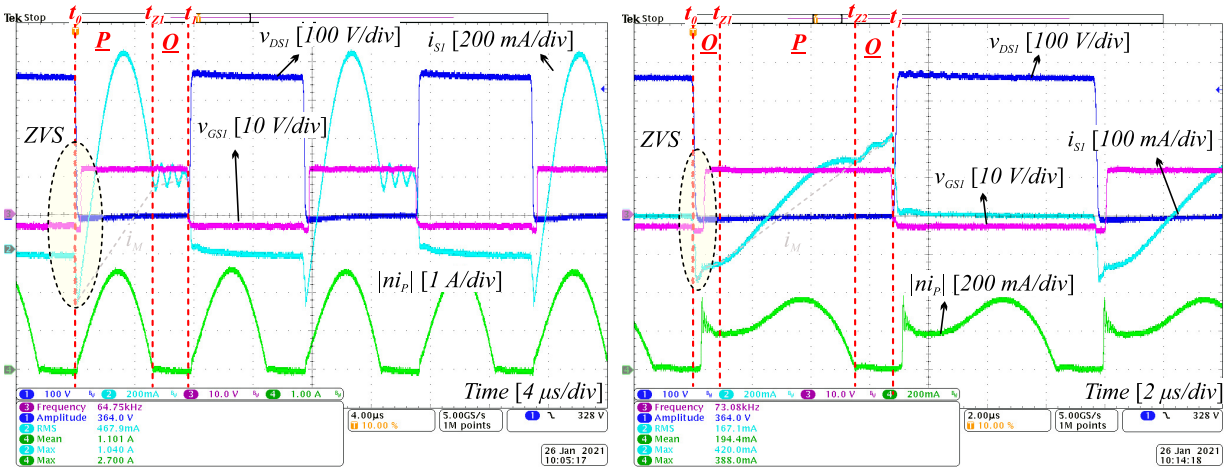


Source: Author.

5.4.2 Experimental waveforms

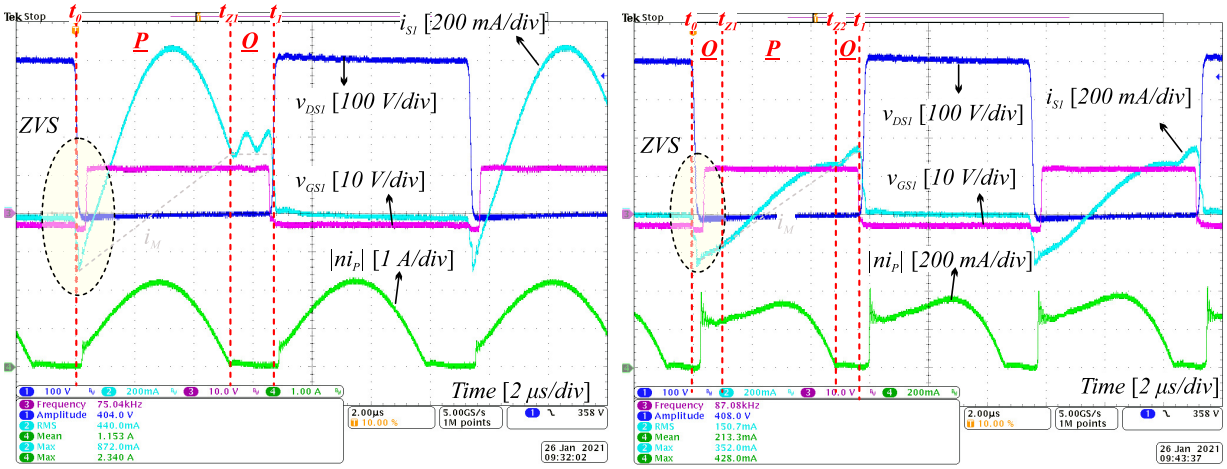
Experimental waveforms are now presented to evaluate the converter operation modes and further assess the ZVS and ZCS. Table 14 present the LLC filter F_{104} operation modes and f_{sw} for the minimum, nominal, and maximum V_{INS} as well as for the minimum and maximum I_{LED}. Fig. 90 shows the LLC resonant LED driver main waveform necessary to evaluate the operation mode and switching conditions at $V_{IN} = 360\ V$. As can be seen, for the nominal LED current, the converter operates at PO mode. At minimum output current, the OPO mode

Figure 90 – F_{104} LLC resonant LED driver main waveform for the operation at $V_{IN} = 360\ V$ and extreme output current conditions. Left-trace: $I_O = 1.15\ A$; Right-trace: $I_O = 0.2\ A$.



Source: Author.

Figure 91 – F_{104} LLC resonant LED driver main waveform for the operation at $V_{IN} = 400\ V$ and extreme output current conditions. Left-trace: $I_O = 1.15\ A$; Right-trace: $I_O = 0.2\ A$.

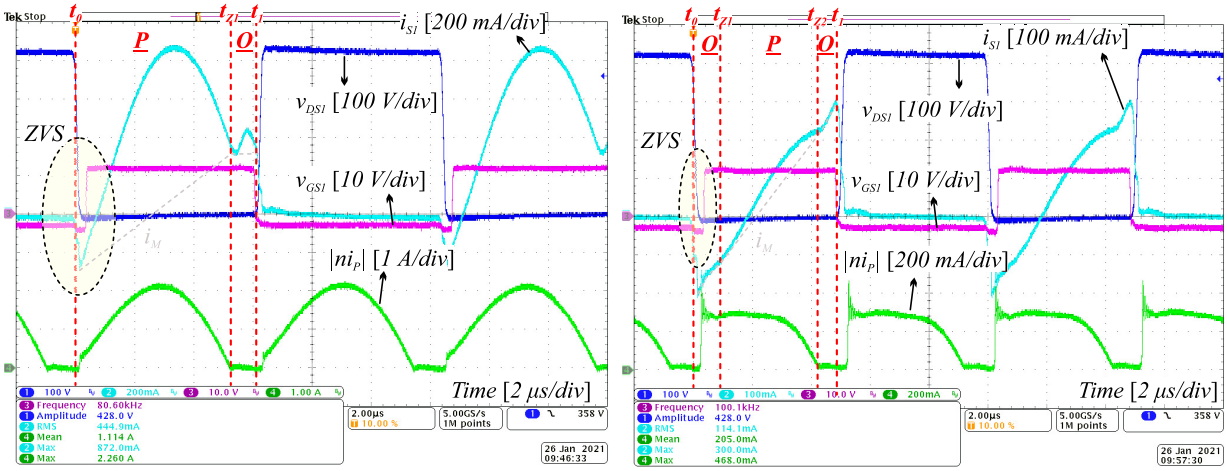


Source: Author.

Table 14 – Operation modes and f_{sw} for the LLC resonant converter filter F_{104}

I_O	$V_{IN} = 360\ V$		$V_{IN} = 400\ V$		$V_{IN} = 420\ V$	
	Mode	$f_{sw}\ (kHz)$	Mode	$f_{sw}\ (kHz)$	Mode	$f_{sw}\ (kHz)$
0.2	OPO	77.7	OPO	90.8	OPO	100.3
1.15	PO	68.7	PO	78.9	PO	85.3

Figure 92 – F_{104} LLC resonant LED driver main waveform for the operation at $V_{IN} = 420\ V$ and extreme output current conditions. Left-trace: $I_O = 1.15\ A$; Right-trace: $I_O = 0.2\ A$.



Source: Author.

is noticed. Furthermore, ZVS conditions and ZCS is achieved for these two load conditions. These same results are observable for the operation at nominal and maximum input voltage, as shown respectively in Fig. 91 and Fig. 92.

5.5 SUMMARY

With the LLC LED driver faithfully solved in the TD, a new design procedure was proposed in this chapter. Given an initial set of filters, the proposed design procedures carefully analyze several features to select the optimal solution from this set.

Initially, the LLC filters in the set are solved in the TD, considering a variable input voltage and a wide output current change required to perform dimming. Afterward, the discrete components for each filter are designed for the critical operation point. In the sequence, the efficiency for each filter is estimated. Then, employing the weighted-average-efficiency concept, the filters are classified. Finally, the filter with the highest efficiency that does not infringe the imposed constraint is selected as the designed one. These constraints ensure ZVS for the HB switches, ZCS for the output rectifier, feasible switching frequency range Δf_{sw}, and enough gain peak to keep under control the output

current over the whole operating window while maintaining a good efficiency without compromising the converter power density.

Experimental results verify the proposed design procedure. The selected filter maintained the ZVS, and ZCS conditions over the whole operating range. Feasible switching frequency range (30 kHz) is also noticed. Besides, high efficiency is noticed over the wide operating range. The peak efficiency of 96.44% is achieved. In comparison to the classical design, the efficiency is improved up to 4.3%.

From a macro point of view, the design procedures present interesting features since an improved performance is achieved compared to the classical design. Besides, several features are known in the design stage. Compared to the classical design, the proposed design should be employed when the LLC resonant LED driver is subjected to a wide operation range, which includes dimming and input voltage variations. For a LLC resonant LED driver without dimming, subjected to a constant input voltage, and operating at series resonance, the classical design procedure outcome in a satisfactory design. Regarding the proposed design, its disadvantage is given by its complexity since it follows several steps, including the LLC time-domain analysis.

6 PI&APDR CONTROLLER

Due to the LLC resonant LED driver small-signal modeling limitations when the converter is subjected to a wide operation range, the employment of a single conventional controllers cannot achieve the required performance at all operating conditions. To overcome this issues, in this chapter a new hybrid robust controller is proposed. Taking advantage of the dual-loop structure, the proposed control system outer loop employs a Proportional-Integral (PI) controller, and the inner loop implements an adaptive periodic disturbance rejection (APDR) subsystem, conceiving the PI&APDR controller. The PI subsystem is designed to maintain the average LED current regulated at the reference value, which depends on the desired output dimming. On the other hand, the APDR subsystem is designed to strictly reject the bus voltage ripple and limit its transmission to the LED current and voltage. Experimental results show the proposed controller feasibility in achieving good tracking behavior, reduced output current ripple, robustness against parametric variations, and simple implementation and design. For the sake of completeness, the proposed PI&APDR is compared with the conventional proportional resonant controller employing experimental results and extra analysis based on simulations.

6.1 INTRODUCTION

Owing to the LED output light direct relationship with its forward current and voltage source electrical behavior, combined with the necessity to present a regulated average current value to perform dimming and reduced current ripple to avoid flicker (IEEE STD 1789, 2015), the LED driver has to be carefully designed as an current-controlled system to properly supply an LED load (SCHRATZ ET AL., 2016).

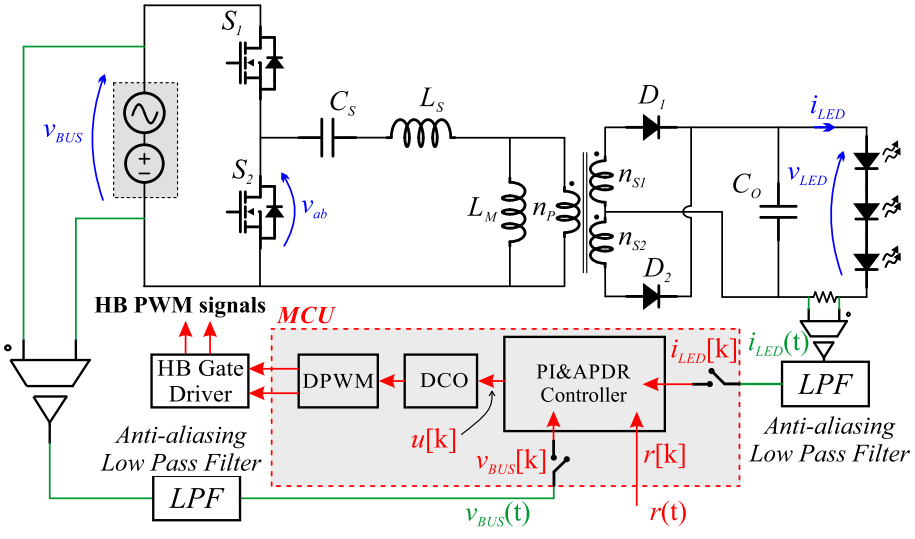
Among classical controllers, it is well-known that the PI controller presents both simplicity and a prominent capability in tracking a DC reference, but a limited loop gain at different frequencies diminish its capacity of rejecting periodic disturbances (ERICKSON ET AL., 2001). On the other hand, adaptive controllers as well as adaptive periodic disturbance rejection (APDR) controllers have strong robustness against different disturbances and unmodelled dynamics at the expense of being a more complex system (IOANNOU E TSAKALIS, 1986), (W. KIM ET AL., 2011). Therefore, combining the advantages of both PI

and APDR controllers, this chapter presents a new hybrid dual-loop controller, namely PI&APDR control, proper for offline LED drivers where a low output current ripple (ΔI_{LED}) and DC regulation is required. The outer loop employing PI controller is responsible for regulating the average LED current (I_{LED}) over a wide operating range and for dictating the transient performance of the whole system. The inner loop subsystem employs an APDR controller being strictly responsible for attenuating ΔI_{LED} regardless of the bus voltage ripple ΔV_{BUS} amplitude and frequency. However, seeking a solution that presents robustness at the same time that preserves simplicity, the APDR subsystem is simplified as much as possible, making it possible to be implemented with a low-cost MCU.

6.2 PROPOSED HYBRID CONTROLLER ANALYSIS

Fig. 93 shows the LLC resonant converter circuit diagram with a high-level representation of the proposed control system, operating as a downstream DC/DC converter in a two independent stage LED driver. As can be seen, the control system is digitally-implemented employing a microcontroller (MCU). The instantaneous LED current $i_{LED}(t)$, and bus voltage $v_{BUS}(t)$ are sampled by the MCU and fed into the PI&APDR controller, being the desired I_{LED} defined by the reference $r[k]$. Inside the MCU, control action $u[k]$ throughout the digitally controlled oscillator (DCO) and digital PWM (DPWM) module determine the modulated HB f_{sw}, which signal feeds the HB gate-driver. Besides, compared to classical solutions, no additional sensors are necessary to implement the PI&APDR controller, because v_{BUS} is usually measured to perform the PFC stage control. Finally, as can be seen in Fig. 93, the PFC stage is not here implemented, being $v_{BUS}(t)$ emulated by a voltage source.

Figure 93 – Circuit diagram of the LLC converter implementing the DC/DC stage of an LED driver.



Source: Author.

Fig. 94 shows the proposed PI&APDR controller scheme, which is based on a dual-loop control structure. The outer loop employing a PI controller is responsible for regulating the average LED current over a wide operating range and for dictating the whole system's transient performance. Besides, the PI is accountable for ensuring robustness against parametric variations. The inner loop, adopting a simplified adaptive controller, is strictly responsible for attenuating ΔI_{LED} regardless of ΔV_{BUS} amplitude and frequency $f_{\Delta V}$. Differing from the conventional dual-loop, where the outer loop usually sets up the reference for the inner loop, in the proposed PI&APDR, each loop produces a control action aiming to carry out its task. So, two decoupled components made up the LLC converter control action $u[k]$, the PI component $u_{PI}[k]$ and the APDR one $u_{APDR}[k]$.

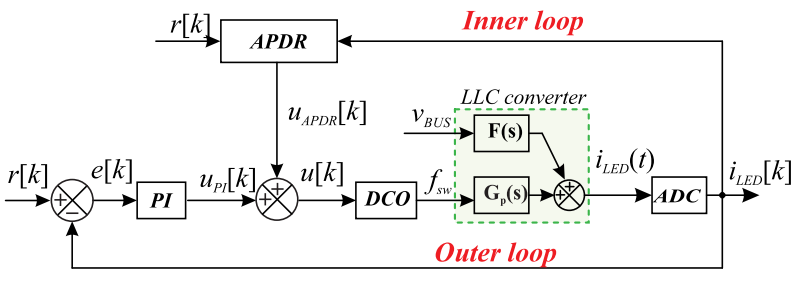
During the offline LED driver operation, the LLC resonant converter shown in Fig. 93 is subjected to parametric variations (V_{BUS}, and filter components), periodic bus voltage disturbance which is given by ΔV_{BUS}, and load variation due to the amplitude modulation (AM) dimming. Besides, for an LED driver with universal input voltage, ΔV_{BUS} frequency ranges between $100-120\,Hz$. In this way, considering the internal model principle (IMP) that establishes that the controller should include a model of the disturbance, it can be stated that the control action $u[k]$ required by the LLC converter to track the output DC reference and reject ΔV_{BUS} as well as reject parametric variations, will present a DC component summed to a periodic signal with the same frequency of the disturbance. Therefore, assuming a sinusoidal periodic disturbance, in steady-state discrete time $u[k]$ is given by

$$u[k] = A + B\sin(2\pi f_{\Delta V} k T_s + \phi) \tag{6.1}$$

where $f_{\Delta V}$ is the v_{BUS} ripple frequency, T_s the discrete control system period, and A and B are constant values.

Taking into account the classical control theory, the derived proportional resonant (PR), PIR, and IQR controllers are capable of generating the signal given by (6.1). On the other hand, translated into frequency domain analysis of the loop gain $T(s)$, the Bode Diagram for PR, PIR, or IQR compensated loop-gain $T(s)$ presents a high DC gain and a high gain (>30 dB) around $f_{\Delta V}$. Phase and gain margins and the crossover frequency are adjusted to achieve

Figure 94 – Proposed hybrid dual-loop based control scheme for LLC resonant converter.



Source: Author.

an acceptable dynamic performance. Unfortunately, as it will be shown, one single linear PR, PIR or IQR controller designed to accomplish these guidelines will present a poor performance when the converter is subjected to a wide operating range. The performance is even worse when parametric variations are taking into account. In fact, considering the resonant based controllers, there is a trade-off between stability margin gains and ripple current rejection for $f_{\Delta V}$ variation, where a better current ripple rejection results in a smaller phase margin and vice-versa (C. LIU ET AL., 2015). Besides, it is impossible to overcome this issue in the design step due to the limitations of the small-signal models for the LLC converter considering operation beyond the series resonance (Z. FANG, J. WANG ET AL., 2018). Notwithstanding, it should be noted that the expression given by (6.1) remains valid. The problem is due to the difficulty of linear controllers to properly generate the signal in (6.1).

However, employing the proposed PI&APDR controller to generate (6.1), an enhanced controlled current can be achieved, since the DC reference tracking is decoupled from the ripple attenuation action, allowing each loop to be optimized in terms of robustness and performance. Thus, the DC tracking decoupling from periodic disturbance rejection, together with the PI and APDR subsystems analysis and design, is highlighted as the main contribution of this proposal.

The procedure of decoupling the controller functions, as well as the employment of dual-loop structures, are not new in the literature. However, as far as the author know, no reported proposal presents a hybrid dual-loop employing PI and a simplified adaptive controller for enhanced robust DC regulation and periodic disturbance rejection.

6.2.1 PI controller subsystem analysis and design guidelines

For the outer loop analysis and design, the inner loop can be omitted because it can be assumed that it is fully functional in rejecting ΔV_{BUS} and does not affect the DC regulation. Hence, the outer loop is designed following the classical frequency-response method, which is based on the analysis of the compensated loop gain $T(s)$.

To track i_{LED} DC reference in the LLC resonant LED driver, as well as to reject dynamic and parametric variations, and so theoretically achieve zero steady-state error, a PI controller will be employed. The PI compensated loop gain can be easily adjusted to present mathematically infinite DC gain and increased phase and gain margins. High gain and phase margins improve the controller robustness against the converter dynamic and parametric variation. The mentioned dynamic variation can occur due to parametric variations and also because of the converter wide operating range to supply the LED load with different current levels to perform dimming. Besides, this dynamic variation is also affected by the resonant converter strong non-linearity, highlighting the necessity of a robust system. On the other hand, since the PI is not responsible for compensating the periodic bus voltage disturbance at $f_{\Delta V}$ frequency, no requirements are imposed to the PI compensated loop gain around $f_{\Delta V}$.

Taking into account the IMP and considering the reference and parametric variation as step signals, the outer loop control action will be then a DC signal under steady-state operation, providing the DC term in (6.1). Besides, to avoid interaction with the inner loop, the PI compensated loop gain has to present a crossover frequency below $f_{\Delta V}$, which demands a low gain at $f_{\Delta V}$. These design guidelines will stamp to the outer loop a dynamic that follows a first-order behavior avoiding electrical stress in the LED load that otherwise could be caused by overshooting. In order to elucidate the outer loop design, further details are presented in next section.

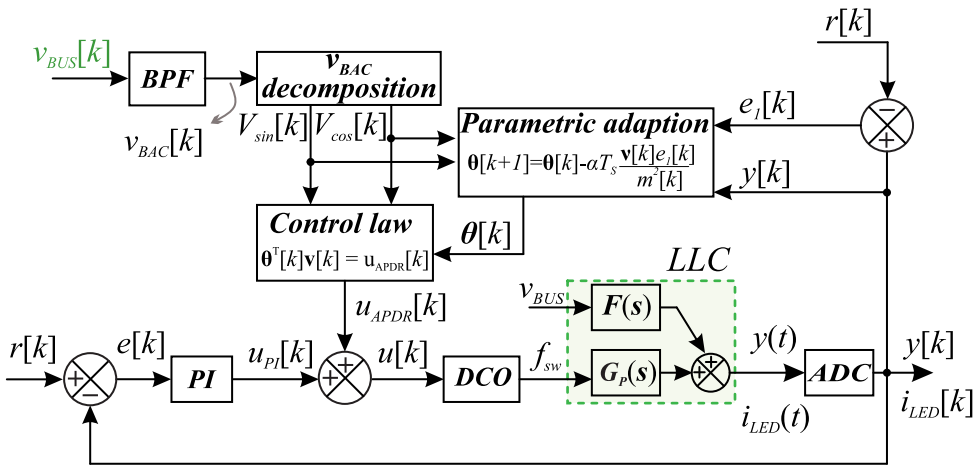
6.2.2 APDR subsystem analysis and design guidelines

Fig. 95 shows the detailed block diagram of the proposed PI&APDR controller; further details of the APDR subsystem will be described later in this section. As aforementioned, the inner loop (APDR) is strictly responsible for the periodic ΔV_{BUS} disturbance rejection. Assuming a sinusoidal ΔV_{BUS}, it is known from the IMP that a sinusoidal component should appear at the control action to reject this disturbance. Indeed, the inner loop function is intended to generate this sinusoidal component. Nevertheless, since the ΔV_{BUS} can present different frequencies due to the universal input voltage, different amplitude depending on PFC topology and output power, and its rejection also depends on the LLC converter dynamic, a versatile and robust inner loop must be developed. To tackle this task, a robust APDR controller is proposed to implement the inner loop.

Therefore, under steady-state operation, the inner loop has to generate a control action given by (6.2). Alternatively, $u_{APDR}[k]$ in (6.2) can be rewritten by (6.3).

$$u_{APDR}[k] = B\sin(2\pi f_{\Delta V} k T_S + \phi). \tag{6.2}$$

Figure 95 – Detailed scheme of the proposed PI&APDR controller for LLC resonant converter.



Source: Author.

$$u_{APDR}[k] = \theta_{\sin}[k]V_{\sin}[k] + \theta_{\cos}[k]V_{\cos}[k]. \tag{6.3}$$

Where $V_{\sin}[k] = V_s \sin(2\pi f_{\Delta V} k T_s)$ and $V_{\cos}[k] = V_c \cos(2\pi f_{\Delta V} k T_s)$ are respectively sine and cosine signals with frequency $f_{\Delta V}$, and V_s and V_c amplitudes; and, $\theta_{\sin}[k]$ and $\theta_{\cos}[k]$ are constant values under steady-state operation, which will define B and phase ϕ of $u_{APDR}[k]$ in (6.2).

Defining the vectors in (6.4), the control action can rewritten by (6.5).

$$\boldsymbol{\theta}^T[k] = \begin{bmatrix} \theta_{\sin}[k] & \theta_{\cos}[k] \end{bmatrix} \tag{6.4a}$$

$$\boldsymbol{v}^T[k] = \begin{bmatrix} V_{\sin}[k] & V_{\cos}[k] \end{bmatrix} \tag{6.4b}$$

$$u_{APDR}[k] = \boldsymbol{\theta}^T[k]\boldsymbol{v}[k] \tag{6.5}$$

Since $u_{APDR}[k]$ and ΔV_{BUS} must have the same frequency $f_{\Delta V}$, and being the frequency of $u_{APDR}[k]$ function of $V_{\sin}[k]$ and $V_{\cos}[k]$, it is reasonable to derive these sine and cosine signals from v_{BUS}. Therefore, as can be seen in Fig. 95 the sampled $v_{BUS}[k]$ signal is filtered by a digital band pass filter (BPF) with the aim to extract the sinusoidal fundamental AC component ($v_{BAC}[k]$) from ΔV_{BUS}. Following, $v_{BAC}[k]$ is then defined as the sinusoidal component ($V_{sin}[k]$) and its signal in quadrature ($V_{cos}[k]$) is obtained from its differentiation. With $V_{\sin}[k]$ and $V_{\cos}[k]$ known, the required control action $u_{APDR}[k]$ to reject periodic bus voltage disturbance can be defined by properly determining $\theta_{\sin}[k]$ and $\theta_{\cos}[k]$. Actually, $\theta_{\sin}[k]$ and $\theta_{\cos}[k]$ correspond to the automatic adapted parameters of the APDR subsystem.

At this point, it is necessary to define how these adapted parameter are determined. To tackle this task, employing the Lyapunov stability theory, a gradient automatic parameter estimation algorithm is designed due to its simplicity (IOANNOU AND TSAKALIS, 1986), (IOANNOU AND SUN, 2012), given by

$$\boldsymbol{\theta}[k+1] = \boldsymbol{\theta}[k] - \frac{\alpha T_s \boldsymbol{v}[k] e_1[k]}{m^2[k]} \tag{6.6}$$

Where α is a design constant, that dictates the automatic parameters adaptation speed, and so consequently the transient time for the periodic disturbance rejection; $e_1[k] = y[k] - r[k]$ is the APDR tracking error, wherein $y[k]$ is the measured LED current $i_{LED}[k]$, and $r[k]$ the I_{LED} reference; and, $m^2[k]$ is a function used to add robustness to the APDR controller.

The function $m^2[k]$ is expressed by (6.7), whose outcome is always ≥ 1. The main purpose of $m^2[k]$ is to stop the sharp variation of $\boldsymbol{\theta}$ due to abrupt changes in $u_{APDR}[k]$, $y[k]$ or $\boldsymbol{v}[k]$, thus adding robustness to the APDR subsystem (IOANNOU AND TSAKALIS, 1986), (IOANNOU AND SUN, 2012).

$$m^2[k] = 1 + u_{APDR}^2[k] + y^2[k] + \boldsymbol{v}^T[k]\boldsymbol{v}[k] \tag{6.7}$$

Being $\theta_{\sin}[k]$ and $\theta_{\cos}[k]$ defined, the control action $u_{APDR}[k]$ is easily determined computing (6.5). Summarizing the APDR subsystem operation, $v_{BUS}[k]$ is filtered by a BPF to define $V_{sin}[k]$, where by derivation $V_{cos}[k]$ is obtained. In sequence, the automatic adapted parameters are calculated to generate the required AC component of the LLC control action to eliminate the tracking error e_1.

Regarding the APDR subsystem design, it must be highlighted that the inner loop design corresponds precisely to the definition of α constant, emphasizing its simple design. The BPF parameters, and the v_{BAC} decomposition algorithm, are the same regardless of the switched converter topology used in the PFC stage. Besides, it can be noticed that the proposed controller presents a simple structure when compared to reported APDR controllers since only two parameters are adapted ($\theta_{\sin}, \theta_{\cos}$), and no parameters estimator is required, thus making it possible the use of low-cost MCUs and highlighting its simple implementation feature. On the other hand, a future analysis could assess the possibility to implemented the APDR subsystem in an analogical way.

6.3 PI&APDR DESIGN EXAMPLE

In this section the components of the DC/DC LLC resonant converter are firstly defined. Following, the PI controller is designed and the section is finished with the APDR subsystem design. Table 15 shows the LLC resonant LED driver parameters, designed employing the classical design procedure. Analyzing Table 15, it can be noticed that the converter is designed to operate with a variable V_{BUS} ranging between 360 V and 420 V, and a variable output current to perform dimming at least between 100% and 20%. Regarding the LED module, three BXRC-50C4000-F-04 devices are connected in series (BRIDGELUX, 2014). The LED module electrical behavior is described in Section 2.1. For the sake of completeness, Appendix G provides access to the MATLAB scripts and PSIM simulation files developed to analyze and design the proposed PI&APDR controller.

6.3.1 PI subsystem design

As aforementioned, the PI subsystem design is based on the frequency-response method. Therefore, initially it is necessary to define the transfer function (TF) that relates the converter output (i_{LED}) with their control action (f_{sw}), denoted as $G_P(s)$. However, as can be seen in Fig. 93, to avoid aliasing effect on the digital system, as well as protect the MCU ADC stage, the measured i_{LED} is filtered by a low pass filter (LPF), whose TF is defined as $H_i(s)$. So, to

Table 15 – LLC resonant LED driver parameters

Parameter	Designator	Value
LLC LED driver design specification		
Nominal DC input voltage	V_{BUS}	400 V
Minimal DC input	$V_{BUS.MIN}$	360 V
Maximum DC input voltage	$V_{BUS.MAX}$	420 V
Bus voltage ripple frequency	$f_{\Delta V}$	94–126 Hz
LLC converter resonant frequency	f_o	100 kHz
Maximum LLC converter output power	P_O	100 W
Minimal LLC converter output power	$P_{O.MIN}$	≈15 W
ADC sampling period	T_s	25 μs
Designed LLC LED driver resonant converter		
Average LED current range	I_{LED}	$0.2 - 1.15\ A$
Average LED voltage	V_{LED}	$80.4 - 87.3\ V$
Resonant capacitor	C_S	12 nF
Resonant inductor EE 20/10/05; 30 turns; 2#AWG27	L_S	211 μH
Magnetizing inductance	L_M	633 μH
Output capacitor (Film capacitor)	C_O	10 μF/100V
Transformer turns ratio (n) EE 30/15/14; $n_P = 32$ (2#AWG27); $n_S = 14$ (3#AWG27)	N_P/N_S	2.29
Half-bridge switching frequency	f_{sw}	86.9–131.1 kHz
Half-bridge power MOSFETs	S_1-S_2	IPD60R280P7S
Output rectifier diodes	D_1-D_2	SB3200TA

Source: Author.

consider the LPF dynamics during PI design, the uncompensated loop gain $T(s)$[1] (loop gain without compensation) will be given by $G_P(s)H_i(s)$.

As a practical rule, the ADC sampling frequency $f_s = 1/T_s$ is usually selected to be 10 times faster than the highest gain crossover frequency (f_c) of interest, and the LPF bandwidth is commonly designed to be lower than $1/2$ of the f_s. Thus, $f_s = 40\ kHz$ is selected in order to be able to assess different controllers, with a cut-off frequency lower than 4 kHz while keeping the same experimental setup. In this way, the LPF is implemented through the Sallen Key topology, with a cut-off frequency of 15 kHz, a quality factor of 0.5, and a damping ratio equal to 1, yielding

$$H_i(s) = \frac{1 \cdot 10^{10}}{(s + 1 \cdot 10^5)^2} \tag{6.8}$$

Given the parameters on Table 15 and considering the nominal operating conditions, the modeling procedure presented in Chapter 3 has been employed to obtain $G_P(s)$. Now, taking into account $H_i(s)$ and the $G_P(s)$, and neglecting the high frequency right half-plane zero, and poles and zeros higher than the f_{sw}, a nominal sixth-order system is obtained for $T(s) = G_P(s)H_i(s)$, given by (6.9). To avoid unexpected instability, special attention have to be given to the RHP zero and its effect in the system dynamic behavior.

[1]The loop gain $T(s)$ is defined as the product of the forward and feedback paths small-signal gains.

$$T(s) = \frac{-2.2591 \cdot 10^{21}}{(s^2 + 1.594 \cdot 10^4 s + 9.973 \cdot 10^8)(s^2 + 1.346 \cdot 10^5 s + 2.453 \cdot 10^{11})} \frac{10^{10}}{(s + 10^5)^2} \quad (6.9)$$

Even though the controller will be digitally implemented, the design of the PI controller is performed employing the well-established frequency-response method. However, since frequency-response methods do not apply to the z plane, the w transformation is employed, which transforms a TF in the z plane into that in the w plane (OGATA, 1995). Afterwards, conventional frequency-response techniques can be used in the w plane. Therefore, based on the procedure presented in (OGATA, 1995), firstly $T(s)$ is discretized with a zero-order hold (ZOH) considering f_s. In the next step, to model the transportation time and obtain a strictly proper TF for the controller, the unit delay (z^{-1}) is added to the TF in the z plane ($T(z)$). Subsequently, using the bilinear transformation, $T(z)$ is converted into a rational function in the w plane, yielding the uncompensated loop gain $T(w)$. In this procedure, the ADC gains are neglected, being their effect compensated in the implementation.

At this point, working in the w plane, the PI regulator is finally designed employing frequency-response technique. With the pole in origin, the gain and zero position are adjusted to obtain: i) a 10 Hz crossover frequency, which is a decade below the minimum value of $f_{\Delta V}$; and, ii) High gain and phase margins, respectively, 44.7 dB and 89.6 deg. With these parameters, a first-order behavior is achieved with a settling time of around 60 ms, which is considered adequate for this particular application. The PI in w domain is given by

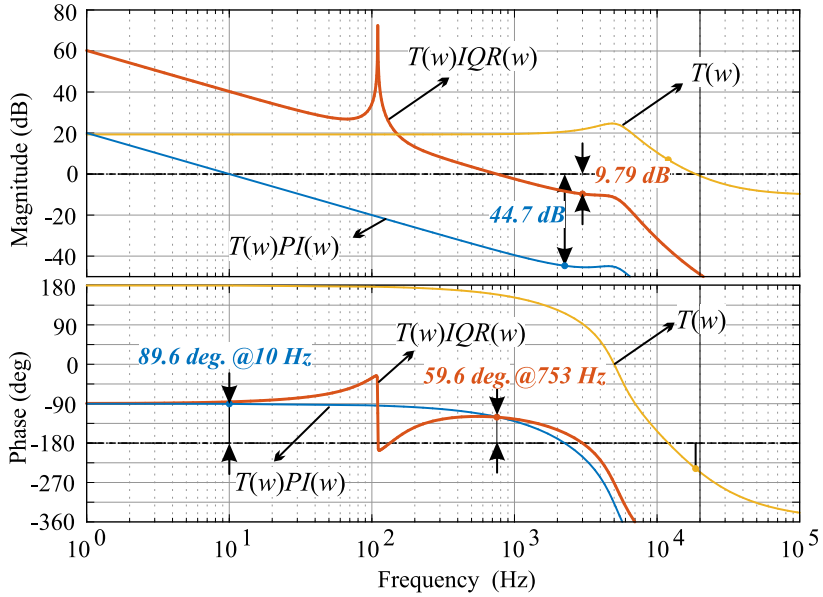
$$PI(w) = -\frac{0.00024(w + 28320)}{w} \quad (6.10)$$

For the sake of comparison, an IQR controller is also designed. The integrator provides ideally an infinite DC gain to track DC reference and reject parametric variations, while the quasi-resonant response is tuned to provide a high gain (> 30 dB) around $f_{\Delta V}$ in order to attenuate ΔI_{LED}. However, due to IQR inherent trade-off, the designed compensator provides a 9.79 dB gain margin, 59.8 deg. phase margin at 753 Hz, 12% overshoot and 5 ms settling time. The IQR TF is given by (6.11). It is worth mentioning that the proposed PI&APDR is compared with its main counterpart considering the same application, which corresponds to the classical resonant-based controller; here, the IQR is selected. Advanced state-of-the-art controllers are not practical solutions for LED drivers due to their complexity and high implementation cost. Thus, further comparisons will be omitted.

$$IQR(w) = \frac{-500(w^2 + 816.8w + 667200)}{w(w^2 + 1.382w + 477700)} \quad (6.11)$$

In order to elucidate the loop gain $T(s)$ analysis, Fig. 96 shows the Bode diagrams of the uncompensated loop gain on the w plane $T(w)$, compensated loop gain with PI controller $T(w)PI(w)$ and IQR controller $T(w)IQR(w)$. As can be seen, ideally both PI and IQR

Figure 96 – Bode Diagram comparison of the LLC LED driver compensated loop gain employing different controllers.



Source: Author.

compensated systems have an infinite DC gain. On the other hand, analyzing $T(w)IQR(w)$ high gains around $100-120\,Hz$ are noticed, guaranteeing the system low output current ripple at this frequency range. Now, assessing $T(w)PI(w)$ a low gain around $100-120\,Hz$ is evident. However, it will not be an issue for the proposed PI&APDR controller since the APDR branch is strictly responsible for attenuating ΔV_{BUS} transmission to $i_{LED}(t)$. In addition, due to the high order TF in the IQR compensated system, multiple $-180°$ crossover frequency are noticed. In this case, the more general Nyquist stability theorem was employed to analyze the system and ensure stability.

Finally, to implement (6.10) and (6.11) in the MCU, both equations are first discretized employing the bilinear method. Then, z^{-1} considered under design to obtain a strictly proper controller, is added to the discretized form of (6.10) and (6.11). If experimental results show that one step delay is not enough to perform all required calculations, the controller must be redesigned, considering further step delays. In the sequence, applying inverse Z transformation the difference equation for each controller is obtained, given by

$$u_{PI}[k+1] = u_{PI}[k] + 0.000155 \cdot e[k] - 0.000326 \cdot e[k-1] \tag{6.12}$$

$$\begin{aligned} u_{IQR}[k+1] = {} & 2.999667 \cdot u_{IQR}[k] - 2.999632 \cdot u_{IQR}[k-1] + 0.999965 \cdot u_{IQR}[k-2] \\ & - 0.006314 \cdot e[k] + 0.006184 \cdot e[k-1] + 0.006311 \cdot e[k-2] \\ & - 0.006186 \cdot e[k-3] \end{aligned} \tag{6.13}$$

For these recursive equations, it should be noticed that parameters are define as float variables with the maximum of 7 digit precision, respecting IEEE754 standard.

6.3.2 Adaptive periodic disturbance rejection design

6.3.2.1 BPF design and v_{BAC} decomposition

In order to extract the AC component from the measured $v_{BUS}(t)$, its sampled signal $v_{BUS}[k]$ is filtered by a digital band-pass filter (BPF). A second-order BPF defined in the continuous domain is given by

$$BPF(s) = \frac{H_o \cdot BW \cdot s}{s^2 + BW \cdot s + \omega_o^2} \tag{6.14}$$

Where $f_o = 2\pi\omega_o$ is the center frequency; BW is the filter bandwidth in rad/s; and, H_o is the circuit gain.

Considering a front-end PFC stage with the universal input voltage, the ΔV_{BUS} frequency $f_{\Delta V}$ ranges between $100-120\ Hz$. Therefore, the BPF design is accomplished by defining $f_o = 110\ Hz$, whose value is at the center of the $f_{\Delta V}$; and, $BW = 2\pi 60\ rad/s$ and $H_o = 1.1$ are so determined in order to avoid attenuation of the filtered AC component of the bus voltage ripple within $100-120\ Hz$.

Fig. 97 shows the designed BPF Bode Diagram and the expression of $BPF(s)$. Following, $BPF(s)$ is discretized using bilinear transformation with $T_s = 25\ \mu s$. Then, with inverse Z transformation, the BPF recursive form $v_{BAC}[k]$ is obtained. Manipulating $v_{BAC}[k]$, the determination of $V_{\sin}[k]$ and $V_{\cos}[k]$ is given by (6.16) and (6.17), respectively.

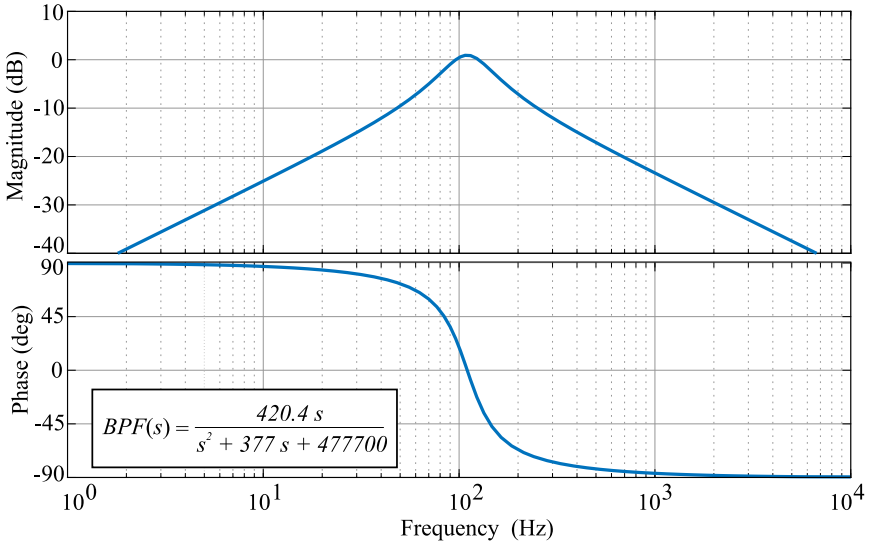
$$\begin{aligned} v_{BAC}[k] = 1.9903 \cdot v_{BAC}[k-1] - 0.9906 \cdot v_{BAC}[k-2] + 0.00523 \cdot v_{BUS}[k] \\ - 0.00523 \cdot v_{BUS}[k-2] \end{aligned} \tag{6.15}$$

$$V_{\sin}[k] = v_{BAC}[k] \tag{6.16}$$

$$V_{\cos}[k] = \frac{1}{2\pi T_s f_{\Delta V}} (v_{BAC}[k] - v_{BAC}[k-1]) \tag{6.17}$$

The main purpose of measuring $v_{BUS}(t)$ is to obtain the fundamental frequency of the periodic disturbance, being the amplitude and phase of u_{APDR} defined by $\theta_{\sin}$ and $\theta_{\cos}$. For instance, if the gain H_o changes, the obtained values for $V_{\sin}[k]$ and $V_{\cos}[k]$ will also change, thus $\theta_{\sin}$ and $\theta_{\cos}$ will converge to a different value in order to compute the correct amplitude and phase for u_{APDR}. On the other hand, advanced techniques such as phase-locked loop (PLL)

Figure 97 – Designed Band Pass Filter Bode Diagram.



Source: Author.

and Kalman filter could be employed to disclose the ΔV_{BUS} frequency. However, these methods usually increase the digital system computational effort and bring additional complexities to the LED driver design.

6.3.2.2 Determination of α

The inner loop control action $u_{APDR}[k]$ is given by (6.3). At this point, $V_{\sin}[k]$ and $V_{\cos}[k]$ are known from bus voltage filtering and signal decomposition. To define the automatic adapted parameters $\theta_{\sin}[k]$ and $\theta_{\cos}[k]$ the algorithm given in (6.6) is rewritten in (6.18) for the sake of readability.

$$\theta_{sin}[k+1] = \theta_{sin}[k] - \frac{\alpha T_s e_1[k]}{m^2[k]} V_{sin}[k] \tag{6.18a}$$

$$\theta_{cos}[k+1] = \theta_{cos}[k] - \frac{\alpha T_s e_1[k]}{m^2[k]} V_{cos}[k] \tag{6.18b}$$

Analyzing (6.18) it is noticed that α is the only undefined parameter. Actually, α is the unique parameter of the APDR subsystem whose definition depends on the application and control-loop performance specifications. As aforementioned, α dictates the automatic parameters adaptation speed, and so consequently the transient time for the periodic disturbance rejection. In this ways, to develop a design procedure for α, the APDR subsystem is analyzed from the stability point of view. Therefore, this section follows presenting an alternative way to determine e_1, whose definition is essential to analyze the APDR stability in the sequence.

Tracking error definition

For the sake of simplicity, both PI and APDR subsystems are considered decoupled. Thus, since the APDR is strictly responsible for rejecting the bus voltage periodic disturbance d, and assuming that PI is fully functional in regulating the DC value at $r = 0$, the system can be represented as shown in Fig. 98. The output y can be then defined by

$$y = y_1 + y_2 = G_p(s)u_{APDR} + F(s)d \tag{6.19}$$

The periodic sinusoidal disturbance d can be defined by a linear combination of V_{sin} and V_{cos}, with weighting parameters $\bar{\theta}^*_{sin}$ and $\bar{\theta}^*_{cos}$, as given by

$$d = -\bar{\theta}^*_{sin}V_{sin} - \bar{\theta}^*_{cos}V_{cos} = -\bar{\boldsymbol{\theta}}^{*T}\mathbf{v} \tag{6.20}$$

where $\bar{\boldsymbol{\theta}}^* = \left[\bar{\theta}^*_{sin}; \bar{\theta}^*_{cos}\right]^T$.

Following (6.5), in continuous time, the APDR subsystem control action is given by

$$u_{APDR} = \boldsymbol{\theta}^T\mathbf{v} \tag{6.21}$$

With $r = 0$, the APDR tracking error $e_1 = y - r$, is reduced to $e_1 = y$. Hence, substituting (6.21) and (6.20) into (6.19), yields

$$e_1 = G_p(s)\boldsymbol{\theta}^T\mathbf{v} - F(s)\bar{\boldsymbol{\theta}}^{*T}\mathbf{v} \tag{6.22}$$

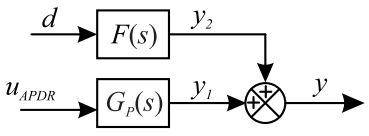
Inspecting (6.22), it is noticed that e_1 depends of $\boldsymbol{\theta}$ and $\bar{\boldsymbol{\theta}}^*$. Where $\boldsymbol{\theta}$ origin is in the APDR control action, and $\bar{\boldsymbol{\theta}}^*$ is related to the periodic disturbance d. From the APDR subsystem point of view, it is assumed that there is a correct solution called $\boldsymbol{\theta}^*$ for the adapted $\boldsymbol{\theta}$ that reject the disturbance d and brings e_1 to zero. Thus, the parametric adaption error ($\tilde{\boldsymbol{\theta}}$) is defined by

$$\tilde{\boldsymbol{\theta}} = \boldsymbol{\theta} - \boldsymbol{\theta}^* \tag{6.23}$$

Now, substituting the identity $\boldsymbol{\theta} = \tilde{\boldsymbol{\theta}} + \boldsymbol{\theta}^*$ in (6.22) yields in

$$e_1 = G_p(s)\tilde{\boldsymbol{\theta}}^T\mathbf{v} + G_p(s)\boldsymbol{\theta}^{*T}\mathbf{v} - F(s)\bar{\boldsymbol{\theta}}^{*T}\mathbf{v} \tag{6.24}$$

Figure 98 – Simplified block diagram of the LLC resonant LED driver employing PI&APDR controller.



Source: Author.

Defining $p = G_p(s)\boldsymbol{\theta}^{*T}\mathbf{v} - F(s)\bar{\boldsymbol{\theta}}^{*T}\mathbf{v}$, (6.24) is rewritten as (6.25). The signal p is bounded once $\mathbf{v}$ is finite and $G_p(s)$ and $F(s)$ represent stable systems. Besides, since there is a solution for $\bar{\boldsymbol{\theta}}^*$ and $\boldsymbol{\theta}^*$, which means that these parameters are constant, the signal p tends to zero in steady-state. Furthermore, the dynamic variation of p is defined by $G_p(s)$ and $F(s)$.

$$e_1 = G_p(s)\tilde{\boldsymbol{\theta}}^T\mathbf{v} + p \tag{6.25}$$

Analysis of the APDR subsystem stability

Consider the LLC resonant converter as an LTI system, whose TF is

$$G_p(s) = k_p\frac{Z_p(s)}{R_p(s)} = k_p\frac{s^n + a_{n-1}s^{(n-1)} + ... + a_1 s + a_0}{s^n + b_{n-1}s^{(n-1)} + ... + b_1 s + b_0} \tag{6.26}$$

Where Z_p is a monic Hurwitz polynomial, R_p is a monic polynomial, and k_p is the high-frequency gain with known sign.

In continuous time, the APDR control action is given by (6.27), and the parametric adaptive law is defined by (6.28).

$$u_{APDR} = \boldsymbol{\theta}^T\boldsymbol{v} \tag{6.27}$$

$$\dot{\boldsymbol{\theta}} = -\frac{\alpha\mathbf{v}e_1}{m^2} \tag{6.28}$$

Employing Lyapunov's second method, the adopted defined positive V scalar function is given by

$$V = \frac{1}{2}\tilde{\boldsymbol{\theta}}^T\tilde{\boldsymbol{\theta}} \tag{6.29}$$

Now, if it is proved that the gradient of V is negative, it means that $\tilde{\boldsymbol{\theta}}$ tends to zero. Consequently, the tracking error also tends to zero, and the APDR subsystem will be stable. The derivative of (6.29) with respect to t yields

$$\dot{V} = \frac{1}{2}\dot{\tilde{\boldsymbol{\theta}}}^T\tilde{\boldsymbol{\theta}} + \frac{1}{2}\tilde{\boldsymbol{\theta}}^T\dot{\tilde{\boldsymbol{\theta}}} = \tilde{\boldsymbol{\theta}}^T\dot{\tilde{\boldsymbol{\theta}}} \tag{6.30}$$

From (6.23), the time derivative of parametric adaption error gives $\dot{\tilde{\boldsymbol{\theta}}} = \dot{\boldsymbol{\theta}}$. Now, considering e_1 defined by (6.25), defining $\delta = d/dt$ as the differential operator, and taking into account (6.28), $\dot{\tilde{\boldsymbol{\theta}}}$ can be rewritten as (6.31). Substituting (6.31) in (6.30) yields (6.32). To avoid the use of time and frequency domain in the same equations, the differential operator δ is defined (ASTROM ET AL., 2008). So, $G_p(s)$ and $G_p(\delta)$ are equivalent.

$$\dot{\tilde{\boldsymbol{\theta}}} = \dot{\boldsymbol{\theta}} = -\alpha \frac{\mathbf{v}\left(G_p(\delta)\tilde{\boldsymbol{\theta}}^T\mathbf{v} + p\right)}{m^2} \tag{6.31}$$

$$\dot{V} = -\alpha \frac{\tilde{\boldsymbol{\theta}}^T\mathbf{v}\left(G_p(\delta)\tilde{\boldsymbol{\theta}}^T\mathbf{v}\right)}{m^2} - \alpha \frac{\tilde{\boldsymbol{\theta}}^T\mathbf{v}p}{m^2}. \tag{6.32}$$

At this point, the sign of (6.32) has to be carefully analyzed in order to assess system stability. Because p tends to zero in steady-state with the dynamic of $G_p(\delta)$ and $F(\delta)$, which means, much faster than the variation of $\tilde{\boldsymbol{\theta}}$, only the first term in the right side of (6.32) is analyzed under stability point of view.

Therefore, to ensure a negative gradient, the sign of α ($sign(\alpha)$) must have the same sign of the plant high frequency gain k_p. Besides, if $G_p(\delta)$ owned a constant value, $\dot{V}$ would be negative tending to zero while e_1 is decreasing. However, $G_p(\delta)$ is a system with limited bandwidth. In this way, since m^2 is positive and α is constant with same sign as k_p, to guarantee that $\dot{V}$ is negative, it is necessary to ensure that term $\tilde{\boldsymbol{\theta}}^T\mathbf{v}\left(G_p(\delta)\tilde{\boldsymbol{\theta}}^T\mathbf{v}\right)$ remains predominantly with the same sign. To address this last constraint, it is required that the dynamic behavior of the parametric adaptation law must be considerable slower than $G_p(\delta)$. Once the dynamic behavior of the parametric adaptation law is a function of α it is inferred that $G_p(\delta)$ bandwidth (BW_p) must satisfy (6.33) to ensure system stability. Actually, the constraint given in (6.33) can be seen as a design guideline for the magnitude of α. Where $sign(\alpha) = sign(k_p)$.

$$BW_p >> |\alpha| \tag{6.33}$$

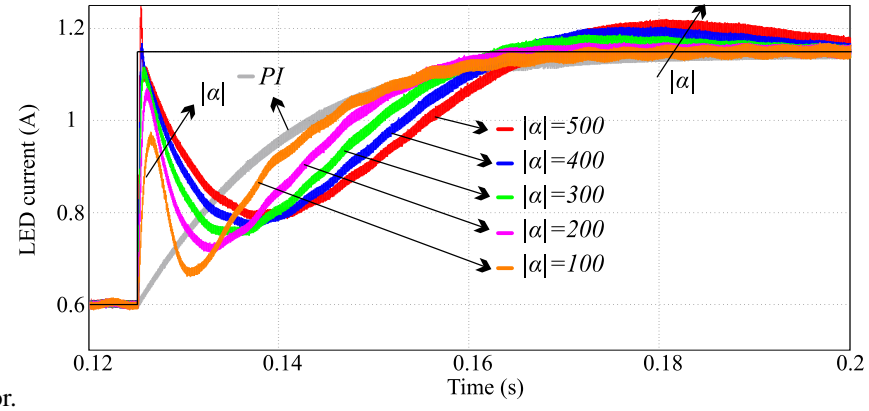
Summarizing the above presented APDR subsystem stability analysis, the constraints to define α are obtained as follows: i) the sign of α have to be equal to the sign of the plant high frequency gain, i.e., $sign(\alpha) = sign(k_p)$; ii) the absolute value of α rad/s must be very small in comparison to the plant bandwidth BW_p rad/s.

In this way, analyzing $T(s)$ in (6.9), a negative sign for k_p is noticed. Then, assuming that $|T(s)| \approx |T(w)|$, a bandwidth around $BW_p \approx 44$ k rad/s (≈ 7 kHz) can be seen in Fig. 96. However, before defining $|\alpha| << BW_p$, it should be carried in mind that the LLC is strongly non-linear, and the converter is subjected to a wide operating range. Thus, to obtain a conservative design, $|\alpha| \leq BW_p/100$ should be employed. On the other hand, during the transient response of the whole control system, it is expected that the dynamic behavior follows the PI response. In this way, assessing (6.18), it can be seen that as greater α greater will be the variation of $\boldsymbol{\theta}$ during the transient response when e_1 differs from zero. Consequently, greater will be u_{APDR} during this transition, impacting the whole system transient response. To elucidate this scenario, Fig. 99 shows simulation results of the LED current response under a reference step for different values of $|\alpha|$. In this simulation, the LLC parameters given in Table 15 are employed, and ΔV_{BUS} is set to zero. Then, employing the proposed PI&APDR controller the response is obtained for

different values of $|\alpha|$. The response labeled as PI (gray trace) employs the single PI, being $u_{APDR} = 0$. As can be seen, the higher $|\alpha|$ more the transient response diverges from PI ones. In addition, also employing simulation results, Fig. 100 shows the LED current waveform during the transition from the use of the single PI to PI&APDR controller for different values of $|\alpha|$. As shown, for $|\alpha| = 1000$ the system is unstable. On the other hand, if $|\alpha| = 1$, it can be seen that the current ripple is going to be rejected, but with a prolonged transition.

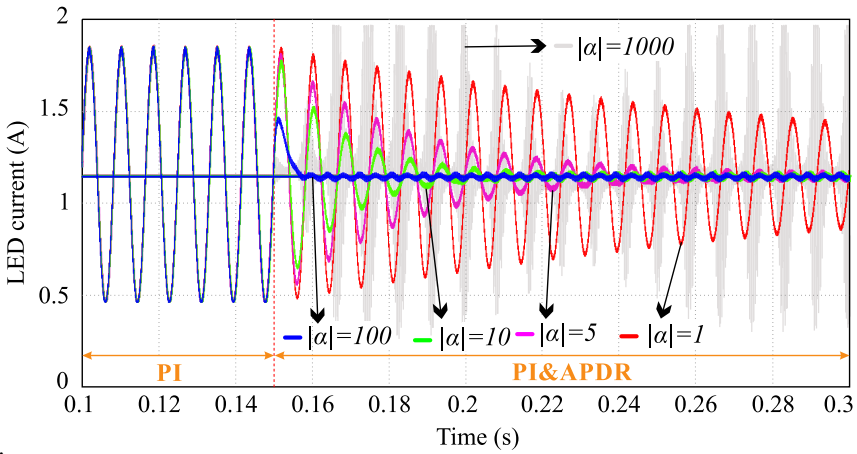
Gathering these results, the following procedure is proposed for α design: **i)** $sign(\alpha) = sign(k_p)$; **ii)** Restrain the value of α taking into account $|\alpha| \leq BW_p/100$; **iii)** in order to optimize the design, the system transient behavior under load step should be analyzed for different values of α, while satisfying (ii). Then following this methodology, it culminates in selecting $\alpha = -250$ for the presented LLC resonant LED driver. It is worth mentioning that refining the adjustment of design parameters based on experimental and/or simulation results is usual in adaptive controllers. Nevertheless, it must be noted that only one parameter is analyzed, which simplifies this optimization.

Figure 99 – LED current transient behavior under reference step for different values of α.



Source: Author.

Figure 100 – LED current i_{LED} waveform during the transition from single PI to PI&APDR controller for different values of α.



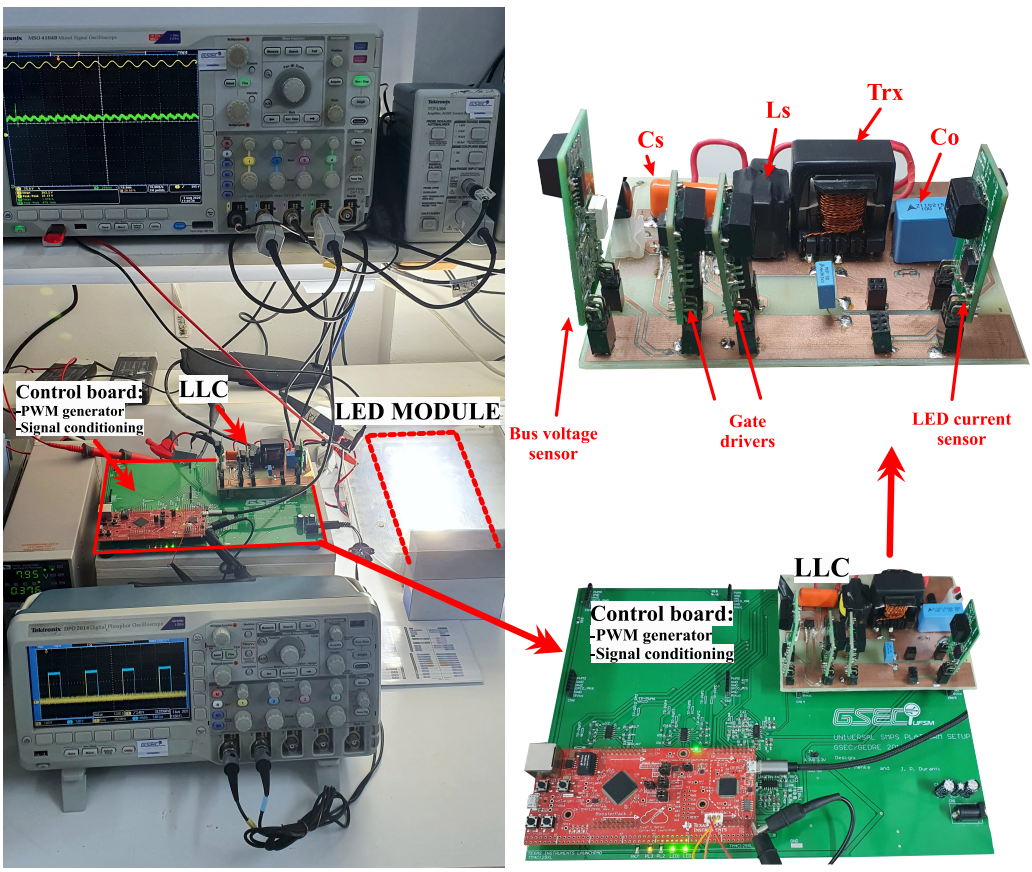
Source: Author.

6.4 EXPERIMENTAL RESULTS

Experimental results are presented in this section in order to evaluate the performance of proposed PI&APDR control system for the LLC resonant converter supplying an LED load over a wide dimming range. To better assess the PI&APDR, its performance is compared with IQR controller. The comparison is intended to evaluate the performance of the proposed control-system with the classical solutions, which claim for simplicity. Table 15 presents the employed components to build up the digitally controlled LLC LED driver shown in Fig. 93. To realize the digital control system, TM4C1294NCPDT MCU from Texas Instruments is employed, which contains a 120 MHz clock and 12 bits ADC converter (TEXAS INSTRUMENTS, 2014). Fig. 101 shows photography of the laboratory test bench utilized to obtain the experimental results.

Since the focus of this study lies on the control system of the DC/DC stage, the front-end PFC is not implemented, and the v_{BUS} is provided by a controllable voltage source (Keysight 6812B). Nevertheless, in order to emulate the real conditions established by the front-end PFC stage, it is taken into account the ΔV_{BUS} variation as a function of the output power ($P_O = V_{LED}I_{LED}$), frequency ($f_{\Delta V}$), average bus voltage (V_{BUS}), C_{BUS} and converter

Figure 101 – Photography of the laboratory test bench.



Source: Author.

efficiency (η), as given by (6.34). The DC-link capacitance is assumed to be 25 μF and PFC efficiency $\eta = 90\%$.

$$\Delta V_{BUS} = \frac{V_{LED} I_{LED}}{\pi f_{\Delta V} V_{BUS} C_{BUS} \eta} \tag{6.34}$$

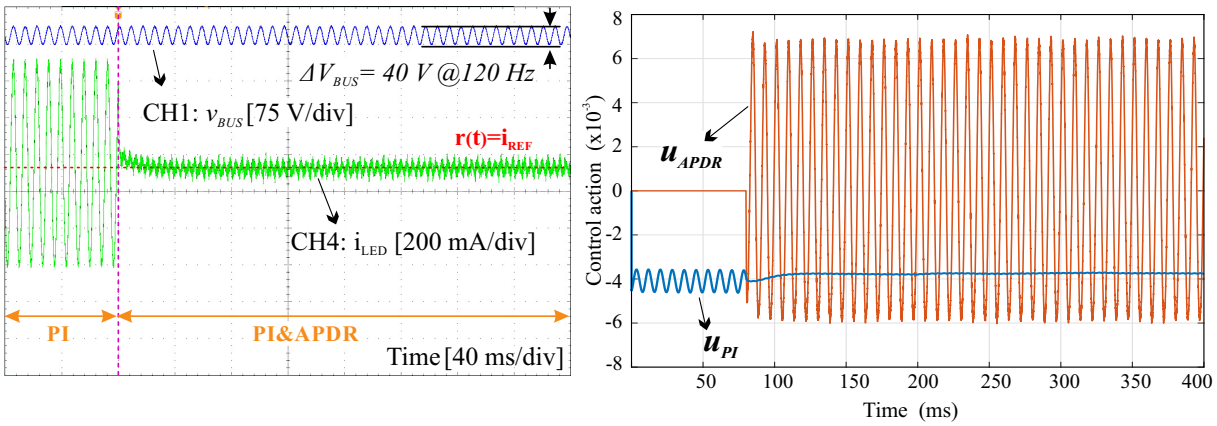
6.4.1 Steady-state operation of the closed-loop LLC resonant LED driver

Fig. 102 shows the LED current and both PI and APDR control action during the transition from operation employing solely a single PI to the operation with PI&APDR controller. As can be seen, when only PI is employed, the LED current presents a considerable high ΔI_{LED}. Observing u_{PI} it can be seen an effort to generate the required AC component to reject ΔV_{BUS}, however due to PI reduced gain around $f_{\Delta V}$ this effort is not enough. Nevertheless, when the APDR subsystem is enabled and so culminating in the PI&APDR controller, the ΔI_{LED} is now strongly reduced due to u_{APDR}, which provides to the converter the required control action to reject ΔV_{BUS}. Hence, it can be inferred that the APDR subsystem is functioning as expected, strictly reducing ΔI_{LED} without interfering with average output current regulation, which is controlled strictly by the outer PI loop.

Fig. 103 shows v_{BUS} and i_{LED} measurement for LLC resonant LED driver operating with the IQR controller at the extreme operational conditions, given by nominal and minimum I_{LED}, being $f_{\Delta V} = 120\ Hz$. Fig. 104 shows the same measurement when the proposed PI&APDR controller is employed. As can be seen, for both controllers the reference value is tracked, and a reduced peak-to-peak current ripple is measured even with considerable bus voltage ripple. Notice that ΔV_{BUS} is adjusted for each test as defined by (6.34).

Fig. 105 shows v_{BUS} and i_{LED} measurement for LLC resonant LED driver operating

Figure 102 – LED current i_{LED}, bus voltage v_{BUS} and both PI u_{PI} and APDR u_{APDR} control action waveform during the transition from single PI to PI&APDR controller.

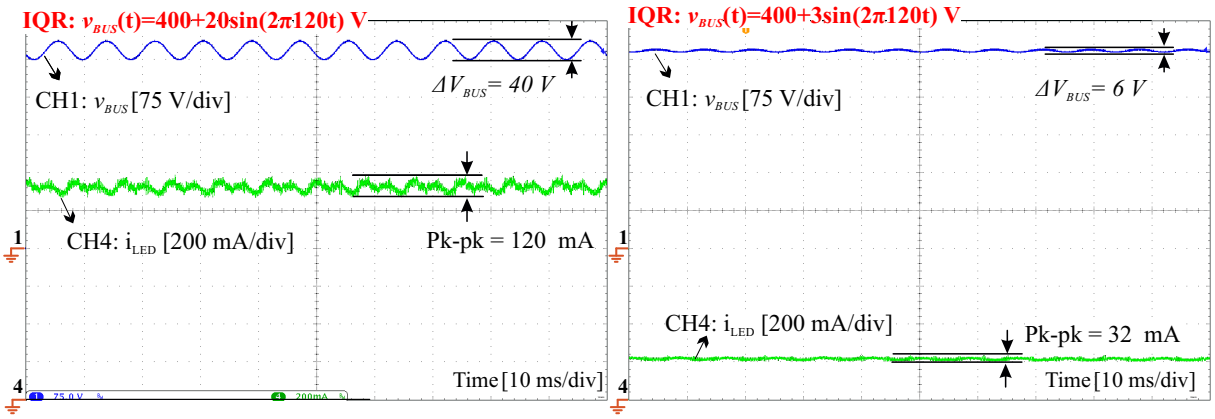


Source: Author.

with the IQR controller at the nominal I_{LED} for different values of $f_{\Delta V}$. Fig. 106 shows the same measurement when the proposed PI&APDR controller is employed. As can be seen in these results, the DC reference is tracked, and regardless the $f_{\Delta V}$, a reduced peak-to-peak current ripple is measured even with a high bus voltage ripple.

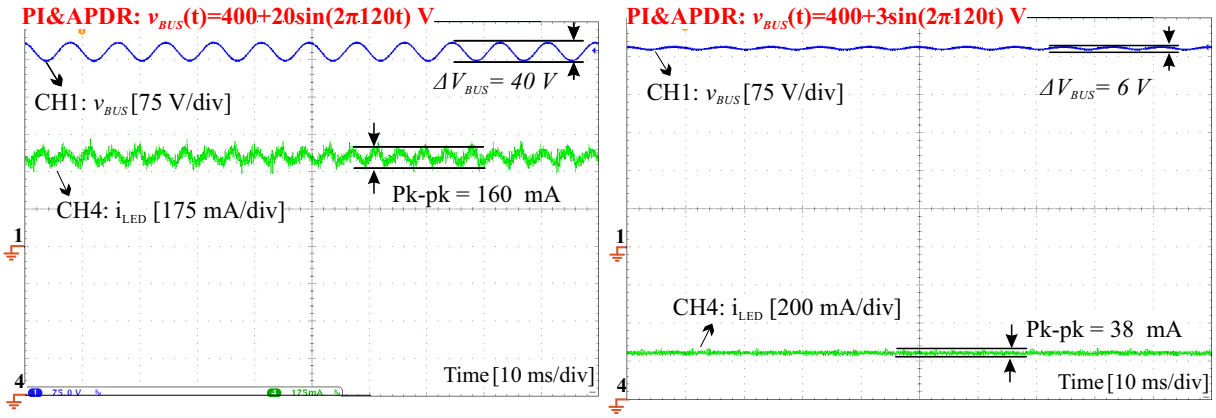
Analyzing Fig. 103, Fig. 104, Fig. 105, and Fig. 106, there is a certain difficulty in identifying the LED current ripple main harmonic component. Therefore, in order to better compare the action of IQR and PI&APDR, the first three harmonics of the current ripple have been calculated using FFT, as shown in Fig. 107 for $f_{\Delta V} = 120\ Hz$. Thus, analyzing the fundamental harmonic of the LED current ripple $\Delta I_{LED.1}$, it can be noticed a superior

Figure 103 – Steady-state v_{BUS} and i_{LED} measurement of the LLC resonant LED driver at the extreme operational conditions employing IQR controller; Left-trace: Nominal $I_{LED} = 1.15\ A$; Right-trace: Minimum $I_{LED} = 0.2\ A$.



Source: Author.

Figure 104 – Steady-state v_{BUS} and i_{LED} measurement of the LLC resonant LED driver at the extreme operational conditions employing PI&APDR controller; Left-trace: Nominal $I_{LED} = 1.15\ A$; Right-trace: Minimum $I_{LED} = 0.2\ A$.

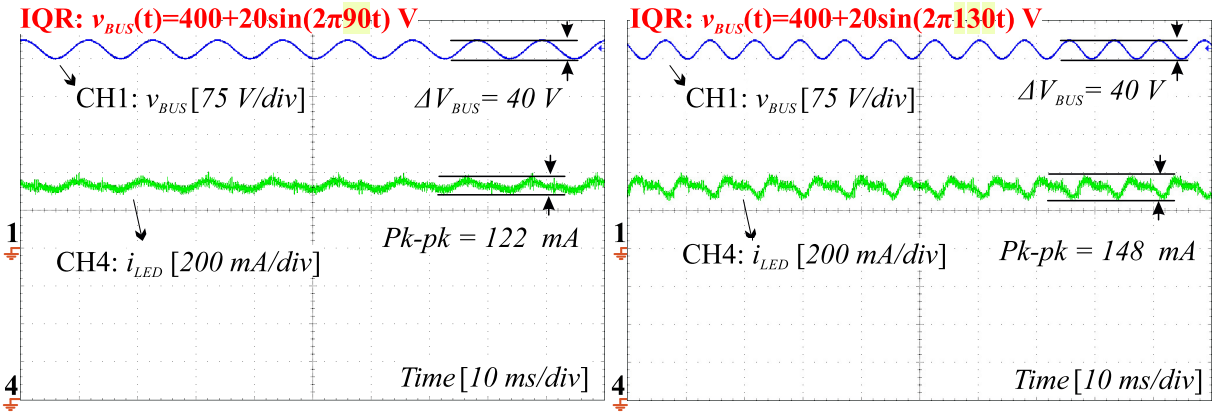


Source: Author.

performance of the proposed PI&APDR in reducing this ripple component in comparison to IQR controller. Regarding the second harmonic $\Delta I_{LED.2}$ at 240 Hz, it can be seen that this harmonic correspond to the main component when PI&APDR is employed. However, its amplitude is lower than IQR ones. For the third harmonic, both PI&APDR and IQR present a similar amplitude over the whole dimming range. Nevertheless, in order to obtain a better insight of the ΔI_{LED} reduction, the driver modulation index (Mod(%)) in comparison to the IEEE Std 1789-2015 (IEEE STD 1789, 2015) limits is analyzed in next subsection.

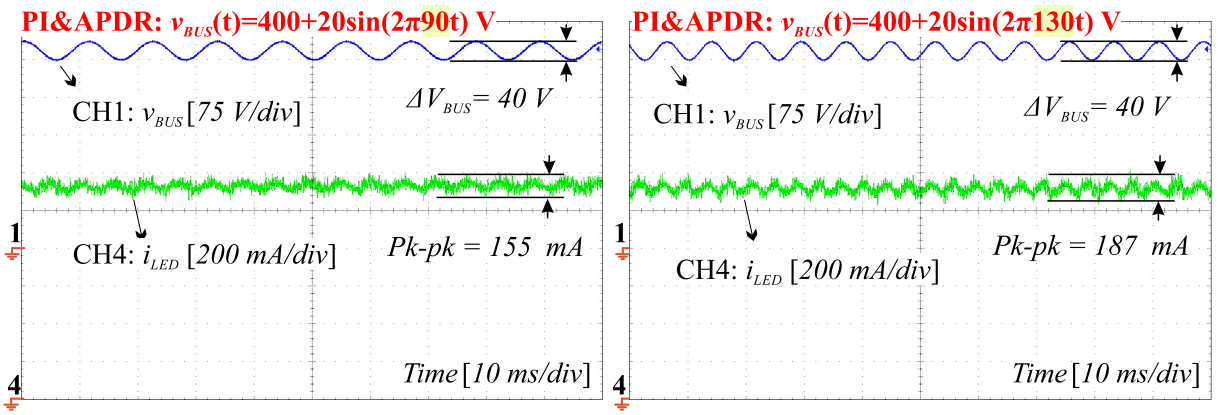
Finally, with the purpose of compare the computational effort, the time required to execute each control law is measured during steady-state operation. The proposed PI&APDR controller needs 7.52 μs to finish all their calculations, which is similar to the value of 6.56 μs

Figure 105 – Steady-state v_{BUS} and i_{LED} of the LLC resonant LED driver at the nominal I_{LED} employing the IQR controller under different values of $f_{\Delta V}$; Left-trace: $f_{\Delta V} = 90\ Hz$; Right-trace: $f_{\Delta V} = 130\ Hz$.



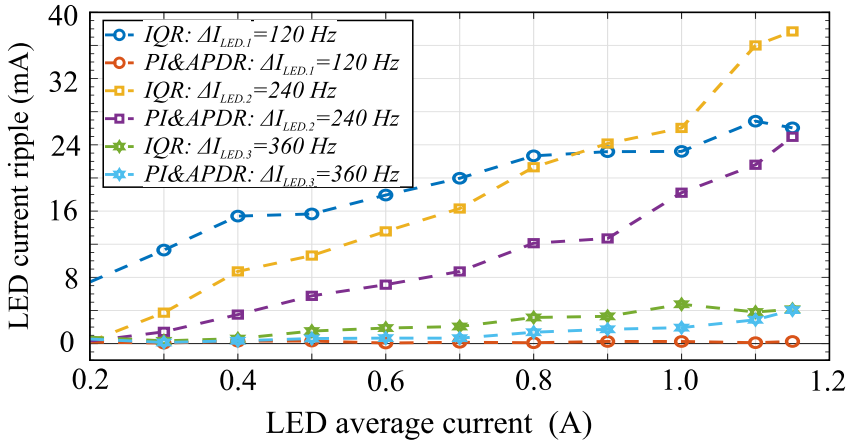
Source: Author.

Figure 106 – Steady-state v_{BUS} and i_{LED} of the LLC resonant LED driver at the nominal I_{LED} employing the PI&APDR controller under different values of $f_{\Delta V}$; Left-trace: $f_{\Delta V} = 90\ Hz$; Right-trace: $f_{\Delta V} = 130\ Hz$.



Source: Author.

Figure 107 – LED current ripple amplitude for the first three harmonics when $f_{\Delta V} = 120\ Hz$.



Source: Author.

required by IQR. Therefore, it can be inferred that the proposed controller implementation is as simple as conventional controllers.

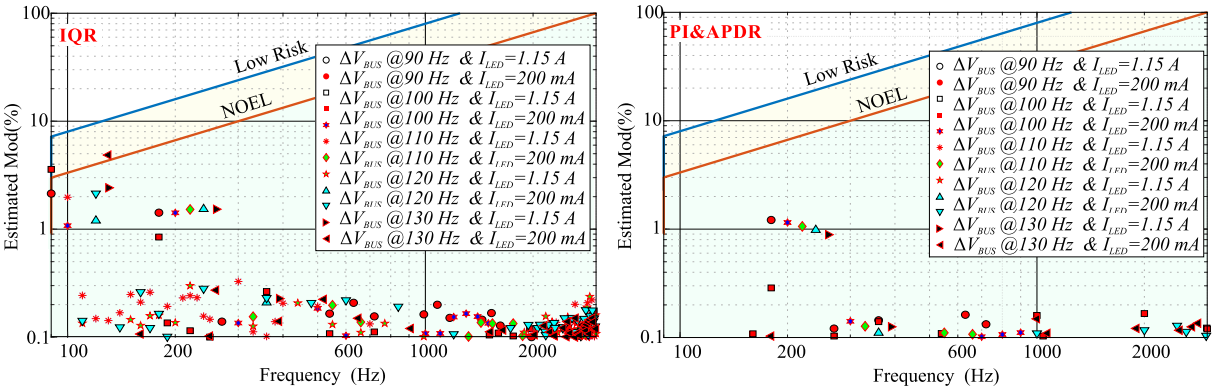
Furthermore, it is worth of mentioning that analyzing the experimental measurements under steady-state, no impact of the controller over the efficiency curve is noticed. Thus, further results comparing the efficiency curve are omitted.

6.4.2 LED driver estimated flicker assessment

Assuming that the LED operates in its linear region, where the output light is directly proportional to i_{LED}, the Mod(%) is estimated from the FFT decomposition of i_{LED}. In this way, each i_{LED} harmonic is translated into the Mod(%) at different frequencies. Although the IEEE Std 1789-201 employs light modulation to limit the harmonic content, it is a common practice to consider that the emitted light is linearly related to the LED current, especially for frequencies below 1 MHz.

From left-to-right, Fig. 108 shows the estimated Mod(%) of the LLC resonant LED driver employing the IQR and PI&APDR controllers, respectively. These results consider the LLC resonant LED driver operating with nominal and minimum output current and different $f_{\Delta V}$, covering the range of a front-end PFC with the universal input voltage, where the frequency can change around $50/60\ Hz\ \pm 10\%$. Under this analysis, ΔV_{BUS} is adjusted for each test as defined by (6.34). As can be noticed, even satisfying the low risk limits proposed by IEEE Std-1789-2015, the LLC operating with IQR presents higher current harmonics at lower frequencies when compared to PI&APDR. Moreover, since low-frequency ripple is strongly attenuated when employing PI&APDR, it would be possible to employ even lower bus capacitance, enhancing the LED driver power density, as well as increasing its operational range, which highlights the proposed controller improved performance in comparison to IQR.

Figure 108 – LLC resonant LED driver estimated modulation index in comparison to the IEEE 1789-2015 recommendations limits.



Source: Author.

Alternatively, to evaluate the level of flicker for an output light that presents several harmonics, the IEEE Std. 1789-2015 recommends the computation of the normalized modulation (*NM*) (IEEE STD 1789, 2015), where a value of $NM < 1$ is an acceptable level of flicker. Basically, the NM corresponds to the weighted sum of the light output different harmonics below 1250 Hz. Assuming that the LED operates in its linear region, where the output light is directly proportional to i_{LED}, the *NM* can be estimated from the FFT decomposition of the measured i_{LED}. In this way, the *NM* is estimated by (6.35), wherein I_{LED} is the LED average current, N is the number of harmonic components below 1250 Hz, and $\tilde{i_m}$ is the weighted LED current Fourier amplitude coefficient ($|i_m|$) corresponding to frequency f_m, which is given by (6.36).

$$NM = \sum_{m=1}^{N} \left(\frac{\tilde{i_m}}{I_{LED}} \right) \tag{6.35}$$

$$\tilde{i_m} = \begin{cases} \frac{4000|i_m|}{f_m} & \text{if} \quad f_m < 90\ Hz, \\ \frac{1250|i_m|}{f_m} & \text{if} \quad 90\ Hz \leq f_m \leq\ 1250\ Hz \end{cases} \tag{6.36}$$

Fig. 109 shows the computed *NM* levels for the cases where the IQR and PI&APDR controllers are employed. As can be seen in Fig. 109, both IQR and PI&APDR controllers yield in $NM < 1$. However, it should be noticed that the IQR presents a deteriorated performance when $f_{\Delta V}$ is away from the IQR resonance (110 Hz), which outcome in a reduced robustness against ripple current rejection for $f_{\Delta V}$ variation.

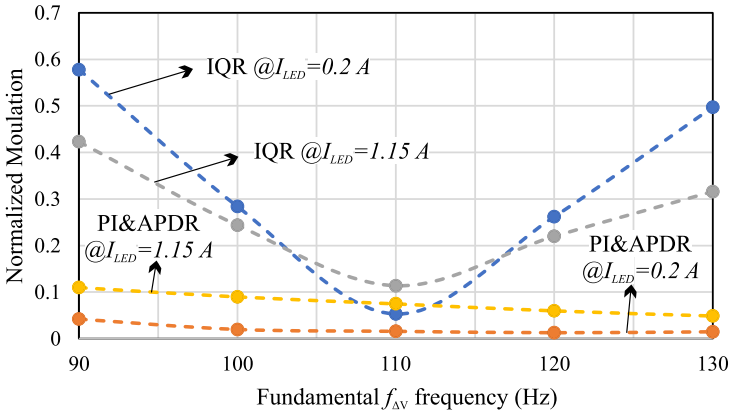


Figure 109 – Normalized modulation for the LLC resonant LED driver operating with IQR and PI&APDR controllers under different bus voltage ripple frequencies $f_{\Delta V}$.

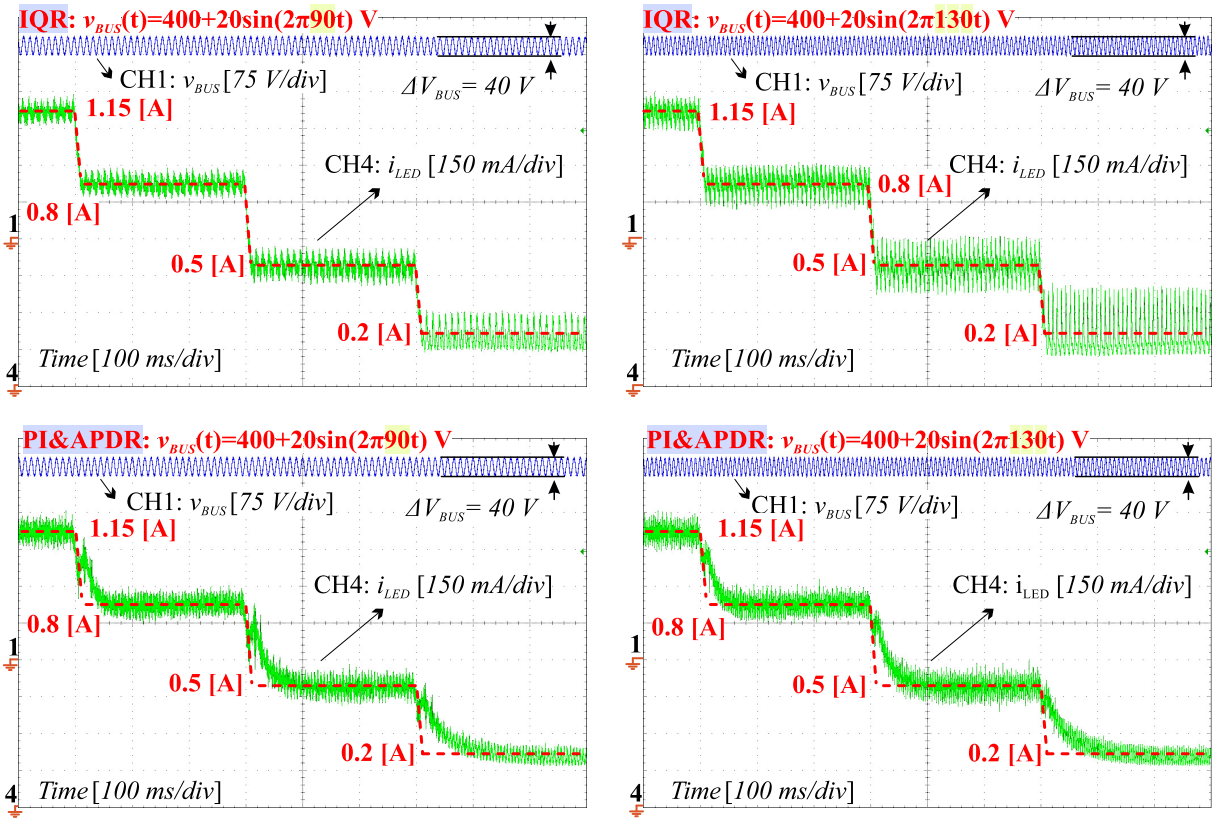
6.4.3 Reference tracking evaluation

In order to evaluate the capability of each controller to track I_{LED} reference and reduce Δi_{LED} during different dimming conditions, Fig. 110 shows the measurement of v_{BUS} and i_{LED} when the IQR or PI&APDR controller are employed considering the same dimming profile. For both controllers i_{LED} tracks the reference, differing in the transient performance and peak-to-peak reduction. As expected, the PI&APDR controller presents a dynamic which is dictated by the PI loop. Regarding ΔI_{LED} reduction, it can be noticed a deteriorated performance for the IQR controller when it goes to deeper dimming levels and when bus voltage ripple frequency diverges from resonant frequency of IQR, which is also expected and explained by the changing of converter dynamic behavior.

6.4.4 V_{BUS} disturbance rejection and transient behavior under reference step

Fig. 111 shows the measured waveform of v_{BUS} and i_{LED} for LLC resonant LED driver operating with IQR or PI&APDR controllers under a DC step in V_{BUS} for $f_{\Delta V} = 100\ Hz$. On the other hand, Fig. 112 shows the transient performance of the LLC resonant LED driver employing IQR and proposed PI&APDR controller when subjected to step in the reference ($\approx 50\%$ to 100%) for $f_{\Delta V} = 120\ Hz$. Analyzing Fig. 111 and Fig. 112, it can be seen that after a transient period i_{LED} reaches its reference value I_{LED} for both controllers. However, the PI&APDR presents a dynamic that is dictated by the PI loop, which follows the first-order behavior avoiding electrical stress in the LED load caused by overshooting. For LED drivers, a smooth transient behavior is preferred to a fast dynamic system with overshoot. To avoid overshoot when IQR is employed, it is necessary to reduce its crossover frequency, which on the other hand, reduces the controller gain around $f_{\Delta V}$ and impairs the ΔI_{LED} attenuation. This

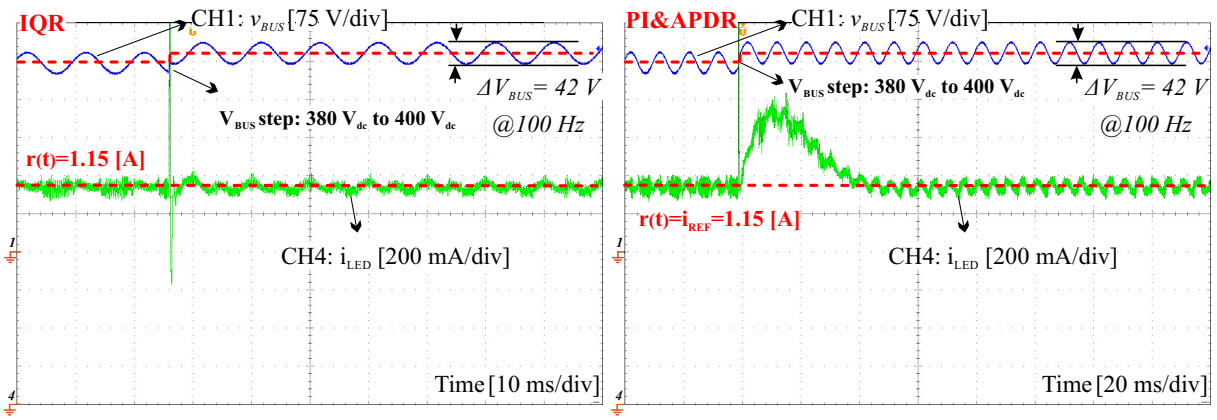
Figure 110 – LLC resonant LED driver v_{BUS} and i_{LED} waveforms during dimming profile; Upper-traces: Operating with IQR controller; Lower-traces: Operating with PI&APDR controller.



Source: Author.

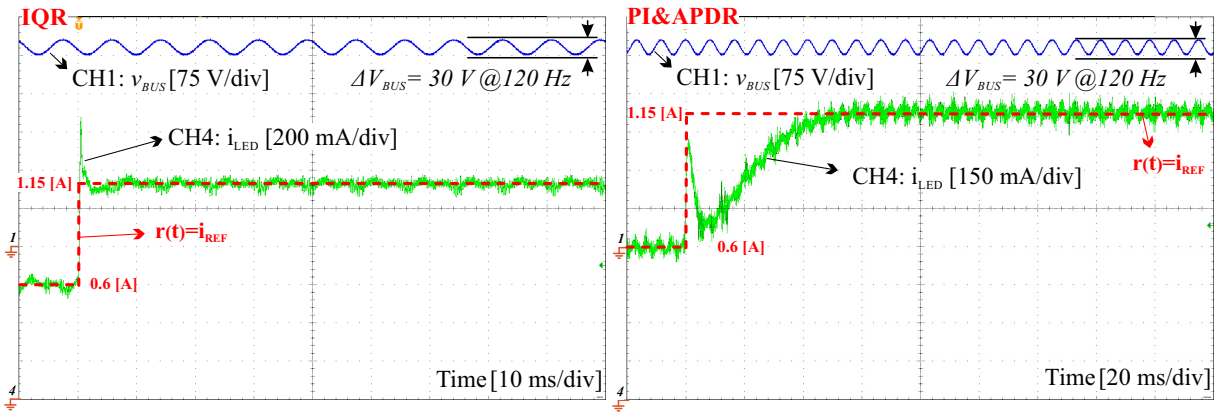
trade-off between dynamic performance and ΔI_{LED} reduction capacity noticed in IQR design does not occur when the proposed PI&APDR controller is employed.

Figure 111 – LLC resonant LED driver transient response for an input voltage step up: with conventional IQR (Left-trace) and proposed PI&APDR (Right-trace) controllers.



Source: Author.

Figure 112 – LLC resonant LED driver transient response when reference changes: with conventional IQR (Left-trace) and proposed PI&APDR (Right-trace) controllers.



Source: Author.

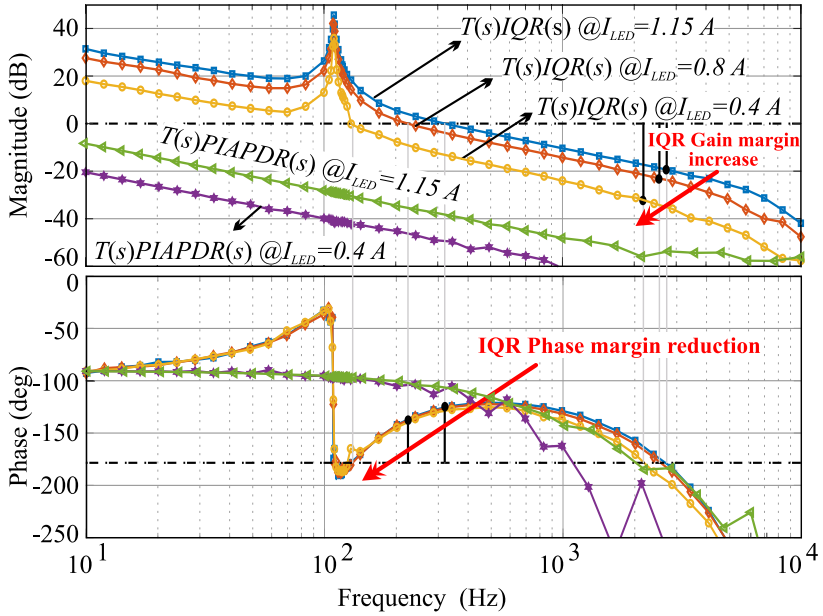
6.4.5 Controllers robustness analysis

This final assessment investigates the robustness of each controller. Therefore, considering a hypothetical scenario, the filter components are reduced in 10%, L_M is increased in 10%, transformer turn ratio is reduced in 5%, and LED module threshold voltage is reduced in 10%, emulating the worst case where the frequency range is shifted to higher values. Under this condition, the LLC resonant LED driver operating with the IQR controller becomes unstable when it goes to deeper dimming levels. In order to elucidate this outcome, the compensated loop gain is obtained from an AC-sweep analysis employing simulation results, as shown in Fig. 113. As can be seen, the IQR compensated loop is shown for an output reference of 1.15 A, 0.8 A, and 0.4 A, where the phase margin reduction is evident as I_{LED} is diminished, reaching almost 0 deg. for 0.4 A. For $I_{LED} < 0.4$ the system becomes unstable when IQR is employed. On the other hand, analyzing the PI&APDR compensated $T(s)$, for $I_{LED} = 0.4\ A$ and $I_{LED} = 1.15\ A$ the phase margin is around 90 deg. with gain margins greater than 40 dB, being so stable. However, a gain crossover frequency reduction is evident, which increases the system settling time.

With similar parametric changes, except by the LED threshold voltage, Fig. 114 shows the experimental measurement of v_{BUS} and i_{LED} during the reference step-down condition, where one of the three LED devices is short-circuited ($V_{LED} \approx 58\ V$). As can be seen, even with the parametric variation and bus voltage periodic disturbance the LED current is stable and regulated at reference when the proposed PI&APDR controller is employed. On the other hand, when IQR is employed, the system becomes unstable when the reference changes.

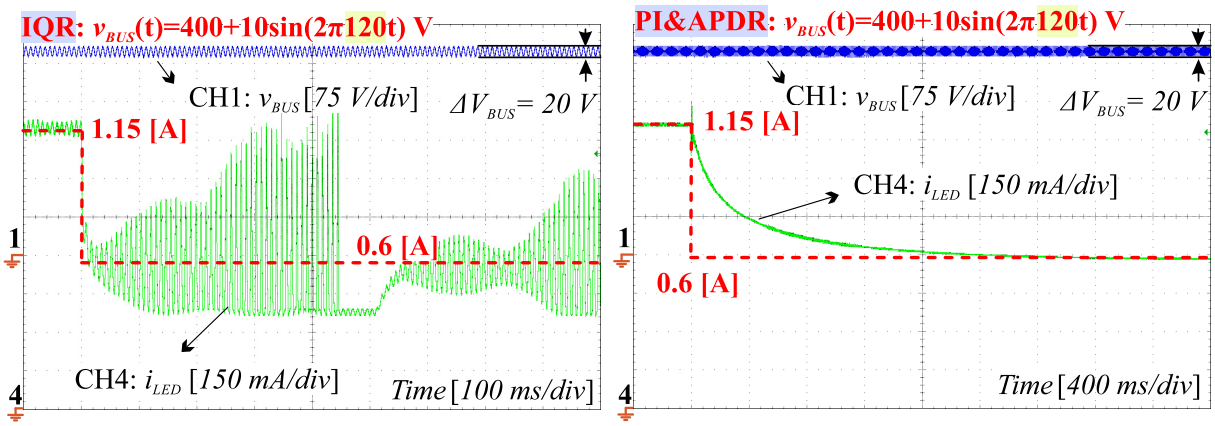
This final assessment reinforces the enhanced performance of the proposed PI&APDR controller compared to resonant-based controllers. In a general way, employing the PI&APDR,

Figure 113 – Simulation results of the compensated loop gain analysis for LLC LED driver with parametric variations: $L_M = 700\ \mu H$, $n = 2.17$, $L_S = 190\ \mu H$, $C_S = 10.9\ nF$.



Source: Author.

Figure 114 – Transient response under reference step for the LLC LED driver with parametric variations $L_M = 683\ \mu H$, $n = 2.17$, $L_S = 190\ \mu H$, $C_S = 10\ nF$, and one LED device short-circuited: Left-trace:Employing IQR controller; Right-trace: Employing PI&APDR controller.



Source: Author.

outstanding performance is demonstrated, where the system becomes robust against parametric variations and robust against different bus voltage ripple frequency and amplitude.

For the sake of completeness, Appendix F presents a brief comparison between the proposed PI&APDR and MRAC controllers.

6.5 SUMMARY

This chapter has presented the conception, analysis, design, and experimentation of a new hybrid dual-loop control system, based on PI and adaptive periodic disturbance rejection (APDR) controllers, named PI&APDR controller. The proposed controller is suited for applications where a low output current ripple is required simultaneously with a DC regulation over a wide operation range. Experimental results and simulation analysis show the outstanding performance of the proposed controller in comparison to conventional counterpart resonant-based controllers. Employing the PI&APDR controller the LED current DC reference is tracked over a wide operating range, even under parametric variations such as average bus voltage, resonant tank elements, and LED module. Besides, enhanced performance is achieved in reducing the output current ripple raised from the bus voltage ripple, where different bus voltage ripple frequencies are also considered. Conventional resonant-based controllers present deteriorated dynamic performance, higher LED ripple current, and even instabilities when subjected to these same conditions.

Finally, it is essential to mention that the proposed controller, even employing non-linear adaptive controllers, preserves the feature of having a simple design and implementation. Besides, knowing that adaptive controllers naturally require more computational resources, it is important to highlight that the computational effort of the proposed PI&APDR controller is quite similar to the conventional resonant-based controller's, allowing the designer to use conventional microcontrollers.

Summarizing the main finding of this chapter, Table 16 presents a qualitative comparison among the proposed controller and their main counterparts, being considered each controller employed in the LLC resonant LED driver performing dimming and subjected parametric variation, and periodic bus voltage disturbance.

Table 16 – LLC resonant LED Driver controllers comparison

Parameter	**PI**	**IQR**	**MRAC**	**PI&APDR**
Design complexity	Low	Low	High	Low
Low-frequency ripple reduction	Low	Medium	High	High
Implementation complexity	Low	Low	High	Low
Computational effort	Low	Low	High	Low
Robustness against periodic disturbance	Low	Moderate	High	High
Robustness against parametric variations	Moderate	Low	High	High
Design trade-off	Low	High	Low	Low
Suitability for LED drivers	Low	Moderate	Low	High

7 CONCLUSIONS AND FUTURE WORKS

7.1 CONCLUSION

Different main topics were investigated during this manuscript, which deals with the LLC resonant LED driver modeling, analysis, design, and control.

Related to the dynamic model of the LLC resonant LED driver, it was shown that the LED electrical behavior must be considered during the modeling procedure. Otherwise, the model accuracy is low and can not be employed to design reliable control systems. Therefore, based on the extended describing function, a new dynamic model for the LLC resonant LED driver was developed. Experimental results show that the proposed dynamic model presents satisfactory accuracy for the operation around the series resonance. However, it is noticed that the predicted model behavior starts diverging from the converter's real dynamic for the operation beyond the main resonance, which issue is not solved.

Regarding the LLC resonant LED driver analysis, a new approach was proposed to predict the converter behavior in the time domain. The time-domain analysis presents more accurate results than the classical first harmonic approximation when a wide operating range is required. The proposed TD solution employs the direct time-domain solution from the state-space representation. The LED electrical behavior is taken into account, and the output voltage is not approximated by a constant voltage source, which outcomes in a more general solution. Even reducing the number of assumptions, the proposed TD solution does not need any laborious calculations. All the computational effort is directed to numerical software employed to solve the system of equations. Besides, a new mode solver and operation mode map algorithms are proposed, which allow to automatically determine the LLC resonant LED driver operation mode. Finally, experimental results show an outstanding accuracy of the proposed method regardless of the operating condition, defined by the filter, load, input, etc. Nevertheless, the proposed approach is not very friendly due to their complexity, and the several steps necessary to outcome with the complete time-domain solution. Besides, even achieving accurate results with the proposed solution, it is noticed that parasitic components, neglected in the analysis, strongly impact the converter voltage and current levels. Therefore, new analyses are required where the parasitic components of the converter have to be taken into account. Besides, the developed solution employs real converter parameters, which is a drawback in comparison to normalized analysis where generic analysis can be developed.

Given the wide operating range of an LLC resonant LED driver, a new design procedure was proposed for this converter based on the weighted average-efficiency-orientated

concept. Besides, further constraints are assessed to ensure enough current gain, ZVS for the primary side, feasible switching frequency, and reduced electrical stress in the LLC components. This design procedure utilizes the TD analysis results, leading to a reliable design since the converter behavior is accurately predicted. Experimental results show the feasibility of the proposed design procedure, achieving a high performance over a wide operating range, 20% dimming. Specifically, the peak efficiency of 96.44% is achieved. In comparison to the classical design, the efficiency is improved up to 4.3%. Compared to the classical design, the proposed design should be employed when the LLC resonant LED driver is subjected to a wide operation range, which includes dimming and input voltage variations. For a LLC resonant LED driver without dimming, subjected to a constant input voltage, and operating at series resonance, the classical design procedure outcome in a satisfactory design. Regarding the proposed design, its disadvantage is given by its complexity since it follows several steps, including the LLC time-domain analysis. Besides, the design procedure does not outcomes in normalized curves.

Finally, a new hybrid control system optimized for the offline two-stage E-Cap-less Flicker-free LED driver was proposed. The essence of this control is given by a PI plus an adaptive periodic disturbance rejection subsystem. Experimental results show that the proposed control system presents a superior performance in comparison to the proportional resonant classical solutions. Precisely, an enhanced performance was noticed in tracking the LED current DC reference over a wide range, rejecting input and output step disturbance, and rejecting periodic disturbance rejection from the bus voltage ripple even under a wide frequency range. Besides, even employing non-linear adaptive controllers, the PI&APDR preserves the feature of having a simple design and implementation.

7.2 Proposal for future works

Suggested future works are presented in the following:

1. Development of the time-domain analysis for the LLC resonant LED driver considering other modulation techniques and parasitic elements.

2. Development of the time-domain analysis employing the classical normalized parameters (Q, L_n, Z_b).

3. Assess the hybridization of the APDR and other linear controllers to achieve faster dynamic response maintaining robustness, for instace, PID and APDR.

4. Development of the LLC resonant LED driver design employing optimization tools, or even, multiple objective optimization.

5. Study the performance of PI&APDR controller for an LED reference given by CC+CA signal.

6. Program an LLC analysis and design tool, incorporating the proposed time-domain solution and proposed design procedure.

7. Study of the PI&APDR controller stability in the discrete-time.

8. Study of the different small-signal modeling procedures seeking for an alternative procedure to achieve better accuracy over a wide operation range of the LLC resonant LED diver.

7.3 PUBLICATIONS

Paper published on periodicals:

1. MENKE, MAIKEL FERNANDO; SEIDEL, ALYSSON RANIERE ; TAMBARA, RODRIGO VARELLA . **"LLC LED Driver Small-Signal Modeling and Digital Control Design for Active Ripple Compensation"**. *IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS*, V.66, N.1, 2019.

2. MENKE, MAIKEL FERNANDO; DURANTI, JOÃO PAULO, ROGGIA, LEANDO, BISOGNO, FÁBIO ECKE; TAMBARA, RODRIGO VARELLA, SEIDEL, ALYSSON RANIERE, "**Analysis and Design of the LLC LED Driver Based on State-Space Representation Direct Time-Domain Solution**, *IEEE TRANSACTIONS ON POWER ELECTRONICS*, v.35, N.12, Dec. 2020.

Paper with recommendation for publication on periodicals:

1. MENKE, MAIKEL FERNANDO; ALONSO, J. MARCOS, TAMBARA, RODRIGO VARELLA, SEIDEL, ALYSSON RANIERE, "**Hybrid Dual-Loop Control for Current Regulation and Low-frequency Ripple Rejection in LED Drivers**", *REVISTA ELETRÔNICA DE POTÊNCIA*; Recommended publication on 18-Aug-2021.

Papers published in conference proceedings:

1. MENKE, MAIKEL FERNANDO; TAMBARA, RODRIGO VARELLA ; SEIDEL, Álysson Raniere. "**Controle Adaptativo por Modelo de Referência em Tempo Discreto Aplicado ao Conversor CC-CC LLC Ressonante Alimentando uma Carga LED**". In: IEEE/IAS International Conference on Industry Applications, 2018, São Paulo - SP. 13th IEEE/IAS International Conference on Industry Applications, 2018.

2. MENKE, MAIKEL FERNANDO; BISOGNO, FÁBIO ECKE ; TAMBARA, RODRIGO VARELLA ; SEIDEL, Álysson Raniere. **"Solução no Domínio do Tempo do Conversor CC-CC LLC Ressonante"**. In: IEEE/IAS International Conference on Industry Applications, 2018, São Paulo - SP. 13th IEEE/IAS International Conference on Industry Applications, 2018.

3. MENKE, MAIKEL FERNANDO; TAMBARA, RODRIGO VARELLA ; SEIDEL, Álysson Raniere,**"Model Reference Adaptive Control in Discrete-time Applied on the LLC LED Driver"**. In: Congresso Brasileiro de Automática, 2018, João Pessoa - PB. XXII Congresso Brasileiro de Automática - CBA2018, 2018.

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APPENDIX A - LLC RESONANT LED DRIVER DESIGN BASED ON FHA

This appendix presents the LLC resonant LED driver classical design procedure. In this procedure, the LLC resonant converter analysis is based on the FHA.

A.1 CONVENTIONAL LLC RESONANT LED DRIVER DESIGN

2 | *FHA-LLC-LED-DRIVER-design.nb*

LLC resonant LED driver design Classical design employing First Harmonic Approximation

Maikel Fernando Menke
Federal University of Santa Maria

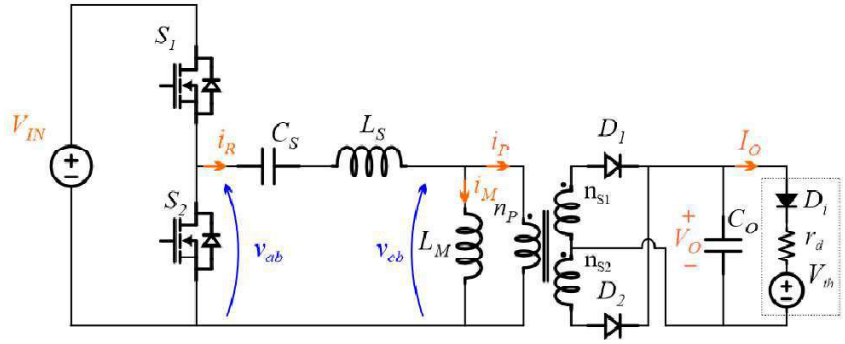


Figure 1.1. LLC LED driver circuit

1.1. Script instructions

Cels with light brown backcolor are comments.
Cells with light blue backcolor are evaluatable cells.
Cells with light purple backcolor are evaluatable cells, however, the variable value must be manually defined.
Press SHIFT+ENTER do evaluate each cell or ENTER from numeric keypad.

1.2. Universal Plot configuration

In[360]:=

```
Remove["Global`*"]
PlotStyle1 = Sequence @@ {
    Frame → True, LabelStyle → {FontFamily → "Times New Roman", 16, Black},
    ImageSize → {500, 400}, AspectRatio → 0.6, GridLines → Automatic,
    GridLinesStyle → Directive[Gray, Dashed], FrameStyle → Directive[Thickness[0.0025]]};
```

1.3. Converter specifications

In[ ]:=
```
Vbus = 400; (*Nominal bus votlage*)
Vinmin = 360; (*Minimal bus voltage*)
Vinmax = 420; (*Maximum bus voltage*)
fo = 100 000; (*LLC main resonance*)
fs = fo;
```

- **Application specifications**

In[ ]:=
```
Io = 1.15;(*Nominal output current*)
Iomax = Io;
Iomin = 0.2; (*Minimal output current*)
```

- **Initial calculations**

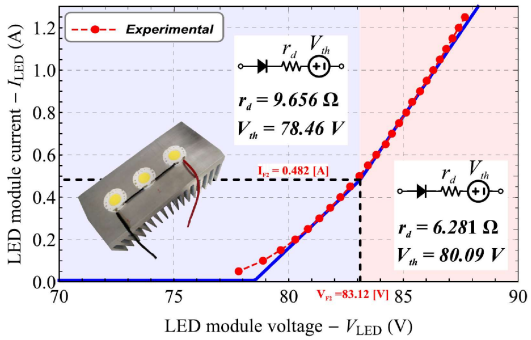


Figure 1.2. LED module i-v curve

In[ ]:=
```
rdL = 9.656; VthL = 78.46;
rdH = 6.281; VthH = 80.09;
Ith = 0.482;

rd = rdH; Vth = VthH; (*Nominal LED equivalent circuit model parameters*)

vLED[iLED_] = Which[iLED > Ith, iLED rdH + VthH,
    iLED ≤ Ith, iLED rdL + VthL];

Vo = vLED[Io];(*Nominal output voltage*)
Vomax = vLED[Iomax];(*Nominal output voltage*)
Vomin = vLED[Iomin]; (*Minimal output voltage*)
Po = Io Vo; (*Nominal output power*)
Pomin = Iomin Vomin; (*Minimal output power*)
RL = Vo/Io;

Print["Nominal LED current = ", Io];
Print["Nominal Module Voltage =", Vo];
Print["Nominal output power = ", Po];
Print["Minimal output current = ", Iomin];
Print["Minimal module voltage = ", Vomin];
Print["Minimal output power = ", Pomin];
```

```
Nominal LED current = 1.15

Nominal Module Voltage =87.3132

Nominal output power = 100.41

Minimal output current = 0.2

Minimal module voltage = 80.3912

Minimal output power = 16.0782
```

- **Semiconductor specifications specifications**

In[ ]:=
```
(*Coss=280  10^-12;*) (*IPD60R280P7S*)
Coss = 150 × 10^-12; (*STD10NM60N*)
```

1.4. Design procedure

1.4.1. Turns ratio design

In[ ]:=
```
n = Vbus / (2 (Vo)); Print["n = ", n]
```

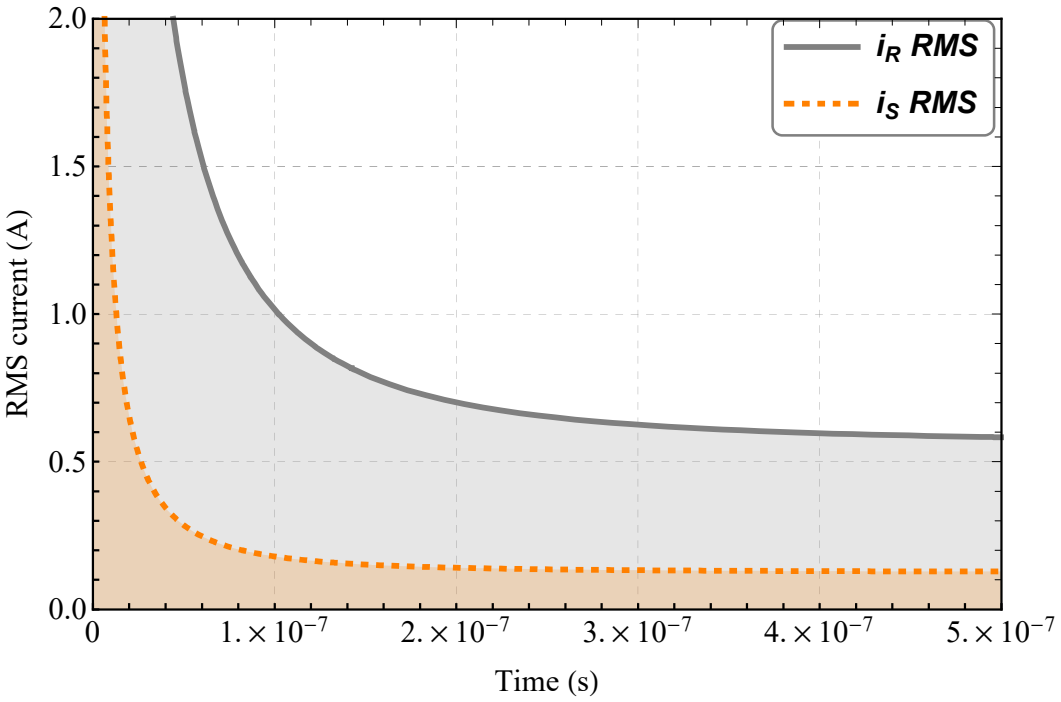
```
n = 2.29061
```

- Turns ratio is designed based on the nominal input voltage and output voltage, which is assumed as the most common operating condition and high efficiency at resonant point is desired. Therefore, the LED driver is designed to achieve high efficiency under normal condition. Consequently, the design of transformer's turns ratio should make the converter operate close to the resonant frequency under normal condition, which is the most efficient operating point of LLC resonant converter.

1.4.2. Dead-time Analysis

In[ ]:=
```
ip[td_] = 1/8 Vo/(n RL) Sqrt[ 2 n^4 RL^2 (1/fs)^2 / (1/fs td/(16 Coss))^2 + 8 π^2 ] ; (*Resonant tank RMS current*)

is[td_] = 1/4 Vo/(n RL) Sqrt[ (5 π^2 - 48)/(12 π^2) n^4 RL^2 (1/fs)^2 / (1/fs td/(16 Coss))^2 + 1 ] ; (*Secondary RMS current*)

Plot[{ip[td], is[td]}, {td, 0, 500 × 10^-9},
 PlotRange → {{0, 500 × 10^-9}, {0, 2}},
 PlotStyle → {{Gray, AbsoluteThickness[3]}, {Orange, AbsoluteThickness[3], Dashed}},
 PlotLegends → Placed[LineLegend[{"i_R RMS", "i_S RMS"},
    LabelStyle → {Black, Bold, Italic, 16},
    LegendLayout → {"Column", 1},
    LegendFunction → ((Framed[#, FrameMargins → 0, Background → White,
         RoundingRadius → 5, FrameStyle → Gray] &))], {0.87, 0.9}],
 FrameLabel → {{"RMS current (A)", None}, {"Time (s)", None}},
 Filling → Axis,
 Evaluate@PlotStyle1]
```

Out[ ]=



1.4.3. Define optimal dead-time based on plot

- Analyzing the relationship between dead-time and primary and secondary side RMS currents, the dead-time is chosen to minimize the total conduction loses. As it will be seen, the magnetizing inductance value is determined based on the dead-time and Coss of the half-bridge MOSFETs.

In[ ]:=
```
td = 300 × 10^-9;
```

1.4.4. Magnetizing inductance design

In[ ]:=
```
LmC = N[ (1/fo) td / (16 Coss) ];
Print["Critical L_M = ", LmC];(*Critical magnetizing inductance*)
```

```
Critical L_M = 0.00125
```

- Magnetizing inductance must be smaller that the critical value above calculated

In[ ]:=
```
Lm = 633 × 10^-6; (*Selected Lm*)
```

1.4.5. Ln and Q analysis

- In this section the LLC LED driver current gain is evaluated employing different normalized parameters. Details of this analysis and further informations, please see reference A.

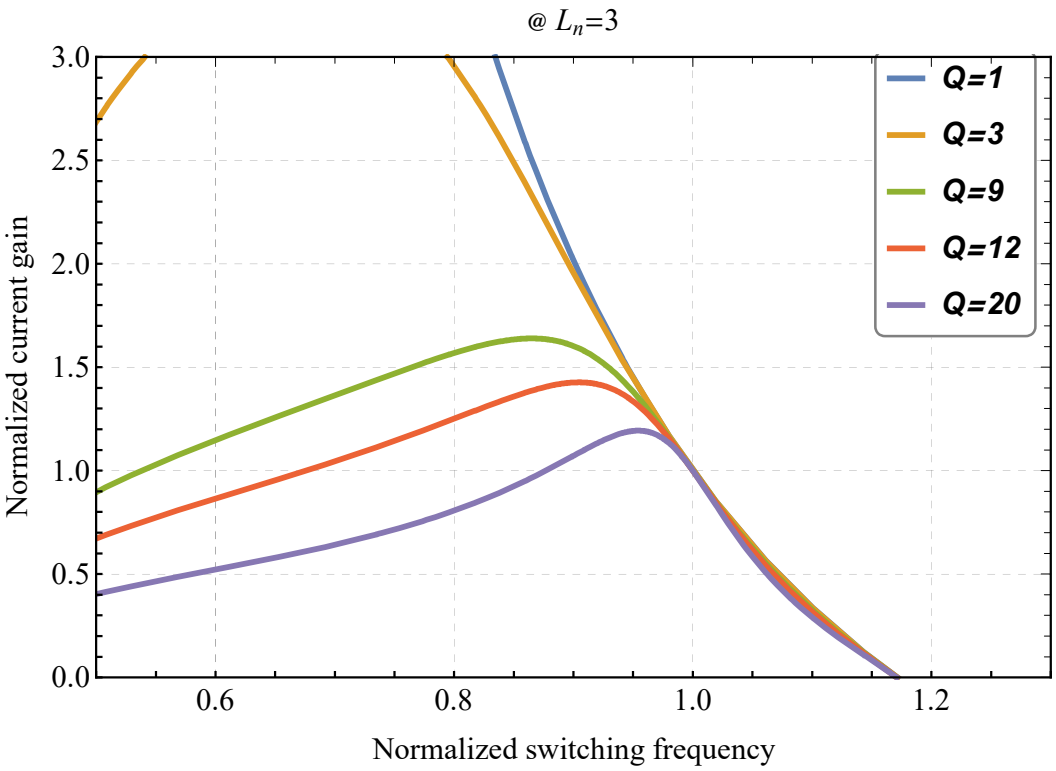
In[ ]:=

$$\mathrm{Ai_{on}}[\mathrm{Lnx\_},\ \mathrm{fnx\_},\ \mathrm{Qx\_},\ \mathrm{Vbusx\_},\ \mathrm{Vthx\_},\ \mathrm{nx\_}] = \left(2\,\mathrm{nx}\left(-\left(1+\frac{1-\frac{1}{\mathrm{fnx}^2}}{\mathrm{Lnx}}\right)^2+\sqrt{\left(\left(1+\frac{1-\frac{1}{\mathrm{fnx}^2}}{\mathrm{Lnx}}\right)^4-\left(\left(1+\frac{1-\frac{1}{\mathrm{fnx}^2}}{\mathrm{Lnx}}\right)^2+\left(\frac{1}{\mathrm{fnx}}-\mathrm{fnx}\right)^2\mathrm{Qx}^2\right)\left(\left(1+\frac{1-\frac{1}{\mathrm{fnx}^2}}{\mathrm{Lnx}}\right)^2-\frac{\mathrm{Vbusx}^2}{4\,\mathrm{nx}^2\,\mathrm{Vthx}^2}\right)\right)}\right)\mathrm{Vthx}\right)\Big/\left(\left(\left(1+\frac{1-\frac{1}{\mathrm{fnx}^2}}{\mathrm{Lnx}}\right)^2+\left(\frac{1}{\mathrm{fnx}}-\mathrm{fnx}\right)^2\mathrm{Qx}^2\right)(\mathrm{Vbusx}-2\,\mathrm{nx}\,\mathrm{Vthx})\right);$$

■ Current gain for different Q values

In[ ]:=
```
Plot[{
  Ai_on[3, fnx, 1, 400, Vth, n],
  Ai_on[3, fnx, 3, 400, Vth, n],
  Ai_on[3, fnx, 9, 400, Vth, n],
  Ai_on[3, fnx, 12, 400, Vth, n],
  Ai_on[3, fnx, 20, 400, Vth, n]}, {fnx, 0, 2},
 PlotStyle → AbsoluteThickness[3],
 PlotRange → {{0.5, 1.3}, {0, 3}},
 PlotLegends → Placed[LineLegend[{"Q=1", "Q=3", "Q=9", "Q=12", "Q=20"},
    LabelStyle → {Black, Bold, Italic, 16},
    LegendLayout → {"Column", 1},
    LegendFunction → ((Framed[#, FrameMargins → 0, Background → White,
         RoundingRadius → 5, FrameStyle → Gray] &))], {0.9, 0.78}],
 FrameLabel → {{"Normalized current gain", None},
   {"Normalized switching frequency", "@ Ln=3"}},
 Evaluate@PlotStyle1]
```

Out[ ]=



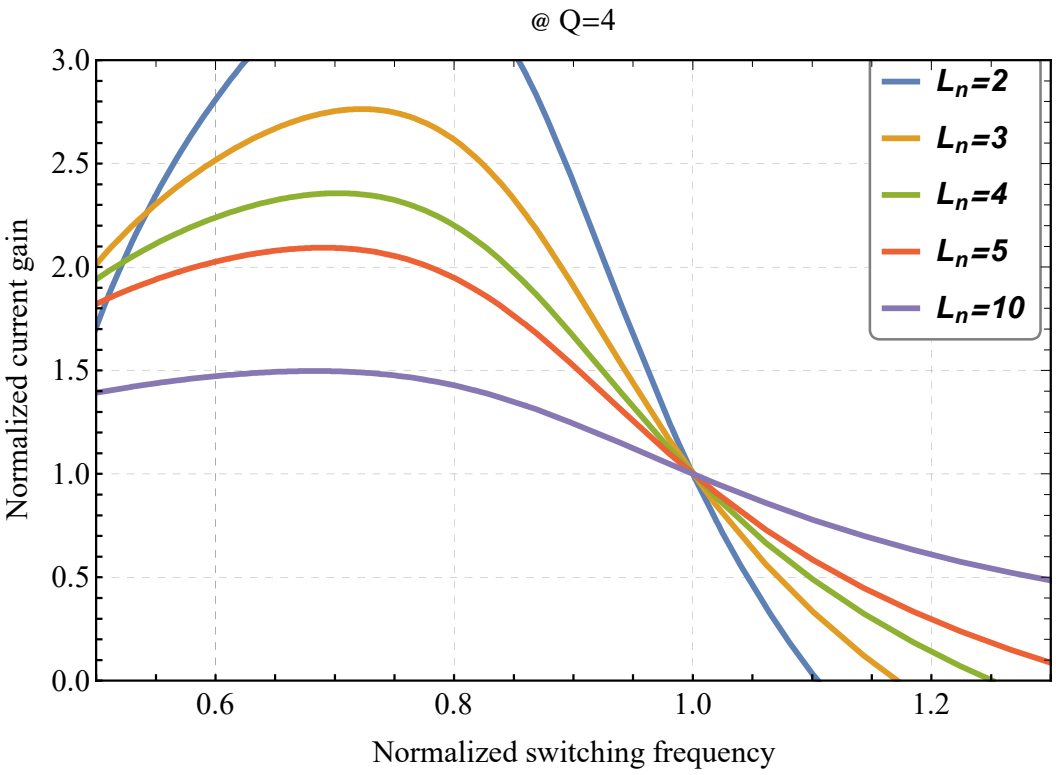
- As it can be seen in the plot above, for a constant L_n value, the quality factor has a low influence over the operating range, impacting only in the peak gain current.

■ Current gain for different L_n values

In[ ]:=

```
Plot[{
  Ai_on[2, fnx, 4, 400, Vth, n],
  Ai_on[3, fnx, 4, 400, Vth, n],
  Ai_on[4, fnx, 4, 400, Vth, n],
  Ai_on[5, fnx, 4, 400, Vth, n],
  Ai_on[10, fnx, 4, 400, Vth, n]}, {fnx, 0, 2},
 PlotStyle → AbsoluteThickness[3],
 PlotRange → {{0.5, 1.3}, {0, 3}},
 PlotLegends → Placed[LineLegend[{"Ln=2", "Ln=3", "Ln=4", "Ln=5", "Ln=10"},
    LabelStyle → {Black, Bold, Italic, 16},
    LegendLayout → {"Column", 1},
    LegendFunction → ((Framed[#, FrameMargins → 0, Background → White,
         RoundingRadius → 5, FrameStyle → Gray] &))], {0.9, 0.78}],
 FrameLabel → {{"Normalized current gain", None},
   {"Normalized switching frequency", "@ Q=4"}},
 (*Filling→Axis,*)
 Evaluate@PlotStyle1]
```

Out[ ]=



- The impact of L_n and Q on the converter behavior is investigated in order to found some design criteria. The shape of these curves changes and hence impact the converter operation mainly under dimming conditions. Smaller L_n value, the narrower the switching frequency range under dimming condition. As higher L_n wider will be the switching frequency range. Reducing L_M reduces L_n. However, reducing L_M increases the switch turn-off current at resonance. There is a trade-off between switching frequency range and switch turn-off current.
- In addition, the combination of L_n and Q impact on the current gain. It is necessary to assess the values of L_n and Q that provide enough current gain within the whole operating range (Output and input variation). Actually, we must ensure that the LLC converter will provide 100% constant current under worst condition V_{IN-MIN} and $V_{OUT-MAX}$

- Design criteria:
  * Smaller L_n is preferred because narrower f_{sw} range can be achieved.
  * Input voltage and output voltage variation also needs to be considered.
  * Minimum input and maximum output correspond to the worst case for peak gain.

1.4.6. Ln and Q selection

- Based on the previous analysis, Ln=3 is selected in order to avoid a wide switching frequency range and also outcome in enough current gain under minimum input voltage.

In[•]:=
```
Ln = 3;
```

1.4.7. Resonant filter elements definition

In[•]:=
```
Ls = N[Lm / Ln]; Print["Ls = ", Ls];
```

```
Ls = 0.000211
```

- Since resonant frequency is given by $f_o = \frac{1}{2\pi\sqrt{L_s C_s}}$, we can solve this equation for Cs.

In[•]:=
```
Cs = N[1 / (4 π^2 Ls fo^2)]; Print["Cs = ", Cs];
```

```
Cs = 1.20049×10^-8
```

- In order to obtain commercial value for Cs, we can change the value of Ls around the previous value calculated until C_S converge to an commercial value

In[•]:=
```
Ls = 0.000211;
Cs = 1 / (4 π^2 Ls fo^2);

Lm = Ln Ls;
Print["Resonant filter parameters"]
Print["Cs = ", Cs]
Print["Ls = ", Ls]
Print["Lm = ", Lm]
```

```
Resonant filter parameters
Cs = 1.20049×10^-8
Ls = 0.000211
Lm = 0.000633
```

In[•]:=
```
Qc = Sqrt[Ls / Cs] / (8 n^2 rd / π^2); Print["Q = ", Qc]
```

```
Q = 4.96298
```

1.4.8. Output capacitor design

In[ ]:=
```
ΔVp = 0.25/100; (*Perceptual output voltage ripple*)
ΔVo = Vo ΔVp; (*Output voltage ripple*)
ΔiLEDHF = ΔVo/rd; (*High-frequency LED current ripple*)
Co = 0.21 Io/(ΔVo fs 2) (*Calculate Co*)
```

Out[ ]= 5.53181×10^{-6}

- Select Co greater than the value previously calculated

In[ ]:=
```
Co = 10×10^-6;
```

1.4.9. Converter operating window - Considering LED MBPWL equivalent circuit

- The LLC LED driver must have the capability to provide nominal current within the whole input and output ranges. It means, achieve peak current gain requirements. Therefore, in order to evaluate this feature, the converter output current under different input voltage is assessed.

In[ ]:=
```
i_LED[Vbusx_, fn_] =
Which[((((2 n (-(1 + (1 - 1/fn^2)/Ln)^2 + Sqrt((1 + (1 - 1/fn^2)/Ln)^4 - ((1 + (1 - 1/fn^2)/Ln)^2 + (1/fn - fn)^2 (Sqrt(Ls/Cs)/(8 n^2 rdH/π^2))^2))) ((1 + (1 - 1/fn^2)/Ln)^2 - Vbusx^2/(4 n^2 VthH^2)))) VthH)/
((((1 + (1 - 1/fn^2)/Ln)^2 + (1/fn - fn)^2 (Sqrt(Ls/Cs)/(8 n^2 rdH/π^2))^2) (Vbusx - 2 n VthH)) (Vbusx/(2 n) - VthH)/rdH) ≤ Ith,
((((2 n (-(1 + (1 - 1/fn^2)/Ln)^2 + Sqrt((1 + (1 - 1/fn^2)/Ln)^4 - ((1 + (1 - 1/fn^2)/Ln)^2 + (1/fn - fn)^2 (Sqrt(Ls/Cs)/(8 n^2 rdL/π^2))^2))) ((1 + (1 - 1/fn^2)/Ln)^2 - Vbusx^2/(4 n^2 VthL^2)))) VthL)/
```

$$\left(\left(\left(1+\frac{1-\frac{1}{fn^2}}{Ln}\right)^2+\left(\frac{1}{fn}-fn\right)^2\left(\frac{\sqrt{\frac{Ls}{Cs}}}{\frac{8\,n^2\,rdL}{\pi^2}}\right)^2\right)(Vbusx-2\,n\,VthL)\right)\frac{\frac{Vbusx}{2\,n}-VthL}{rdL},$$

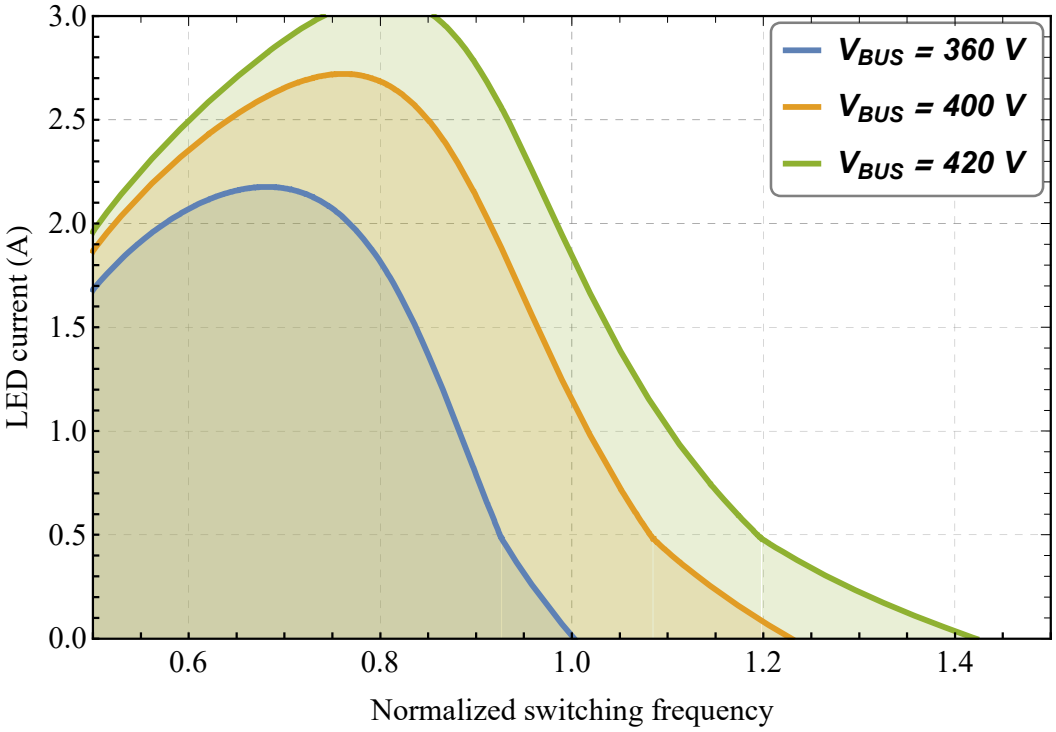
$$\left(\left(\left(2\,n\left(-\left(1+\frac{1-\frac{1}{fn^2}}{Ln}\right)^2+\sqrt{\left(1+\frac{1-\frac{1}{fn^2}}{Ln}\right)^4-\left(\left(1+\frac{1-\frac{1}{fn^2}}{Ln}\right)^2+\left(\frac{1}{fn}-fn\right)^2\left(\frac{\sqrt{\frac{Ls}{Cs}}}{\frac{8\,n^2\,rdH}{\pi^2}}\right)^2\right)\left(\left(1+\frac{1-\frac{1}{fn^2}}{Ln}\right)^2-\frac{Vbusx^2}{4\,n^2\,VthH^2}\right)}\right)VthH\right)\Big/\left(\left(\left(1+\frac{1-\frac{1}{fn^2}}{Ln}\right)^2+\left(\frac{1}{fn}-fn\right)^2\left(\frac{\sqrt{\frac{Ls}{Cs}}}{\frac{8\,n^2\,rdH}{\pi^2}}\right)^2\right)(Vbusx-2\,n\,VthH)\right)\frac{\frac{Vbusx}{2\,n}-VthH}{rdH}\right)>Ith,$$

$$\left(\left(\left(2\,n\left(-\left(1+\frac{1-\frac{1}{fn^2}}{Ln}\right)^2+\sqrt{\left(1+\frac{1-\frac{1}{fn^2}}{Ln}\right)^4-\left(\left(1+\frac{1-\frac{1}{fn^2}}{Ln}\right)^2+\left(\frac{1}{fn}-fn\right)^2\left(\frac{\sqrt{\frac{Ls}{Cs}}}{\frac{8\,n^2\,rdH}{\pi^2}}\right)^2\right)\left(\left(1+\frac{1-\frac{1}{fn^2}}{Ln}\right)^2-\frac{Vbusx^2}{4\,n^2\,VthH^2}\right)}\right)VthH\right)\Big/\left(\left(\left(1+\frac{1-\frac{1}{fn^2}}{Ln}\right)^2+\left(\frac{1}{fn}-fn\right)^2\left(\frac{\sqrt{\frac{Ls}{Cs}}}{\frac{8\,n^2\,rdH}{\pi^2}}\right)^2\right)(Vbusx-2\,n\,VthH)\right)\frac{\frac{Vbusx}{2\,n}-VthH}{rdH}\right)$$

```
  ];
Plot[{
  i_LED[Vinmin, fn],
  i_LED[Vbus, fn],
  i_LED[Vinmax, fn]}, {fn, 0.5, 2},
 PlotStyle → AbsoluteThickness[3],
 PlotRange → {{0.5, 1.5}, {0, 3}},
 PlotLegends → Placed[LineLegend[{"V_BUS = 360 V", "V_BUS = 400 V", "V_BUS = 420 V"},
    LabelStyle → {Black, Bold, Italic, 16},
    LegendLayout → {"Column", 1},
    LegendFunction → ((Framed[#, FrameMargins → 0, Background → White,
        RoundingRadius → 5, FrameStyle → Gray] &))], {0.85, 0.85}],
```

```
FrameLabel → {{"LED current (A)", None}, {"Normalized switching frequency", None}},
Filling → Axis,
Evaluate@PlotStyle1]
```

Out[ ]=



- Based on the plot above, it can be seen that the design filter provides enough current gain for minimum input voltage. In addition, for the maximum input voltage and minimum output current, a feasible switching frequency is noticed.

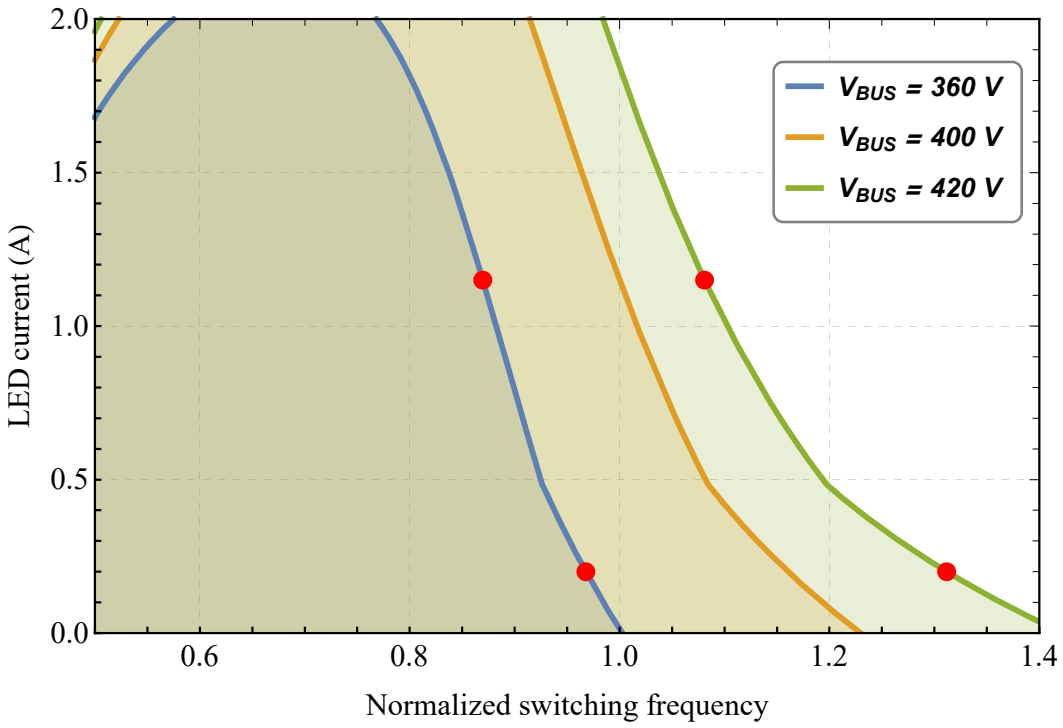
In[ ]:=

```
fsminx = FindRoot[iLED[Vinmin, fn] == 1.15, {fn, 0.89}];
fsmin = fsminx[[1, 2]] fo ;
fsmaxx = FindRoot[iLED[Vinmax, fn] == Iomin, {fn, 1}];
fsmax = fsmaxx[[1, 2]] fo ;

Print["Minimum switching frequency = ", fsmin];
Print["Maximum switching frequency = ", fsmax];
```

```
Minimum switching frequency = 86968.3

Maximum switching frequency = 131175.
```

In[ ]:=
```
fsmaxVminx = FindRoot[iLED[Vinmin, fn] == 0.2, {fn, 0.99}];
fsmaxVmin = fsmaxVminx[[1, 2]] fo ;
fsminVmaxx = FindRoot[iLED[Vinmax, fn] == 1.15, {fn, 0.99}];
fsminVmax = fsminVmaxx[[1, 2]] fo ;

P1 = Plot[{
     iLED[Vinmin, fn],
     iLED[Vbus, fn],
     iLED[Vinmax, fn]}, {fn, 0.5, 2},
    PlotStyle → AbsoluteThickness[3],
    PlotRange → {{0.5, 1.4}, {0, 2}},
    PlotLegends →
     Placed[LineLegend[{"VBUS = 360 V", "VBUS = 400 V", "VBUS = 420 V"},
       LabelStyle → {Black, Bold, Italic, 14},
       LegendLayout → {"Column", 1}, LegendFunction → ((Framed[#, FrameMargins → 0,
            Background → White, RoundingRadius → 5, FrameStyle → Gray] &))], {0.85, 0.8}],
    FrameLabel → {{"LED current (A)", None}, {"Normalized switching frequency", None}},
    Filling → Axis, Exclusions → None,
    Evaluate@PlotStyle1];

P2 = ListPlot[{{fsmin/fo, Io}, {fsmax/fo, Iomin}, {fsmaxVmin/fo, Iomin}, {fsminVmax/fo, Io}},
    PlotStyle → Directive[Red, PointSize[0.02]]];
Show[
 P1,
 P2]
```

Out[ ]=



1.4.10. Magnetic elements specification

- **Maximum current levels on the magnetic elements + 10%**

In[ ]:=

```
(* The maximum filter current is noticed at
 the minimum input voltage and nominal output power*)
ψ = 1.2;(*fator de aumento da corrente no projeto dos magnéticos*)

Zin[fsw_] := i 2 π fsw Ls + 1/(i 2 π fsw Cs) + (i 2 π fsw Lm (8 n^2/π^2) Vo/Io)/(i 2 π fsw Lm + (8 n^2/π^2) Vo/Io);

iRrms = (Vbus √2/π)/Abs[Zin[fo]];(*Nominal resonant tank RMS current*)

(*iR=1/8 Vo/(n RL) √(2 n^4 RL^2 (1/fs)^2/(Lm)^2+8 π^2) ;*)

iRpk = iRrms √2 ;(*Nominal resonant tank  peak current*)

iRrmsMax = (Vinmin √2/π)/Abs[Zin[fsmin]] ψ;(*Maximum filter RMS current + 10%*)

iRpkMax = iRrmsMax √2 ;(*Maximum filter peak current + 10%*)

iSecRMS = Io π/4 1.1;(*Each secondary RMS current + 10%*)
iSecPk = iSecRMS 2; (*each secondary peak current + 10%*)

Print["Resonant filter maximum RMS current = ", iRrmsMax]
Print["Resonant filter maximum peak current = ", iRpkMax]
Print["Secondary RMS current = ", iSecRMS];
Print["Secondary peak current = ", iSecPk];
```

```
Resonant filter maximum RMS current = 0.915432

Resonant filter maximum peak current = 1.29462

Secondary RMS current = 0.993529

Secondary peak current = 1.98706
```

- **Magnetic core parameters**

In[ ]:=
```
JL = 400;
Bmax = 0.35; (*Core maximum flux density – Thorton IP6 @80 °C*)
KwLs = 0.7; (*window utilization factor*)
KwTrx = 0.5; (*fator de ocupação da janela do trafo – 0.5 usual*)
KpTrx = 0.4; (*fator de utilização do primário*)
χskin = 1.65; (*Increase of conductor cross section area due to Litz wires*)

(* >>>>>>        Banco de dado para projeto dos magnéticos <<<<<<      *)
(*
Core data EE =[ NEE –  Ae(cm2) – AeAw(cm4)  – CME (cm) – Ve(cm3) – Aw(cm²)  ],
CME – caminho médio da espira mean-length-per-turn ;
AWG = AWG, area cobre cm2, ohm/cm 100C;
*)

EE = {{"EE.20/10/5", 0.31, 0.08, 3.8, 1.340, 0.26},
      {"EE.25/10/6", 0.39, 0.17, 4.2, 1.910, 0.62},
      {"EE.30/15/7", 0.6, 0.48, 5.6, 4.000, 0.80},
      {"EE.30/15/14", 1.2, 1.02, 6.7, 8.000, 0.85},
      {"EE.40/17/12", 1.48, 1.5, 7.5, 11.396, 1.02},
      {"EE.42/15", 1.81, 2.84, 8.7, 17.100, 1.57},
      {"EE.42/20", 2.4, 3.77, 10.5, 23.300, 1.57},
      {"EE55", 3.54, 8.85, 11.6, 42.5, 2.5}};

AWG = {{"AWG.13", 0.026243, 0.000088, 0.029793},
       {"AWG.14", 0.020811, 0.000111, 0.023800},
       {"AWG.15", 0.016504, 0.000140, 0.019021},
       {"AWG.16", 0.013088, 0.000176, 0.105207},
       {"AWG.17", 0.010379, 0.000222, 0.012164},
       {"AWG.18", 0.008231, 0.000280, 0.009735},
       {"AWG.19", 0.006527, 0.000353, 0.007794},
       {"AWG.20", 0.005176, 0.000445, 0.006244},
       {"AWG.21", 0.004105, 0.000561, 0.005004},
       {"AWG.22", 0.003255, 0.000708, 0.004013},
       {"AWG.23", 0.002582, 0.000892, 0.003221},
       {"AWG.24", 0.002047, 0.001125, 0.002586},
       {"AWG.25", 0.001624, 0.001419, 0.002078},
       {"AWG.26", 0.001287, 0.001789, 0.001671},
       {"AWG.27", 0.001021, 0.002256, 0.001344},
       {"AWG.28", 0.000810, 0.002845, 0.001083},
       {"AWG.29", 0.000642, 0.003587, 0.000872},
       {"AWG.30", 0.000509, 0.004523, 0.000704},
       {"AWG.31", 0.000404, 0.005704, 0.000568},
       {"AWG.32", 0.000320, 0.007192, 0.000459},
       {"AWG.33", 0.000254, 0.009070, 0.000371},
       {"AWG.34", 0.000201, 0.011437, 0.000300},
       {"AWG.35", 0.000160, 0.014422, 0.000243},
       {"AWG.36", 0.000127, 0.018186, 0.000197},
       {"AWG.37", 0.000100, 0.022932, 0.000160}};
```

- **Inductor Ls design**

In[ ]:=
```
(* >>> Determine inductor wire gauge <<<*)
Clear[STLs, AWGmin, AWGi, LsAWG, ρLs, AWGok];
STLs = iRrmsMax / JL; (*Inductor conductor required cross section area*)
AWGmin = STLs;
```

```
AWGi = 0;

For[AWGi = Length[AWG], AWGi ≥ 1, AWGi -- ,
      AWGLs = AWG[[AWGi, 2]];
      If[AWGLs ≥ AWGmin, AWGok = AWGi; AWGi = 0];
 ];

LsAWG = AWG[[AWGok, 1]]; (*Selected inductor wire gauge*)
ρLs = AWG[[AWGok, 3]];
Print["Inductor wire gauge = ", LsAWG]
(* >>> Determine inductor magnetic core EE<<< *)
Clear[EEi, AeAwmin, AeAwLs, LsNEE, LsAe, LsVe, LsCME, EEok];

AeAwmin = Ls iRrmsMax iRpkMax / (Bmax JL KwLs) 10 000;
For[EEi = 1, EEi ≤ Length[EE], EEi++,
  AeAwLs = EE[[EEi, 3]];
  If[AeAwLs ≥ AeAwmin, EEok = EEi;
   EEi = Length[EE]];
 ];
Print["Initial inductor EE core = ", EE[[EEok, 1]]];
(* calcula posibilidade de execução*)
Clear[ExcLs];
ExcLs = 2;

While[ExcLs > 1,
          LsNEE = EE[[EEok, 1]];
          LsAe = EE[[EEok, 2]];
          LsVe = EE[[EEok, 5]];
          LsCME = EE[[EEok, 4]];
          (* >>> Define inductor number of turns <<<*)
          NeLs = iRpkMax Ls / (LsAe Bmax) 10 000;
          rdcLs = ρLs LsCME NeLs;
          (* >>> Evaluate execution possibility <<<*)
          Awmin = NeLs AWG[[AWGok, 4]] χskin / KwLs;
          Clear[ExcLs];
          ExcLs = Awmin / EE[[EEok, 6]];
          If[ExcLs > 1,
           EEok = EEok + 1;
       ];
 ];
Print["Inductor core = ", LsNEE];
Print["Inductor number of turns = ", NeLs];
Print["Inductor execution factor = ", ExcLs];
```

```
Inductor wire gauge = AWG.23

Initial inductor EE core = EE.20/10/5

Inductor core = EE.20/10/5
```

```
Inductor number of turns = 25.1764

Inductor execution factor = 0.735186
```

- **Transformer design**

In[ ]:=

```
(* >>> Determine transformer winding wire gauge <<<*)
NpAWG = LsAWG;
ρnp = ρLs;
STnp = STLs;

STTrxNs = iSecRMS / JL;
AWGmin = STTrxNs;
AWGi = 0;
For[AWGi = Length[AWG], AWGi ≥ 1, AWGi -- ,
      AWGNs = AWG[[AWGi, 2]];
      If[AWGNs ≥ AWGmin, AWGok = AWGi;
       AWGi = 0];
 ];
NsAWG = AWG[[AWGok, 1]];
ρns = AWG[[AWGok, 3]];
 STns = AWG[[AWGok, 4]];

Print["Transformer primary coil wire gauge = ", NpAWG];
Print["Transformer secondary coil wire gauge = ", NsAWG];

(* >>> Determine transformer magnetic core EE<<< *)
Clear[EEi, AeAwmin, AeAwTrx, EEok, TrxNEE, TrxAe, TrxVe, TrxCME];

AeAwmin = iRrmsMax Vo n / (2 JL KwTrx KpTrx Bmax fsmin) 10 000;

(*     AeAwmin= iRRMSMAX n Vo / (2 JL KwTrx KpTrx Bmax fsw);*)

For[EEi = 1, EEi ≤ Length[EE], EEi ++,
   AeAwTrx = EE[[EEi, 3]];
   If[AeAwTrx ≥ AeAwmin, EEok = EEi;
    EEi = Length[EE]];
 ];

Print["Initial transformer EE core = ", EE[[EEok, 1]]];

Clear[ExcTrx];
ExcTrx = 2;

While[ExcTrx > 1,
      TrxNEE = EE[[EEok, 1]];
      TrxAe = EE[[EEok, 2]];
      TrxVe = EE[[EEok, 5]];
      TrxCME = EE[[EEok, 4]];

      (* >>> Projeta np <<<*)
```

```
np = (Vo n)/(2 fsmin TrxAe Bmax) 10000; (*np=(Vo n)/(2 fsw TrxAe Bmax);*)

rdcnp = ρnp TrxCME np;
ns = np/n;
rdcns = ρns TrxCME ns;

(* >>> Testa possibilidade de execução <<<*)
AwminTrx = ((np STnp + 2 ns STns)/KwTrx) χskin;
Clear[ExcTrx];
ExcTrx = AwminTrx/EE[[EEok, 6]];
If[ExcTrx > 1,
 EEok = EEok + 1;
 ];
];
Print["Final Tranformer core = ", TrxNEE];
Print["Turns of wire on primary coil = ", np];
Print["Turns of wire on secondary coil = ", ns];
Print["Transformer execution factor = ", ExcTrx];
```

```
Transformer primary coil wire gauge = AWG.23
Transformer secondary coil wire gauge = AWG.23
Initial transformer EE core = EE.30/15/7
Final Tranformer core = EE.30/15/14
Turns of wire on primary coil = 27.3773
Turns of wire on secondary coil = 11.952
Transformer execution factor = 0.542169
```

- **Skin effect evaluation**

In[ ]:=

```
fsmax = fo 1.5;
fskin = 7.5;

Print["Inductor wire cross section area = ", STLs];
Print["Transformer primary coil wire cross section area = ", STnp];
Print["Transformer secondary coil wire cross section area = ", STTrxNs];
Print["Maximum switching frequency = ", fsmax]

Sskin = π (fskin / Sqrt[fsmax])^2 ;(*Conductor maximum cross section area*)
AWGmax = Sskin;
Print["Maximum cross section to avoid skin effect = ", AWGmax]
AWGi = 0;

For[AWGi = 1, AWGi ≤ Length[AWG], AWGi++,
      AWGskin = AWG[[AWGi, 2]];
      If[AWGskin ≤ AWGmax, AWGok = AWGi; AWGi = Length[AWG] + 1];
 ];
STskin = AWG[[AWGok, 2]];
AWGskin = AWG[[AWGok, 1]];
Print["Required AWG to avoid skin effect = ", AWGskin]
Print["Cross section of the wire = ", STskin]
NpPar = STnp / STskin;
NsPar = STTrxNs / STskin;
Print["Number of wires in parallel for inductor = ", NpPar];
Print["Number of wires in parallel for transformer primary coil = ", NpPar];
Print["Number of wires in parallel for transformer secondary coil = ", NsPar];
```

```
Inductor wire cross section area = 0.00228858
Transformer primary coil wire cross section area = 0.00228858
Transformer secondary coil wire cross section area = 0.00248382
Maximum switching frequency = 150000.
Maximum cross section to avoid skin effect = 0.0011781
Required AWG to avoid skin effect = AWG.27
Cross section of the wire = 0.001021
Number of wires in parallel for inductor = 2.24151
Number of wires in parallel for transformer primary coil = 2.24151
Number of wires in parallel for transformer secondary coil = 2.43273
```

In[ ]:=
```
(*For a wire gauge thinner*)
AWGok = AWGok + 1;
STskin = AWG[[AWGok, 2]];
AWGskin = AWG[[AWGok, 1]];
Print["Required AWG to avoid skin effect = ", AWGskin]
Print["Cross section of the wire = ", STskin]
NpPar = STnp / STskin;
NsPar = STTrxNs / STskin;
Print["Number of wires in parallel for inductor = ", NpPar];
Print["Number of wires in parallel for transformer primary coil = ", NpPar];
Print["Number of wires in parallel for transformer secondary coil = ", NsPar];
```

1.5. Designed converter

In[ ]:=
```
Print[Style["DESIGNED LLC LED DRIVER CONVERTER", 16, Bold, Red]];
Print["Nominal bus voltage = ", Vbus];
Print["Minimum input bus voltage = ", Vinmin];
Print["Maximum input bus voltage = ", Vinmax];
Print["Nominal output current = ", Io];
Print["Minimum output current = ", Iomin];
Print["Nominal switching frequency = ", fo];
Print[Style["Nominal switcing frequency correspond to main resonance", Italic, 10]]
Print["Switching frequency @ Vinmin and rated Io -> fsmin = ", fsmin];
Print["Switching frequency @ Vinmax and Iomin -> fsmax = ", fsmax];
Print["Cs = ", Cs];
Print[Style["----- Inductor specifications -----", 12, Bold, Blue]]
Print["Ls = ", Ls];
Print["Indutor core = ", LsNEE];
Print["Inductor coil number of turns = ", NeLs];
Print["Inductor wire gauge = ", AWGskin]
Print["Number os parallel wires = ", NpPar]
Print["Inductor execution factor = ", ExcLs];
Print[Style["----- Transformer specifications -----", 12, Bold, Blue]]
Print["Transformer core = ", TrxNEE];
Print["Transformer wire gauge = ", AWGskin]
Print["Primary coil number of turns = ", N[np]];
Print["Number os parallel wires = ", NpPar]
Print["Secondary coil number of turns = ", N[ns]];
Print["Number os parallel wires = ", NsPar]
Print["Transformer execution factor = ", ExcTrx];
Print["Lm = ", Lm];
```

DESIGNED LLC LED DRIVER CONVERTER

Nominal bus voltage = 400

Minimum input bus voltage = 360

Maximum input bus voltage = 420

Nominal output current = 1.15

Minimum output current = 0.2

Nominal switching frequency = 100 000

Nominal switcing frequency correspond to main resonance

Switching frequency @ Vinmin and rated Io -> fsmin = 86 968.3

Switching frequency @ Vinmax and Iomin -> fsmax = 150 000.

$C_S = 1.20049 \times 10^{-8}$

----- Inductor specifications -----

$L_S = 0.000211$

Indutor core = EE.20/10/5

Inductor coil number of turns = 25.1764

Inductor wire gauge = AWG.27

Number os parallel wires = 2.24151

Inductor execution factor = 0.735186

----- Transformer specifications -----

Transformer core = EE.30/15/14

Transformer wire gauge = AWG.27

Primary coil number of turns = 27.3773

Number os parallel wires = 2.24151

Secondary coil number of turns = 11.952

Number os parallel wires = 2.43273

Transformer execution factor = 0.542169

$L_M = 0.000633$

1.6. References

A. Wu, H. (2011). Multi-Channel Constant Current LED Driver for Indoor LED Luminaries. Faculty of the Virginia Polytechnic Institute.

B. Wu, H., Ji, S., Lee, F. C., & Wu, X. (2011). Multi-channel constant current (MC3) LLC resonant LED driver. IEEE Energy Conversion Congress and Exposition-ECCE, 2568–2575. https://doi.org/10.1109/ECCE.2011.6064111

APPENDIX B - WOLFRAM MATHEMATICA EXAMPLE CODE

This appendix presents an example of the code developed in Wolfram Mathematica v.12 to analyze the LLC resonant LED driver under the time-domain, where it is assumed the operation at PO mode. Appendix G provides the access to this Mathematica notebook.

B.1 LLC RESONANT LED DRIVER - PO MODE TD SOLUTION

LLC resonant LED driver time-domain analysis for PO mode

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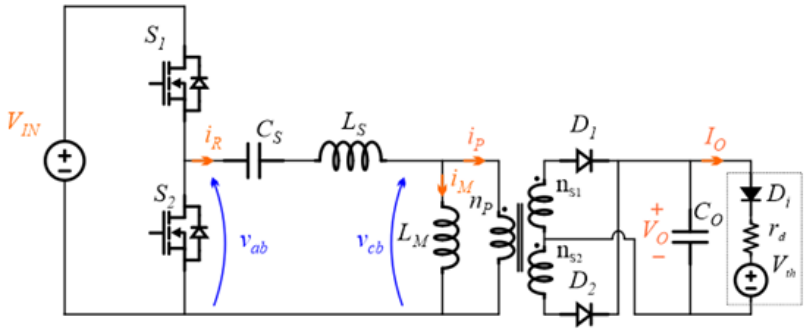


Figure 1.1. DC/DC LLC resonant LED driver

1.1. Analytic time-domain solution for PO mode

1.1.1. Resonant stages matrices

In[1]:=

```
Remove["Global`*"];
Off[General::stop];

to = 0;
u = {{Vin}, {Vth}};

AP = {{0, -1/Ls, 0, -n/Ls}, {1/Cs, 0, 0, 0}, {0, 0, 0, n/Lm}, {n/Co, 0, -n/Co, -1/(rd Co)}};
BP = {{1/Ls, 0}, {0, 0}, {0, 0}, {0, 1/(rd Co)}};
AO = {{0, -1/(Ls+Lm), 0, 0}, {1/Cs, 0, 0, 0}, {0, -1/(Ls+Lm), 0, 0}, {0, 0, 0, -1/(rd Co)}};

BO = {{1/(Ls+Lm), 0}, {0, 0}, {1/(Ls+Lm), 0}, {0, 1/(rd Co)}};
AOr = {{0, -1/(Ls+Lm), 0}, {1/Cs, 0, 0}, {0, 0, -1/(rd Co)}};
BOr = {{1/(Ls+Lm), 0}, {0, 0}, {0, 1/(rd Co)}};

Xo = {{Iro}, {Vcso}, {Imo}, {Vcoo}};
```

1.1.2. Zero-state and zero-input response for each step

In[8]:=

```
(*Solutions for step 1 given by stage P: [to, tz1]*)
ΦhS1Pt = MatrixExp[AP (t - to)];
ΦpS1Pt = Inverse[AP].(MatrixExp[AP (t - to)] - IdentityMatrix[Length[AP]]).BP .u;

(*Solutions for step 2 given by stage O: [tz1,tz2]*)
ΦhS2Otr = MatrixExp[AOr (t - tz1)];
ΦpS2Otr = Inverse[AOr].(MatrixExp[AOr (t - tz1)] - IdentityMatrix[Length[AOr]]).BOr .u;
```

1.1.3. State-space representation direct time-domain solution

In[12]:=

```
(* ------------------------------------------------------------------------ *)
(*Solutions for step 1 given by stage P: [to, tz1]*)
XS1Pt = ΦhS1Pt.Xo + ΦpS1Pt;
XS1Ptz1 = XS1Pt /. t → tz1;

(*Solutions for step 2 given by stage O: [tz1,tz2], preceded by stage P*)
XS2POtr = ΦhS2Otr.({{1, 0, 0, 0}, {0, 1, 0, 0}, {0, 0, 0, 1}}.XS1Ptz1) + ΦpS2Otr;
XS2POt = {XS2POtr[[1]], XS2POtr[[2]], XS2POtr[[1]], XS2POtr[[3]]};
XS2POtz2 = XS2POt /. t → tz2;
```

1.2. Converter parameters

In[17]:=
```
Vin = 400;
Ls = 253.3 × 10^-6;
Cs = 10 × 10^-9;
Co = 10 × 10^-6;
n = 2.6122;
Lm = 1393 × 10^-6;
fsw = 78 927;
dc = 0.5;

(*Expected output current *)
Io = 1.15;

(*LED module paramenters *)
If[Io > 0.482,
  rd = 6.22; Vth = 80.09;, (*high output*)
  rd = 9.656; Vth = 78.46 (*low output*)
 ];
```

1.3. Numerical time-domain solution

1.3.1. Initial definitions

In[27]:=
```
Ts = 1/fsw;
t1 = dc Ts;
t2 = Ts;
tz2 = t1;
fo = 1/(2 π √(Ls Cs));
ModeViolation = 0;
OperatingModeFound = 0;
```

1.3.2. Define initial guess for unknown variables

In[34]:=
```
Iro0 = -0.305;
Imo0 = -0.300;
Vcso0 = -220;
Vcoo0 = (Vth - 0.1);
tz10 = 4.69 × 10^-6 ;
```

1.3.3. Set up the system of equation to be numerically solved and find roots

In[39]:=

```
Clear[X0, Iro, Imo, Vcso, Vcoo, tz1];
XS1Ptv = XS1Pt;
XS1Ptz1v = XS1Ptz1;
XS2POtv = XS2POt;
XS2POtz2v = XS2POtz2;

X0 = FindRoot[{
     Re[XS2POtz2v[[1, 1]]] == -Iro,
     Re[XS2POtz2v[[3, 1]]] == -Imo,
     Re[XS2POtz2v[[2, 1]]] == (Vin - Vcso),
     Re[XS2POtz2v[[4, 1]]] == Vcoo,
     Re[XS1Ptz1v[[1, 1]]] == Re[XS1Ptz1v[[3, 1]]]},
    {Iro,  Iro0}, {Imo,  Imo0}, {Vcso, Vcso0},
    {Vcoo, Vcoo0}, {tz1, 0.9999 tz10}, MaxIterations → 200];

Iro = X0[[1, 2]];
Imo = X0[[2, 2]];
Vcso = X0[[3, 2]];
Vcoo = X0[[4, 2]];
tz1 = X0[[5, 2]];

Print[Style["State-vector initial values and tranzition time", 12, Blue]];
Print["Imo = ", Imo];
Print["Vcso = ", Vcso];
Print["Vcoo = ", Vcoo];
Print["tz1 = ", tz1];
```

State-vector initial values and tranzition time

Imo = -0.44167

Vcso = 39.8393

Vcoo = 87.2384

tz1 = 5.0887×10^{-6}

1.3.4. Validate operation with PO mode

In[55]:=

```
VLmtz1 = Lm/(Ls + Lm) (Vin - Re[XS1Ptz1v[[2, 1]]]);
VLmtz2n = Lm/(Ls + Lm) (0 - Re[XS2POtz2v[[2, 1]]]);
VLmtz2 = Lm/(Ls + Lm) (Vin - Re[XS2POtz2v[[2, 1]]]);

Vcotz1r = n Re[XS1Ptz1v[[4, 1]]];
Vcotz2r = n Re[XS2POtz2v[[4, 1]]];
iMtz2 = XS2POtz2v[[3, 1]];
iRtz2 = XS2POtz2v[[1, 1]];


If[fsw ≥ fo, ModeViolation = 1; Print[Style["# Error: fsw > fo", 12, Red]]];

If[tz1 ≤ 0, ModeViolation = 1;
  Print[Style["# Error: Mode violation - time constraints", 12, Red]]];

If[(Abs[Abs[Imo] - Abs[iMtz2]]) > 0.001, ModeViolation = 1;
  Print[Style["# Error: iM constraints", 12, Red]]];

If[(Abs[VLmtz2n] ≤ Vcotz2r), ModeViolation = 1;
      Print[Style["# Error: VLmtz2n  constraints", 12, Red]]];

If[(Abs[VLmtz2] ≥  (Vcotz2r + 0.005)), ModeViolation = 1;
      Print[Style["# Error: VLmtz2p  constraints", 12, Red]];];

If[((Abs[VLmtz1] ≤ Abs[Vcotz1r]) && (Imo < 0) && ModeViolation == 0),
      Print[Style[">>>> PO TRUE <<<", 12, Bold, Blue]];
      OperatingModeFound = "PO", Print["# MODE NOT DEFINED."];];
```

```
>>>> PO TRUE <<<
```

1.3.5. Evaluate converter voltage and current levels

In[68]:=

```
If[OperatingModeFound == "PO",

  Print[Style["Evaluating converter voltage and current levels..", 12, Bold, Blue]];
  IMO0 = Imo;
  IRO0 = Imo;
  VCSO0 = Vcso;
  TZ10 = tz1 ;
  TS0 = Ts;
  VoReal = 1/t1
    (NIntegrate[XS1Ptv[[4, 1]], {t, 0, tz1}] + NIntegrate[XS2POtv[[4, 1]], {t, tz1, tz2}]);
  Io = (VoReal - Vth)/rd;
  Po = VoReal Io;
  iS1off = -Iro;
  iS1rms = √((1/t2 (NIntegrate[XS1Ptv[[1, 1]]^2, {t, 0, tz1}] +
```

```
        NIntegrate[XS2POtv[[1, 1]]^2, {t, tz1, tz2}])];

iRrms = Sqrt[(2 (1/t2 (NIntegrate[XS1Ptv[[1, 1]]^2, {t, 0, tz1}] +
          NIntegrate[XS2POtv[[1, 1]]^2, {t, tz1, tz2}]))];

XS1Ptv2 = {-XS1Pt[[1]], Vin - XS1Pt[[2]], -XS1Pt[[3]], XS1Pt[[4]]} /. t → t - t1;
XS2POtv2 = {-XS2POt[[1]], Vin - XS2POt[[2]], -XS2POt[[3]], XS2POt[[4]]} /. t → t - t1;

vCsrms = Sqrt[(1/t2 (NIntegrate[XS1Ptv[[2, 1]]^2, {t, 0, tz1}] + NIntegrate[XS2POtv[[2, 1]]^2,
        {t, tz1, t1}] + NIntegrate[XS1Ptv2[[2, 1]]^2, {t, t1, t1 + tz1}] +
       NIntegrate[XS2POtv2[[2, 1]]^2, {t, t1 + tz1, t2}]))];
iRt  = Which[0 ≤ t ≤ tz1, XS1Ptv[[1, 1]], tz1 < t ≤ tz2, XS2POtv[[1, 1]]];
iMt = Which[0 ≤ t ≤ tz1, XS1Ptv[[3, 1]], tz1 < t ≤ tz2, XS2POtv[[3, 1]]];
vCot = Which[0 ≤ t ≤ tz1, XS1Ptv[[4, 1]], tz1 < t ≤ tz2, XS2POtv[[4, 1]]];
iSec  = (iRt - iMt) n;
iSecrms = Sqrt[(1/t2 (NIntegrate[iSec^2, {t, 0, t1}]))] ;

iCo = Abs[iSec] - (vCot - Vth)/rd;
iCorms = Sqrt[1/t1 NIntegrate[iCo^2, {t, 0, t1}]] ;
iRpk = NMaximize[{iRt, 0 ≤ t ≤ t1}, t][[1]];
iD1avg = 1/t2 NIntegrate[Abs[iSec], {t, 0, t1}];

Print["Vo = ", VoReal];
Print["Io = ", Io];
Print["fsw = ", 1/Ts];
Print["Po = ", Po];
Print["iS1off = ", iS1off];
Print["iS1rms = ", iS1rms];
Print["iRrms = ", iRrms];
Print["iRpk = ", iRpk];
Print["vCsrms = ", vCsrms];
Print["iSecrms = ", iSecrms];
Print["iCorms = ", iCorms];
Print["iD1avg = ", iD1avg];
Print["Vcso = ", Vcso];
Print["Iro = ", Iro];
Print["Imo = ", Imo];];
```

Evaluating converter voltage and current levels..

```
Vo = 87.2955

Io = 1.15844

fsw = 78927

Po = 101.127

iS1off = 0.44167

iS1rms = 0.43938

iRrms = 0.621377

iRpk = 0.940739

vCsrms = 234.814

iSecrms = 1.02175

iCorms = 0.863574

iD1avg = 0.579221

Vcso = 39.8393

Iro = -0.44167

Imo = -0.44167
```

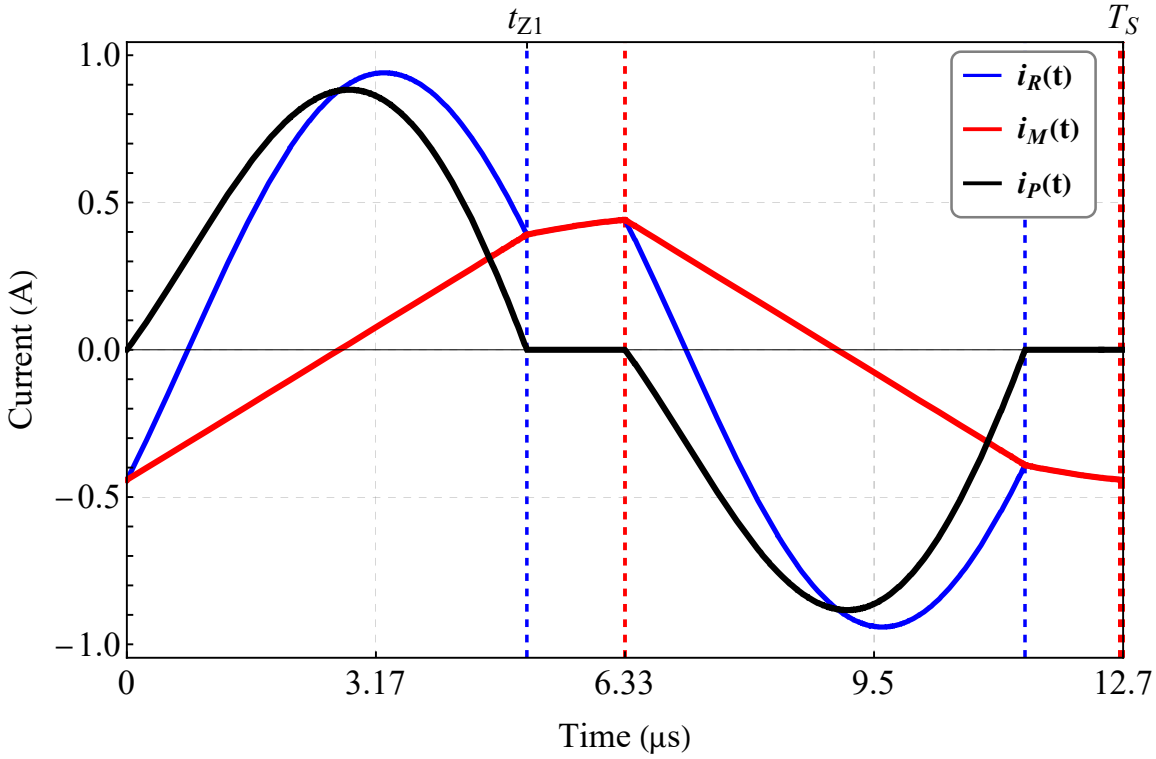
■ 1.3.6. Time-domain main waveforms plot

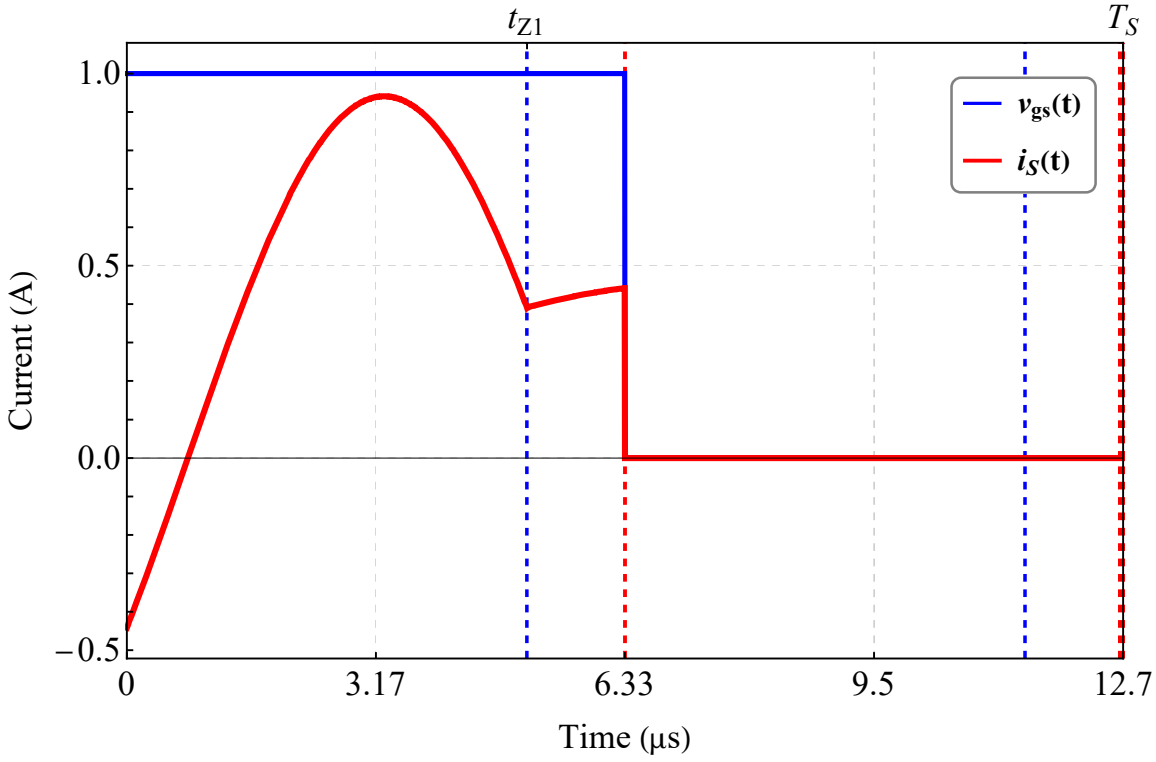
In[69]:=

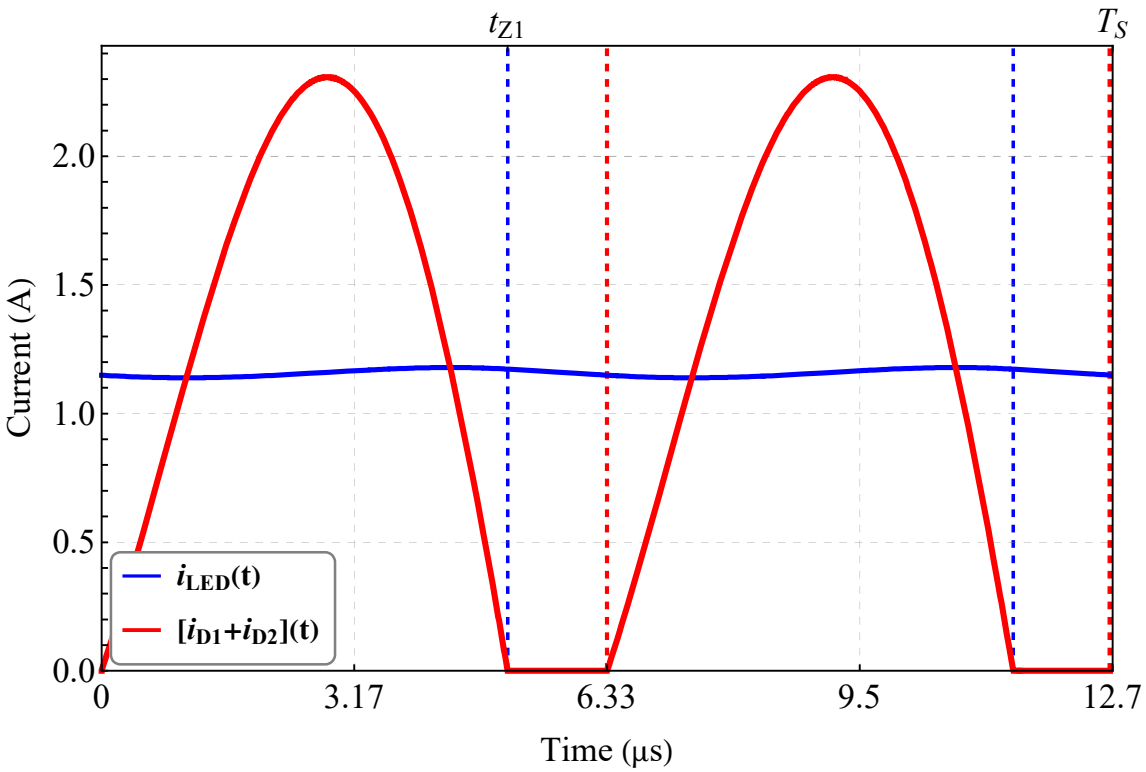
```
(* >>>>>>>>> Adjust states for a complete switching period plot << *)
XS1Ptv2 = {-XS1Pt[[1]], Vin - XS1Pt[[2]], -XS1Pt[[3]], XS1Pt[[4]]} /. t → t - t1;
XS2POtv2 = {-XS2POt[[1]], Vin - XS2POt[[2]], -XS2POt[[3]], XS2POt[[4]]} /. t → t - t1;

(*>>>> defining elements current and voltages in time-domain<<<<*)
iRt  = Which[0 ≤ t ≤ tz1, XS1Ptv[[1, 1]], tz1 < t ≤ tz2, XS2POtv[[1, 1]],
   t1 < t ≤ t1 + tz1, XS1Ptv2[[1, 1]], t1 + tz1 < t ≤ t2, XS2POtv2[[1, 1]]];
vCst = Which[0 ≤ t ≤ tz1, XS1Ptv[[2, 1]], tz1 < t ≤ tz2, XS2POtv[[2, 1]],
   t1 < t ≤ t1 + tz1, XS1Ptv2[[2, 1]], t1 + tz1 < t ≤ t2, XS2POtv2[[2, 1]]];
iMt  = Which[0 ≤ t ≤ tz1, XS1Ptv[[3, 1]], tz1 < t ≤ tz2, XS2POtv[[3, 1]],
   t1 < t ≤ t1 + tz1, XS1Ptv2[[3, 1]], t1 + tz1 < t ≤ t2, XS2POtv2[[3, 1]]];
vCot = Which[0 ≤ t ≤ tz1, XS1Ptv[[4, 1]], tz1 < t ≤ tz2, XS2POtv[[4, 1]],
   t1 < t ≤ t1 + tz1, XS1Ptv2[[4, 1]], t1 + tz1 < t ≤ t2, XS2POtv2[[4, 1]]];
iS1t = Which[0 ≤ t ≤ tz1, XS1Ptv[[1, 1]], tz1 < t ≤ tz2, XS2POtv[[1, 1]],
   t1 < t ≤ t1 + tz1, 0, t1 + tz1 < t ≤ t2, 0];
vgs1t = Which[0 ≤ t ≤ t1, 1, t1 < t ≤ t2, 0];

(*>>>> PLOT CONFIGURATION <<<*)
PlotStyle1 = Sequence @@ {
    FrameTicks → {{Automatic, None}, {
       {{0, NumberForm[0, 1]}, {t2/4, NumberForm[N[t2/4]/(1×10^-6), 3]},
        {t1, NumberForm[t1/(1×10^-6), 3]}, {t1 + t2/4, NumberForm[N[t1 + t2/4]/(1×10^-6), 3]},
        {t2, NumberForm[N[t2]/(1×10^-6), 3]}}, {{tz1, "t_z1"}, {t2, "T_s"}}}},
    (*Filling→ {1→{2}},*)
    Frame → True,
```

```
    ImageSize → {600, 400},
    FrameLabel → {{"Current (A)", None}, {"Time (μs)", None}},
    PlotRange → {{0, t2}, {Automatic, Automatic}},
    LabelStyle → {FontFamily → "Times New Roman", 18, Black},

    PlotStyle → {{Blue, Thickness[0.005]},
      {Red, Thickness[0.006]},
      {Black, Thickness[0.006]}},

    Exclusions → None,
    (*WorkingPrecision→3,*)
    TicksStyle → {Black, Black},

    GridLines → {{
       {t2/4, Directive[Gray, Dashed]},
       {t1 + t2/4, Directive[Gray, Dashed]},
       {tz1, Directive[Blue, Thickness[0.0035]]},
       {t1, Directive[Red, Thickness[0.004]]},
       {t1 + tz1, Directive[Blue, Thickness[0.0035]]},
       {t2, Directive[Red, Thickness[0.01]]}},
      Automatic},
    GridLinesStyle → Directive[Gray, Dashed],
    FrameStyle → Directive[Thickness[0.002]]};

(*>>>> START PLOT <<<<*)
Print[
  Plot[{iRt, iMt, (iRt - iMt)}, {t, 0, t2},
   PlotLegends → Placed[LineLegend[{"iR(t)", "iM(t)", "iP(t)"},
      LabelStyle → {FontFamily → "Times New Roman", Black, Bold, 16},
      LegendLayout → {"Column", 1},
      LegendFunction → ((Framed[#, FrameMargins → 0, Background → White, RoundingRadius → 5,
           FrameStyle → Gray] &))], {0.9, 0.85}], Evaluate@PlotStyle1]];

Print[
  Plot[{vgs1t, iS1t}, {t, 0, t2},
   PlotLegends → Placed[LineLegend[{"vgs(t)", "iS(t)", "iP(t)"},
      LabelStyle → {FontFamily → "Times New Roman", Black, Bold, 16},
      LegendLayout → {"Column", 1},
      LegendFunction → ((Framed[#, FrameMargins → 0, Background → White, RoundingRadius → 5,
           FrameStyle → Gray] &))], {0.9, 0.85}], Evaluate@PlotStyle1]];



Print[
  Plot[{(vCot - Vth)/rd, Abs[(iRt - iMt)] n}, {t, 0, t2},
   PlotLegends → Placed[LineLegend[{"iLED(t)", "[iD1+iD2](t)"},
      LabelStyle → {FontFamily → "Times New Roman", Black, Bold, 16},
```

```
    LegendLayout → {"Column", 1}, LegendFunction → ((Framed[#, FrameMargins → 0,
          Background → White, RoundingRadius → 5, FrameStyle → Gray] &))], {0.12, 0.1}],
PlotRange → {{0, t2}, {0, Automatic}}, Evaluate@PlotStyle1]];
```






t_{Z1}
T_S
2.0
1.5
1.0
0.5
0.0
Current (A)
$i_{LED}(t)$
$[i_{D1}+i_{D2}](t)$
0
3.17
6.33
9.5
12.7
Time (μs)

APPENDIX C - LLC DISCRETE COMPONENTS DESIGN

This appendix presents the procedure employed to design the inductor and transformer of the LLC resonant converter. Besides, the power semiconductors and capacitors selection is discussed. The magnetic components design involves the core material, shape, size selection, and winding wire selection. To defined the core size, the area product method is employed. To select the power semiconductor and capacitors, the electrical stress in these components is evaluated.

C.1 DISCRETE COMPONENTS DESIGN VARIABLES

Table 17 presents the definition of the parameters employed during the design of the discrete components. To implement the magnetic elements, the ferrites cores from Thornton manufacturer are employed (THORNTON, 2015). Regarding the magnetic core, the EE shape is employed in this work. Table 18 presents the parameters for several EE cores. Finally, Table 19 specify the round copper wires

Table 17 – Discrete components variables

Discrete components design parameters	
$J_m = 400\ A/cm^2$	Peak value of the current density
$B_{sat} = 0.35\ T$	IP12 material magnetic flux saturation
B_m	Maximum magnetic flux density
$k_{ms} = 0.61$	Manual multi-strand wire factor (EBERT, 1997)
$I_{R.RMS}$	Resonant tank maximum RMS current
$I_{R.RMS}$	Resonant tank maximum peak current
$I_{SEC.RMS}$	Secondary side maximum RMS current
k_w	Inductor winding fill factor
k_p	Transformer winding fill factor
MLT	Mean turn length
N	Number of turns
A_e	Core cross-sectional area
A_w	Core window area
ST	Cross-sectional area of the copper wire
ST_i	Cross-sectional area of the isolated copper wire
$\rho(\Omega/cm)$	Wire effective resistivity

Source: Author.

Table 18 – EE core data

Core	$A_eA_w\ (cm^4)$	$A_e\ (cm^2)$	$A_w\ (cm^2)$	$MLT\ (cm)$	$V_e\ (cm^3)$
EE.20/10/5	0.08	0.31	0.26	4.28	1.34
EE.25/10/6	0.17	0.39	0.62	4.90	1.91
EE.30/15/7	0.48	0.60	0.80	6.70	4.00
EE.30/15/14	1.02	1.20	0.85	6.90	8.00
EE.40/17/12	1.50	1.48	1.02	7.70	11.39
EE.42/15	2.84	1.81	1.57	9.70	17.10
EE.42/20	3.77	2.40	1.57	10.50	23.30
EE55	8.85	3.54	2.50	11.60	42.50

Source: Adapted from (THORNTON, 2015)

Table 19 – AWG round copper wire parameters

AWG	$ST(cm^2)$	$ST_i(cm^2)$	$\rho(\Omega/\text{cm})$ @100°C
AWG.13	0.026243	0.029793	0.000088
AWG.14	0.020811	0.023800	0.000111
AWG.15	0.016504	0.019021	0.000140
AWG.16	0.013088	0.105207	0.000176
AWG.17	0.010379	0.012164	0.000222
AWG.18	0.008231	0.009735	0.000280
AWG.19	0.006527	0.007794	0.000353
AWG.20	0.005176	0.006244	0.000445
AWG.21	0.004105	0.005004	0.000561
AWG.22	0.003255	0.004013	0.000708
AWG.23	0.002582	0.003221	0.000892
AWG.24	0.002047	0.002586	0.001125
AWG.25	0.001624	0.002078	0.001419
AWG.26	0.001287	0.001671	0.001789
AWG.27	0.001021	0.001344	0.002256
AWG.28	0.000810	0.001083	0.002845
AWG.29	0.000642	0.000872	0.003587
AWG.30	0.000509	0.000704	0.004523
AWG.31	0.000404	0.000568	0.005704
AWG.32	0.000320	0.000459	0.007192
AWG.33	0.000254	0.000371	0.009070
AWG.34	0.000201	0.000300	0.011437
AWG.35	0.000160	0.000243	0.014422
AWG.36	0.000127	0.000197	0.018186
AWG.37	0.000100	0.000160	0.022932

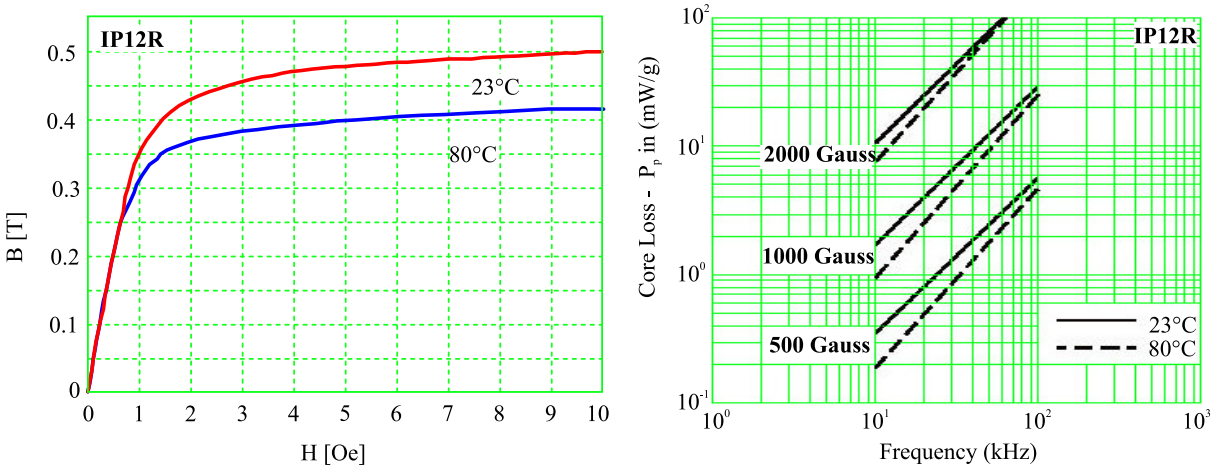
employed.

C.2 Magnetic core materials

As above-mentioned, to implement the magnetic elements of the LLC resonant converter, the ferrites cores from Thornton manufacturer are employed (Thornton, 2015). From the available materials, the IP12R is selected. Fig. 115 shows the BxH curve for the IP12R cores, and the total core loss in W/kg.

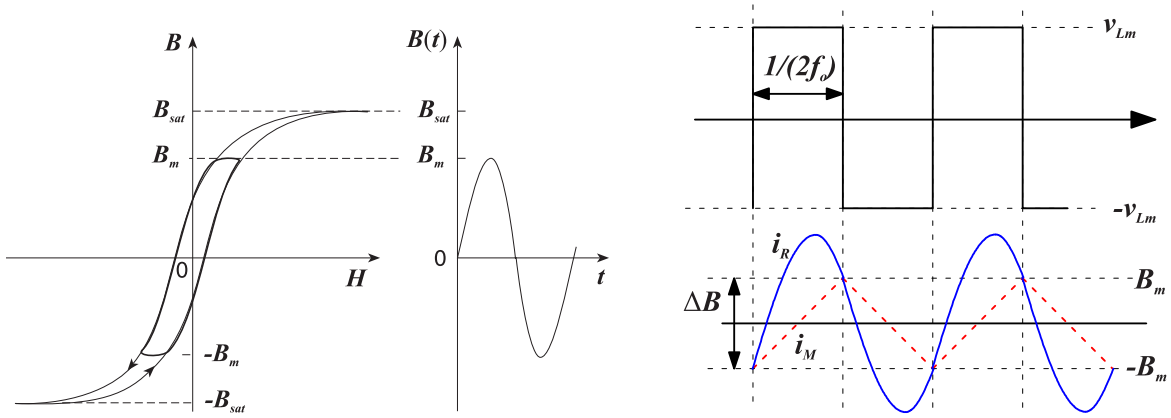
For the sake of clarity, Fig. 116(a) shows the magnetic core hysteresis and the waveforms of the magnetic flux density for AC inductor. As can be seen, to avoid the magnetic core saturation, the peak value (B_m) for the magnetic flux density must be smaller than the saturation flux density (B_{sat}). Regarding the LLC transformer, Fig. 116(b) illustrates that the peak value of the magnetic flux density in the transformer is achieved at the peak of the magnetizing current.

Figure 115 – Manufacturer's published data: Left-trace: IP12 material BxH curve; Right-trace: IP12 material total core loss.



Source: Adapted from (THORNTON, 2015)

Figure 116 – Left-trace: Magnetic core hysteresis and the waveform of the magnetic flux density $B(t)$ for AC inductors; Right-trace: LLC converter waveforms of the transformer magnetizing inductance voltage, primary side current, and magnetizing current.



Source: Adapted from: Left-trace:(KAZIMIERCZUK, 2013). Right-trace: AND90061-D

C.3 SERIES RESONANT INDUCTOR DESIGN

The minimal cross-sectional area of the copper wire is given by (C.1). Then, employing Table 19 the AWG wire is selected.

$$ST_{Ls} = \frac{I_{R.RMS}}{J_m}(cm^2) \tag{C.1}$$

To define the inductor core size, initially, the inductor minimum area product is computed by (C.2). In the sequence, assessing the data in Table 18, the core size that presents a product area equal or greater than (C.2) is chosen.

$$A_e A_w = \frac{L_S I_{R.RMS} I_{R.PK}}{B_m J_m k_w}(cm^4) \tag{C.2}$$

where $B_m = 0.35\ T$, and $k_w = 0.7$.

Now, considering the cross-sectional area A_e of the selected core size, the inductor number of turns is defined by

$$N = \frac{L_S I_{R.PK}}{A_e B_m}. \tag{C.3}$$

The DC and low frequency winding resistance is then defined by

$$R_{DC.Ls} = \rho MLTN(\Omega). \tag{C.4}$$

Given the selected wire and required number of turns, the minimal core window area necessary to accommodate the inductor winding is defined by

$$A_{w.min} = \frac{N\ ST_{Ls}}{k_w k_{ms}}(cm^2). \tag{C.5}$$

The inductor design is finished if $A_{w_{Ls}} \geq A_{w.min}$, otherwise a larger core must be employed.

It is worth mentioning that the skin effect is considered to define the number of parallel wires. Multi-strand wires are constructed manually. Thus, to consider the increase of the cross-sectional wire area, the manual multi-strand wire factor k_{ms} is used in the design procedure described.

C.4 TRANSFORMER DESIGN

The transformer primary winding is subjected to the same current of the series resonant inductor. Thus the minimal cross-sectional area of the copper wire is

$$ST_{Np} = ST_{Ls}. \tag{C.6}$$

On the other hand, the cross-sectional area of the copper wire for the secondary windings is defined by

$$ST_{Ns} = \frac{I_{SEC.RMS}}{J_m}(cm^2). \tag{C.7}$$

The LLC transformer minimal area product is calculated by

$$A_e A_w = \frac{I_{R.RMS} n V_{O.MAX}}{2 J_m k_w k_p B_m f_{sw.min}}(cm^4). \tag{C.8}$$

Where $k_w = 0.5$, $k_p = 0.5$, and $B_m = 0.175\ T$.

With the computed product area A_eA_w, the transformer core size is chosen from the EE core data table. For the selected magnetic core, the values of A_e and A_w are obtained from the EE core data table.

The minimal number of turns for the transformer primary winding is defined by

$$N_{p.min} = \frac{nV_{O.NOM}}{2A_eB_mf_{sw.min}}. \tag{C.9}$$

Therefore, the primary winding must satisfy $N_p \geq N_{p.min}$. Now, considering the transformer turns ratio n, the number of turns for each secondary winding is given by

$$N_s = \frac{N_p}{n}. \tag{C.10}$$

The DC and low frequency winding resistance is then defined by

$$R_{DC.Np} = \rho_{N_p}\ MLT\ N_p \tag{C.11a}$$
$$R_{DC.Ns} = \rho_{N_s}\ MLT\ N_s. \tag{C.11b}$$

Finally, the minimal core window area necessary to accommodate the transformer windings is defined by

$$A_{w.min} = \frac{N_p\ ST_{Np} + 2\ N_s\ ST_{Ns}}{k_wk_{ms}}(cm^2). \tag{C.12}$$

The transformer design is finished if $A_w \geq A_{w.min}$, otherwise a larger core size must be employed.

Analyzing (C.9) it can be seen that for a given applied voltage we can reduce the N_p turns by increasing B_m. Reducing N_p has an effect of decreasing the cooper loss. However, increasing B_m outcomes in higher core losses (P_{Fe}), since $P_{Fe} \propto B_m^{\beta}$. As a result there is an optimal choice for B_m. On the other hand, analyzing (C.8) it can be seen that we can reduce the core size by increasing B_m. Magnetic core with reduced size present accordingly a smaller volume, so consequently the core loss is reduced, since $P_{Fe} \propto V_e$. Besides, analyzing (C.8) and (C.9) the f_{sw} dependence is also noticed. Increasing f_{sw} results in smaller cooper losses, since N_p is reduced. With the increase of f_{sw} smaller core size are required, which reduces $P_{Fe} \propto V_e$. However, increasing f_{sw} has an effect of increasing P_{Fe}, since $P_{Fe} \propto f_{sw}^{\alpha}$.

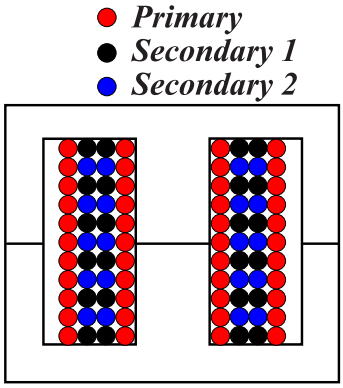
In conclusion, it is easy to see that the transformer optimization includes several analyses, especially when the power density and efficiency are taken into account. The proposal of an optimized design for the magnetic components is not the focus of this thesis.

C.4.1 Transformer construction

The primary and secondary windings are sandwiched to improve the coupling between windings and reduce the proximity effect. In addition, the bifilar winding method is employed to reduce the converter conduction losses caused by the imbalance on the currents in the secondary side of the transformer (JUNG, 2013). Actually, the bifilar method reduces the imbalance in secondary leakage inductance imbalance.

Fig. 117 illustrates the transformer construction where the sandwiched winding and the bifilar method is employed.

Figure 117 – LLC transformer assembly illustration, where the sandwiched winding and bifilar method is employed.



Source: Author.

C.5 Power semiconductor devices selection

For the LLC resonant LED driver, the employed power semiconductors are the MOSFETs switches used in the half-bridge and the rectifier diodes applied in the full-wave output rectifier.

The selected MOSFET must withstand the maximum current and voltage stress. Besides, MOSFETs with low drain-source on-state resistance ($R_{DS(on)}$) and small output capacitance (C_{oss}) are preferable. The input voltage defines the maximum voltage for the half-bridge switches. The switch peak and RMS current are a function of the employed resonant tank. To compute the half-bridge current levels, the time-domain analysis should be used since high accuracy is achieved. The rectifier diode will be subjected to voltage stress given by $2V_o$. The average current is given by $I_o/2$. Since the output voltage is low and the current is considerable, it is suitable to select Schottky diodes to reduce the conduction losses.

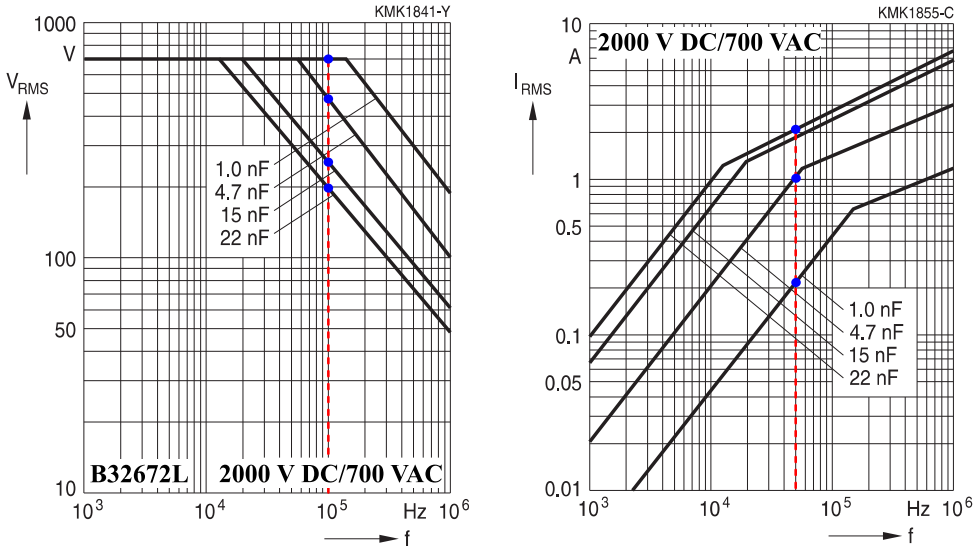
C.6 Series resonant capacitor component selection

In the LLC resonant converter, the series resonant capacitor C_S is subjected to the tank current i_R and high RMS voltage stress $v_{Cs.rms}$. Therefore, the selected device must withstand these high voltage and current levels. In this work, the B32672L series from the EPCOS Metallized Polypropylene Film Capacitors was selected for the series resonant capacitor. The B32672L series presents several capacitance values, whose electrical specifications are: 250 VDC/160 VAC; 450 VDC/200 VAC; 630 VDC/250 VAC; 1000 VDC/250 VAC; 1300 VDC/500 VAC; 1600 VDC/600 VAC; 2000 VDC/700 VAC; 2000 VDC/900 VAC.

Being the capacitance values defined, the next step is to pick up the correct capacitor from the selected series. In this way, it is necessary to evaluate the maximum permissible AC voltage of each capacitor. The maximum permissible AC voltage of the capacitor must be higher than the $v_{Cs.rms}$ imposed by the LLC filter. Similarly, the allowable RMS current of the capacitor must be higher than the maximum resonant tank current. Fig. 76 shows the maximum permissible AC voltage and current derating versus frequency for the B32672L series specified by 2000 VDC/700 VAC.

As can be seen in Fig. 76, for the operation at 100 kHz, as higher the capacitance value, the lower will be the maximum permissible AC voltage. For the maximum permitted current, as higher the capacitor, the higher will be the maximum permissible AC current.

Figure 118 – Metallized Polypropylene Film Capacitors maximum permissible AC voltage and current derating versus frequency for the B32672L series - 2000 VDC/700 VAC.



Source: Adapted from (EPCOS, 2018).

APPENDIX D - LLC POWER LOSS MODEL

This appendix shows the method employed in Chapter 5 to estimate the LLC resonant converter power losses. The converter power loss is given by the sum of each discrete element power loss determined by a power loss model (Z. FANG, CAI ET AL., 2015; MUMTAHINA ET AL., 2018; SUEL ET AL., 2019; H. WANG E BLAABJERG, 2014; C.-H. YANG ET AL., 2013; R. YU ET AL., 2012). The power loss determination employs the current and voltages levels defined with the proposed time-domain procedure. Besides, parameters from the datasheet of the component are also utilized.

D.1 HALF-BRIDGE SWITCHES POWER LOSS

Employing MOSFETs as the HB switches, the HB power loss can be divided into conduction, switching, and body diode losses (GRAOVAC ET AL., 2006). Conduction losses are mainly defined by the RMS current flowing through the MOSFETs, which is modeled by a single resistor with a drain-source on-state resistance ($R_{DS(on)}$). Numerically, the HB conduction loss ($PL_{HB.cond}$) is estimated by (D.1). Where the $R_{DS(on)}$ can be obtained from the MOSFET's datasheet; and, $i_{S1.RMS}$ is obtained from the time-domain analysis.

$$PL_{HB.cond} = 2\left(i_{S1.RMS}{}^2 R_{DS(on)}\right) \tag{D.1}$$

Switching losses are divided into turn-off and turn-on losses. However, if the converter operates outside of the capacitive region, the HB switches are turned on with ZVS, and turn-on losses are negligible. Consequently, the HB switching losses ($PL_{HB.sw}$) are mainly given by the turn-off losses. The turn-off power loss depends on switching frequency (f_{sw}) and voltage and current levels at the beginning of the turning-off process. Besides, the switching times also impacts those losses. The $PL_{HB.sw}$ is estimated by (D.2). Wherein V_{IN} is the bus voltage; $i_{S1.off} = i_{S2.off}$ is the turn-off current obtained from the time-domain analysis; and, t_r and t_f are respectively the rising time of the drain-source voltage and falling time of the current, obtained from the MOSFET datasheet.

$$PL_{HB.sw} = 2\left(\frac{V_{IN} i_{S1.off}(t_r + t_f) f_{sw}}{2}\right) \tag{D.2}$$

The body diode losses occur due to the conduction losses of the body diode during dead-time. However, as usually done in the LLC power losses assessment, the body diode losses are neglected. Finally, the total power loss in the HB (PL_{HB}) can be obtained by summing $PL_{HB.cond}$ and $PL_{HB.sw}$.

D.2 RECTIFIER LOSSES

A well-known LLC feature is its capability to perform natural commutation on the output rectifier when the converter operates at the discontinuous modes (PO and OPO). Thus, the rectifier switching losses are at low levels, allowing one to omit them without compromising the estimated converter losses. Consequently, the principal power loss in the rectifier is given by the conduction losses. These conduction losses occur due to the diode threshold voltage V_F and dynamic series resistor r_{diode}, where both parameters are extracted from the diode datasheet. Numerically, the rectifier conduction power loss is then estimated by

$$PL_{Rec.cond} = 2(i_{D1.AVG} V_F + i_{D1.RMS} r_{diode}) \tag{D.3}$$

where $i_{D1.AVG}$, and $i_{D1.RMS}$ are the diode average and RMS current, respectively. These current levels are computed employing the proposed time-domain analysis.

D.3 Resonant capacitor power loss

The losses associated with the series resonant capacitor are given by (D.4). As can be seen, the losses are determined by the resonant tank current $i_{R.RMS}$ and capacitor dissipation factor $tan(\delta)$ (DF). Thus, metallized polypropylene Film capacitors are usually employed to achieve high efficiency due to their low DF. The DF is obtained from the capacitor datasheet.

$$PL_{Cs} = ESR_{Cs}(i_{R.RMS})^2 \tag{D.4}$$

$$ESR_{Cs} = \frac{DF_{Cs}}{2\pi f_{sw} C_s} \tag{D.5}$$

D.4 Output Capacitor Losses

The output capacitor filters the AC component from the rectified output current. Due to the rectified current high ripple, the output capacitor is subjected to high RMS current levels ($i_{Co.RMS}$). Thus, capacitors with low equivalent series resistance ESR should be employed. The output capacitor losses is estimated by

$$PL_{CO} = ESR_{Co}(i_{Co.RMS})^2 \tag{D.6}$$

where the ESR is the equivalent series resistance of C_O, defined by

$$ESR_{Co} = \frac{DF_{Co}}{2\pi f_{sw} C_O}. \tag{D.7}$$

D.5 Series Resonant Inductor Power Losses

The power loss in the series resonant inductor is categorized as core loss and copper loss. The Copper loss occurs in the inductor winding, where the resonant tank current flows. For the inductor power loss, the resonant tank current is assumed to be a sinusoidal wave, and thus the influence of harmonic losses can be ignored. The core power loss is given by Hysteresis loss and Eddy current loss.

The inductor copper loss can be estimated using the AC resistance (r_{ac}) of winding, defined by

$$r_{ac.Ls} = k_s r_{dc} \tag{D.8}$$

where k_s is the ratio of the AC to DC resistance r_{dc}, which is a function of the inductor quality construction. For the sake of simplification, in this work, we assumed that $k_s = 1$.

The inductor DC resistance can be defined by

$$r_{dc.Ls} = \frac{\rho_{Cu} MLT n^2}{k_w A_w} \tag{D.9}$$

where k_w is the inductor winding fill factor, A_w is the core window area, MLT is the mean length of turn, and ρ_{Cu} is the copper resistivity ($1.72 \cdot 10^{-4}\ \Omega cm^2/m$).

Finally, the inductor copper loss is estimated by

$$PL_{Ls.Cu} = {i_{R.RMS}}^2 r_{ac.Ls} \tag{D.10}$$

The empirical Steinmetz equation (SE) is applied to calculate the total core loss of the inductor. Thus,

assuming a sinusoidal excitation, the inductor core total losses are estimated by

$$PL_{Ls.Fe} = V_{Ls} C_m f_{sw}^{\alpha} \Delta B_{Ls}{}^{\beta} \tag{D.11}$$

Where C_m, α and β are the Steinmetz coefficients derived from the manufacturer datasheet. V_{Ls} is the core volume, and ΔB_{Ls} is the peak of the magnetic flux density.

For the series resonant inductor L_S, the peak flux density is estimated by (D.12).

$$\Delta B_{Ls} = \frac{L_S i_{R.pk}}{N_{Ls} A e_{Ls}} \tag{D.12}$$

D.6 Transformer Losses

Similarly to the inductor power loss, the transformer losses are divided into copper loss and core loss. However, since the LLC transformer is excited with square waveform, SE is not appropriate for its core loss calculation (Suel et al., 2019). Therefore, waveform coefficient FWC is defined first, and then the SE is utilized.

For the square waveform, the FWC is given by

$$FWC_{sq} = \frac{\pi}{4}. \tag{D.13}$$

The transformer core loss is now computed by

$$PL_{Trx.Fe} = FWC_{sq} V_{Trx} C_m f_{sw}^{\alpha} \Delta B_{Trx}{}^{\beta}. \tag{D.14}$$

Where the transformer peak flux density is defined by

$$\Delta B_{Trx} = \frac{n V_o}{4 f_{sw} N_p A e_{Trx}}. \tag{D.15}$$

The transformer copper loss that occurs in the primary ($PL_{Trx.np.cnd}$) and secondary ($PL_{Trx.ns.cnd}$) winding, are estimated by

$$PL_{Trx.np.cnd} = i_{R.RMS}{}^2 r_{dc.np} \tag{D.16a}$$

$$PL_{Trx.ns.cnd} = i_{Sec.RMS}{}^2 r_{dc.ns} \tag{D.16b}$$

$$\tag{D.16c}$$

D.7 Optimization guidelines from power loss model

Further analyzing the power loss model, some guidelines can be derived toward the converter efficiency improvement.

- The HB conduction loss, series resonant capacitor loss, and inductor and transformer copper loss are linked to the resonant tank current. So, any effort in reducing this current outcome in efficiency gain.
- HB switching losses are a function of the switching times, input voltage, and turn-off current. Thus, the selections of MOSFET that can switch faster will reduce this loss. Besides, reducing the switch's turn-off current is also enjoyable.
- Core losses are determined by the peak flux density, switching frequency, core size, and magnetic material. So, the selection of material with reduced losses in high switching frequency is essential. Besides, any attempt to reduce the peak flux density also outcomes in efficiency

gain.

D.8 IP12 CORE LOSS ANALYSIS

In this section, the Steinmetz coefficients are derived from the manufacturer datasheet. For the IP12 material from Thornton manufacturer (THORNTON, 2015), Fig. 119 shows the manufacturer's published data of the total core loss density, in Watts per kg, as a function of sinusoidal excitation frequency and peak AC flux density.

The total core loss density, in Watts per kg, can be approximated by an empirical function (SE) of the form

$$Pp(f_s, B_m) = C_m f_s^{\alpha} B_m^{\beta} \tag{D.17}$$

The constant C_m, α, and β are determined by fitting (D.17) to the data presented in Fig. 119. Thus, following the procedure presented in (EBERT, 1997), four operating conditions have to be selected from manufacturer's published data. Initially, for the same frequency (f_1), the power loss under two different flux densities (B_1, B_2) is selected, yielding in $P_{P1}(f_1, B_1)$ and $P_{P2}(f_1, B_2)$. Following, for the same flux density condition (B_3), the power loss under two different frequencies (f_3, and f_4) are defined, yielding in $P_{P3}(f_3, B_3)$ and $P_{P4}(f_4, B_3)$. Then, β, α, and C_m are determined respectively by (D.18), (D.19), and (D.20).

$$\beta = \frac{\log(P_{P1}) - \log(P_{P2})}{\log(B_1) - \log(B_2)} \tag{D.18}$$

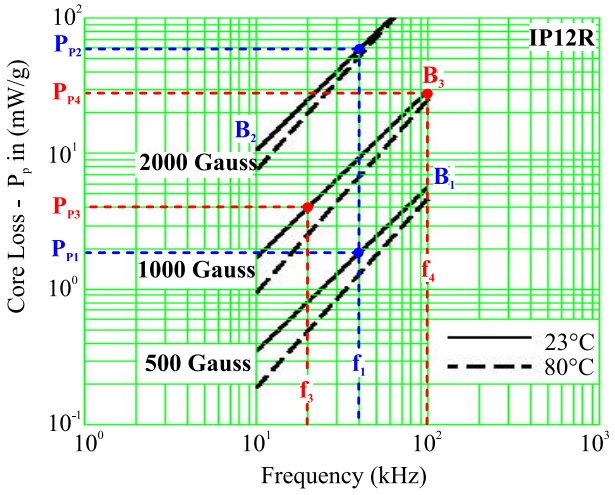
$$\alpha = \frac{\log(P_{P3}) - \log(P_{P4})}{\log(f_3) - \log(f_4)} \tag{D.19}$$

$$C_m = 10^{-\beta \log(B_3) - \alpha \log(f_3) + \log(P_{P3})} \tag{D.20}$$

Fig. 120(left) shows the fitted curves compared to the experimental points. The expression for the power loss computation is shown at the bottom of this figure. Given the IP12 material mass density of 4800 kg/m^3, the volumetric power loss can be computed, as shown in Fig. 120(right).

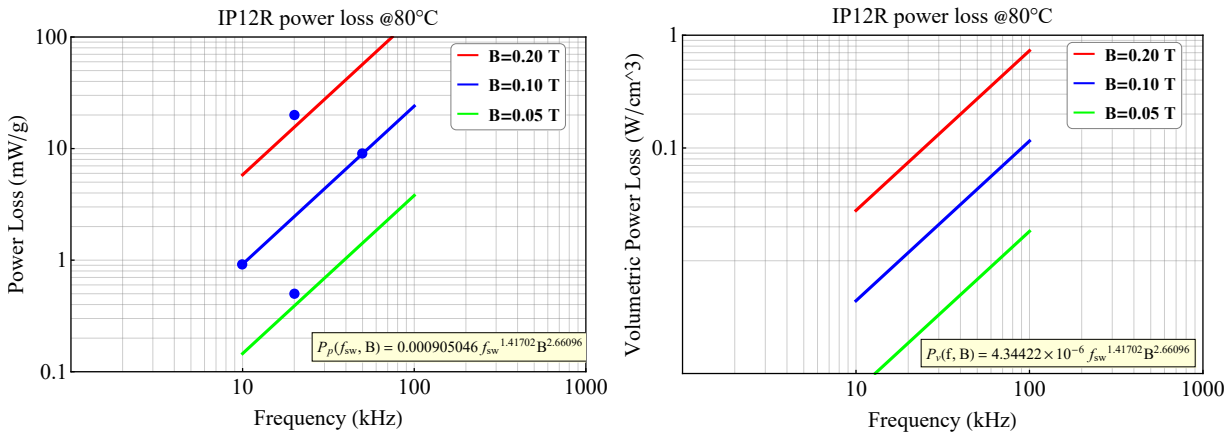
At this point, in order to optimize the design or even avoid the operation at the worst condition,

Figure 119 – IP12 material core loss: Manufacturer's published data.



Source: Adapted from (THORNTON, 2015)

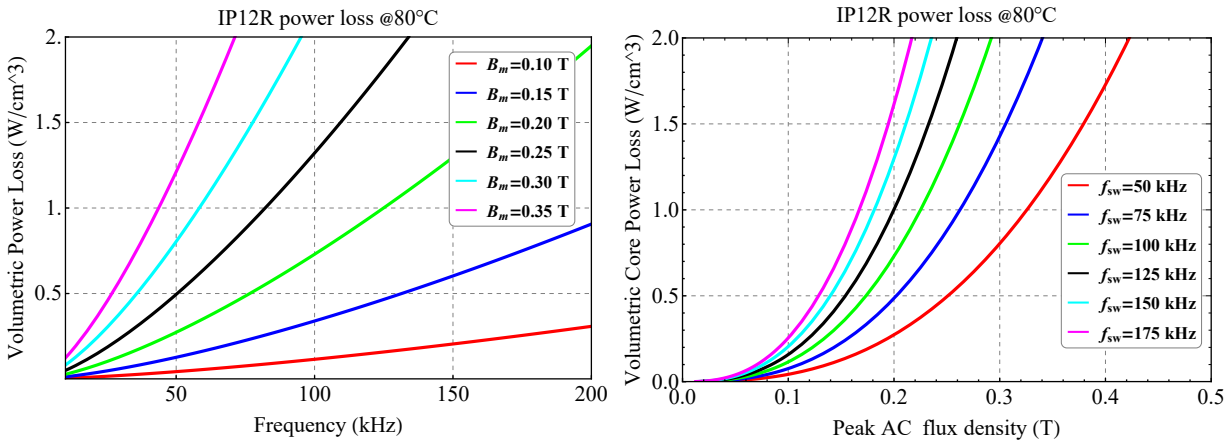
Figure 120 – Theoretical reproduction for Manufacturer's published data. Left-trace: Power loss density in W/kg as a function of the frequency for different peak flux densities; Right-trace: Volumetric power loss as a function of the frequency for different peak flux densities.



Source: Author.

the total volumetric core loss can be assessed for the main parameters' variation. Therefore, Fig. 121 shows the volumetric power loss for the frequency and peak flux density variation. As can be seen in Fig. 121(left-trace), for the same volumetric losses, as higher the frequency, the smaller should be the peak flux density. Analyzing the Fig. 121(right-trace), for the same peak flux density, it can be seen that the volumetric losses are higher as higher is the frequency. Nevertheless, it should be bear in mind that the selection of the switching frequency and peak flux density influences the magnetic core size and the winding number of turns, impacting the magnetic element copper losses. Therefore, extended analysis is developed in the next section.

Figure 121 – IP12R total core power loss analysis. Left-trace: Volumetric power loss as a function of the frequency for different peak flux densities. Right-trace: Volumetric power loss as a function of peak flux density for different frequencies.



Source: Author.

D.9 Extended analysis for the transformer loss

The transformer number of turns for the primary winding is given by

$$N_p = \frac{nV_o}{4A_eB_mf_{sw}} \tag{D.21}$$

The dc winding resistance can be computed by

$$R_{dc} = \frac{N_p\rho_{Cu}MLT}{ST_i} = \frac{N_p\rho_{Cu}MLT}{\frac{k_uA_w}{N}} = \frac{\rho_{Cu}MLT\left(\frac{nV_o}{4A_eB_mf_{sw}}\right)^2}{k_uA_w} \tag{D.22}$$

At this point, the dc resistance for the primary winding can be rewritten by

$$R_{dc.Np} = \frac{n^2V_o^2}{16f_{sw}^2}\frac{\rho_{Cu}MLT}{A_e^2A_wk_u}\frac{1}{B_m^2} \tag{D.23}$$

The dc resistance for the secondary winding is given by

$$R_{dc.sec} = \frac{nV_o^2}{16f_{sw}^2}\frac{\rho_{Cu}MLT}{A_e^2A_wk_u}\frac{1}{B_m^2} \tag{D.24}$$

Finally, the total copper losses in the transformer can be computed by

$$P_{Trx.Cu} = i_p^2R_{dc.Np} + 2i_{sec}^2R_{dc.sec} \tag{D.25}$$

Then, considering dc resistance definitions, the total copper loss is rewritten by

$$P_{Trx.Cu} = \frac{nV_o^2(ni_p^2 + 2i_{sec}^2)}{16f_{sw}^2}\frac{\rho_{Cu}MLT}{A_e^2A_wk_u}\frac{1}{B_m^2} \tag{D.26}$$

Fig. 122 shows the copper loss analysis for different magnetic core sizes and different frequencies. In this analysis, $n = 2.28$, $V_o = 87\ V$, $i_p = 0.6\ A$, $i_s = 1\ A$, $k_u = 0.45$. The remaining parameters are function of the employed core. As can be seen, as the peak flux density increase, the copper losses are reduced. However, to complete the magnetic component loss analysis, the core losses and the copper losses should be analyzed simultaneously.

The transformer core loss is given by

$$PL_{Trx.Fe} = V_{Trx}C_mf_{sw}^{\alpha}\Delta B_{Ls}{}^{\beta} \tag{D.27}$$

Consequently the total power loss of the transformer is computed by

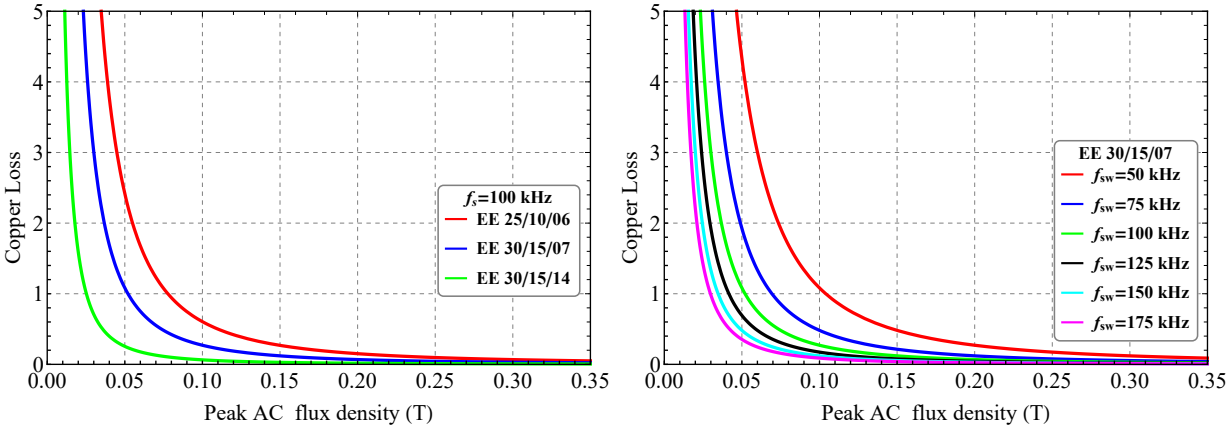
$$P_{Trx.tot} = PL_{Trx.Fe} + PL_{Trx.Cu} \tag{D.28}$$

Fig. 123 shows the LLC transformer total power loss for two different magnetic cores operating at 75 kHz. As can be seen, there is an optimal operating condition for the peak flux density. After some calculations, the equation that defines the optimal peak flux density is derived, given by

$$B_{m.Op.Trx} = 8^{-\frac{1}{\beta+2}}\left(\frac{A_e^3A_w\beta C_mk_uf_{sw}^{\alpha+2}}{i_p^2n^2\rho_{Cu}V_o^2 + 2i_s^2n\rho_{Cu}V_o^2}\right)^{-\frac{1}{\beta+2}} \tag{D.29}$$

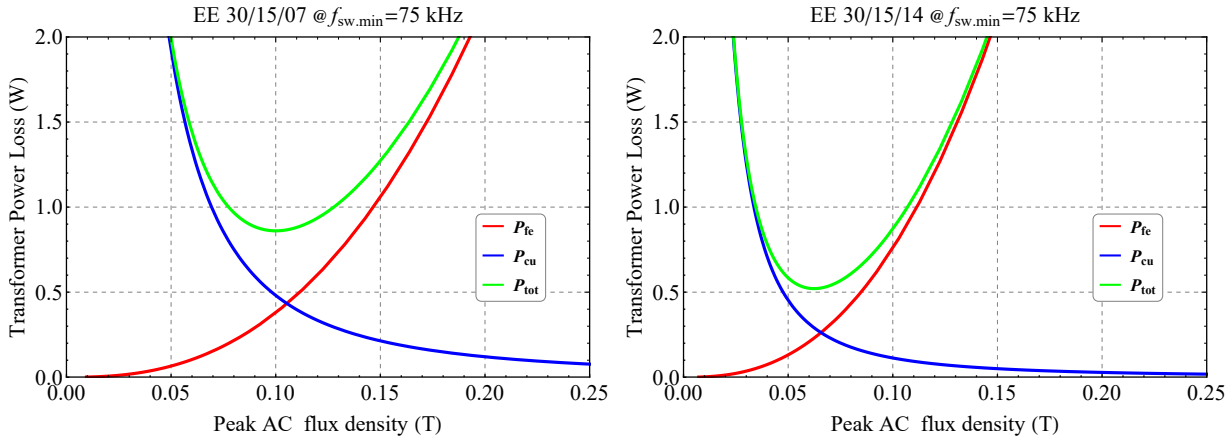
In order to further assess the LLC transformer total power loss, Fig. 124 shows the losses for different magnetic core sizes operating at $f_{sw} = 50\ kHz$ and $f_{sw} = 75\ kHz$. Similarly, Fig. 125 shows the losses

Figure 122 – LLC converter transformer copper loss analysis. Left: Copper loss as a function of the peak flux density for different magnetic core sizes. Rigt: Copper loss as a function of the peak flux density for the EE.30/15/07 core under different switching frequencies.



Source: Author

Figure 123 – LLC transformer total power loss. Left-trace: EE30/15/07 operating with $f_{sw} = 75\ kHz$; Right-trace: EE30/15/14 operating with $f_{sw} = 75\ kHz$.

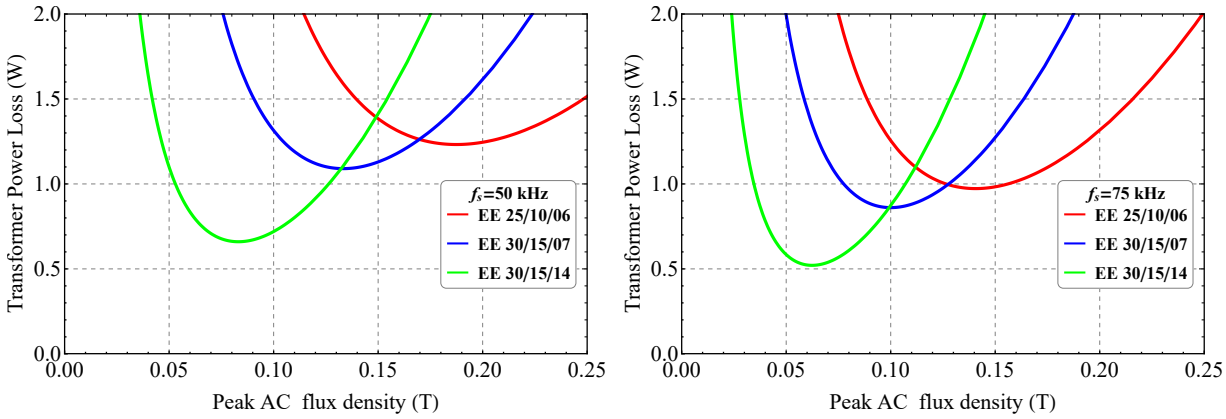


Source: Author.

for different switching frequencies and different magnetic core sizes. As it is clearly shown, there is an optimal peak flux density for each combination of core size and frequency.

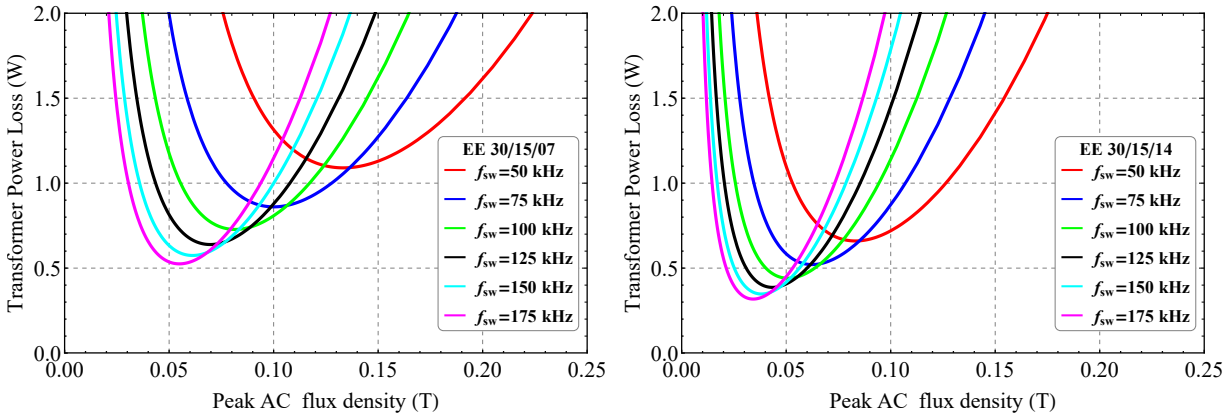
However, there is an issue related to the transformer's execution possibility when the optimal peak flux density is considered. For instance, for the same switching frequency, as higher the magnetic core size, the smaller the optimal peak flux density. For small peak flux density, the number of turns for each winding increases. Even though the core is larger for small optimal peak flux density, there are some cases where the core window area is not enough to accommodate the transformer's three windings. In this way, further analysis is required to outcome with an optimal design for the LLC transformer, which is out of this thesis's scope.

Figure 124 – LLC transformer total power loss as a function of the peak flux density for different magnetic core sizes operating at $f_{sw} = 50\ kHz$ and $f_{sw} = 75\ kHz$.



Source: Author.

Figure 125 – LLC transformer total power loss as a function of the peak flux density for different switching frequencies and different magnetic core sizes.



Source: Author

APPENDIX E - EXPERIMENTAL SETUP

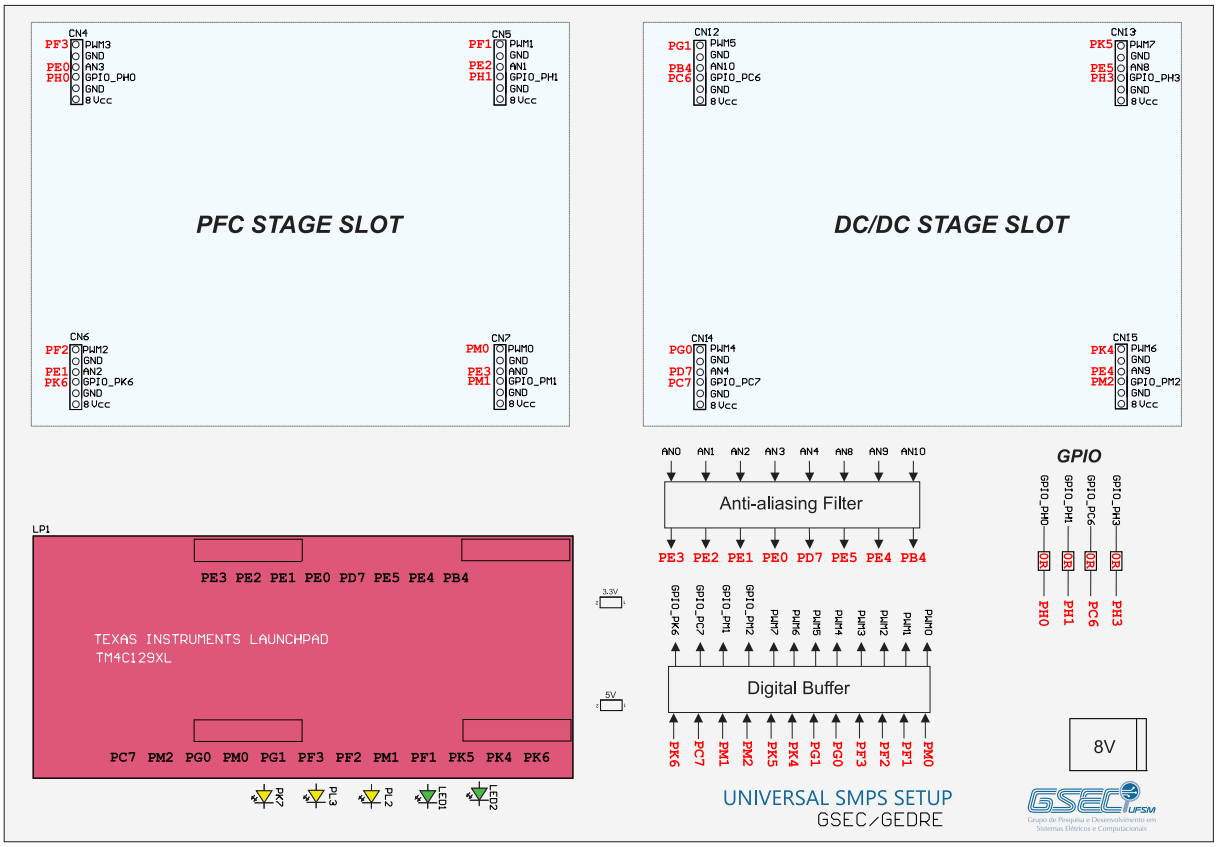
This appendix presents the experimental setup employed in this thesis. In order to accelerate the development of the experimental examinations, the implemented setup employs a modular concept. Several modules compose the experimental setup: gate-driver module, voltage and current sensors modules, power converter module, and the main control board that interconnects the above modules.

E.1 MAIN CONTROL BOARD MODULE - MCBM

Fig. 126 shows the main control board (MCBM) structure in a high-level representation. Compose this module the microcontroller (MCU) slot, a digital buffer, the analogical anti-aliasing filter, and GPIO signals. The digital signals from the MCU are amplified by the digital buffer and directed to connectors CN#, where the power converter module under test is attached. The gate-driver module is connected directly to the board of the power converter under test. Thus, in the power converter board, the PWM signal from CN# is directed to the gate-driver module and from this module to the MOSFETs in the converter. Voltage and current sensor modules are also attached to the power converter board. These sensors modules convert the measured levels into a current signal which is sent through the CN# connector to the current-to-voltage conversion stage found in the main control board. Finally, this voltage signal is filtered by the anti-aliasing stage and sampled by the MCU.

The circuit diagram of the MCBM is divided into two parts. Fig. 127 shows the circuit diagram of the

Figure 126 – High level representation of the Main control board



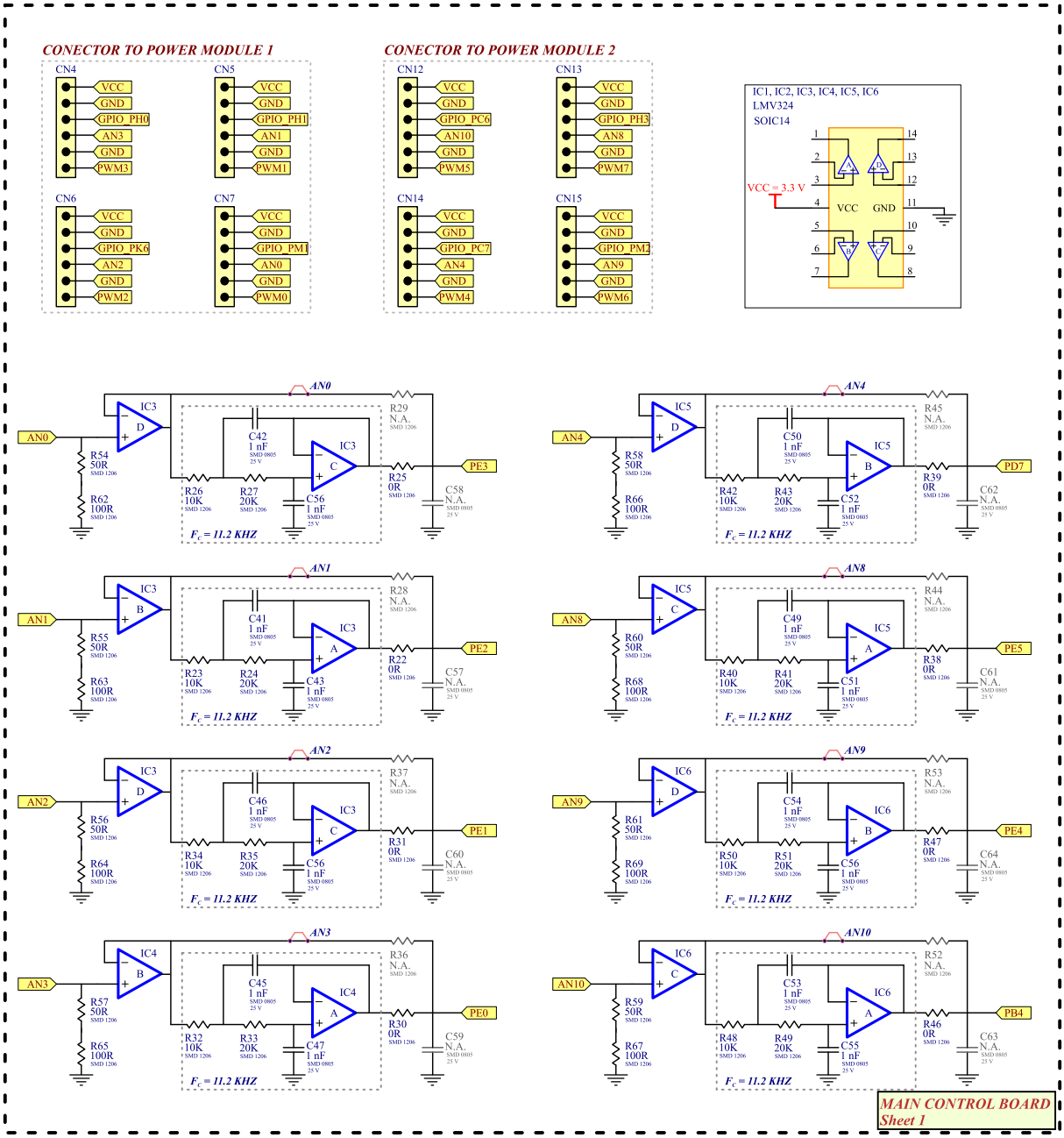
Source: Author.

analog signal conditioning. Initially, the current-to-voltage conversion of the signal that comes from the sensors modules is performed. In sequence, this signal is filtered to avoid the aliasing effect in the digital system. The anti-aliasing filter is implemented by the Sallen-key structure, that allows the realization of different kind of filters, for instance, LPF, BPF, and HPF, without any layout alteration.

Fig. 128 shows the circuit diagram of the MCBM that performs the digital signal conditioning. The digital signals from the MCU are amplified by the digital buffer (SN7407). Furthermore, Fig. 128 shows the details of the MCU slot and the power source that supplies all the modules of the setup (except the power converter).

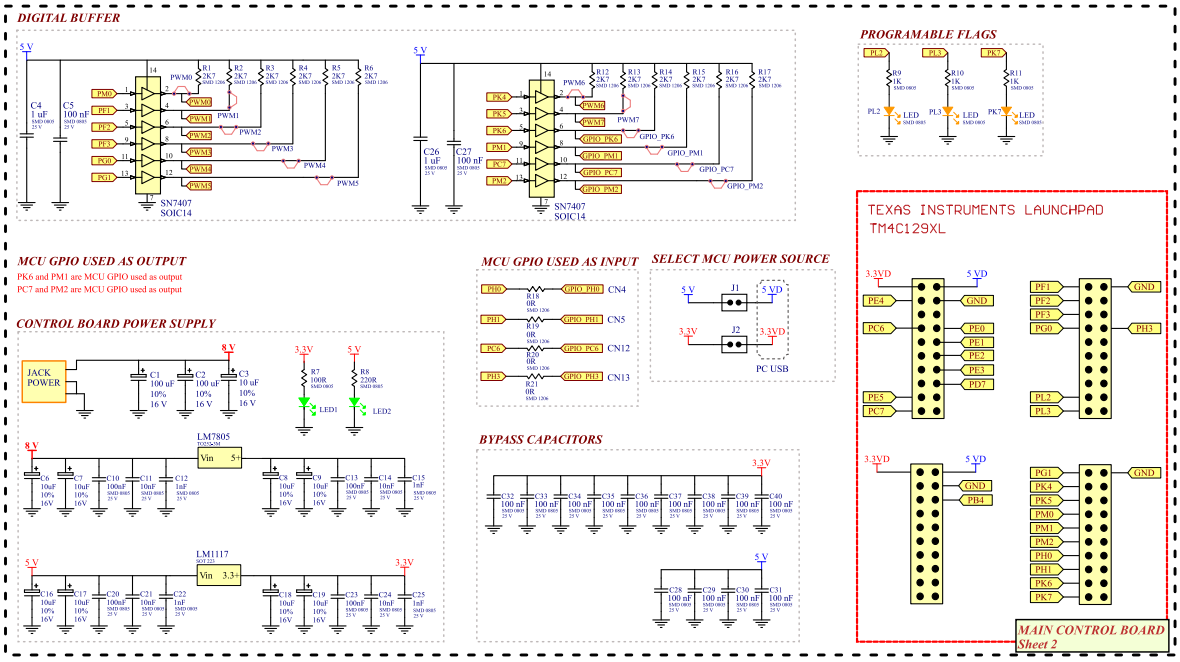
Fig. 129 shows the photography of the implemented MCBM, where the main stages are highlighted.

Figure 127 – Schematic of the analogical signal conditioning circuit in the main control board module.



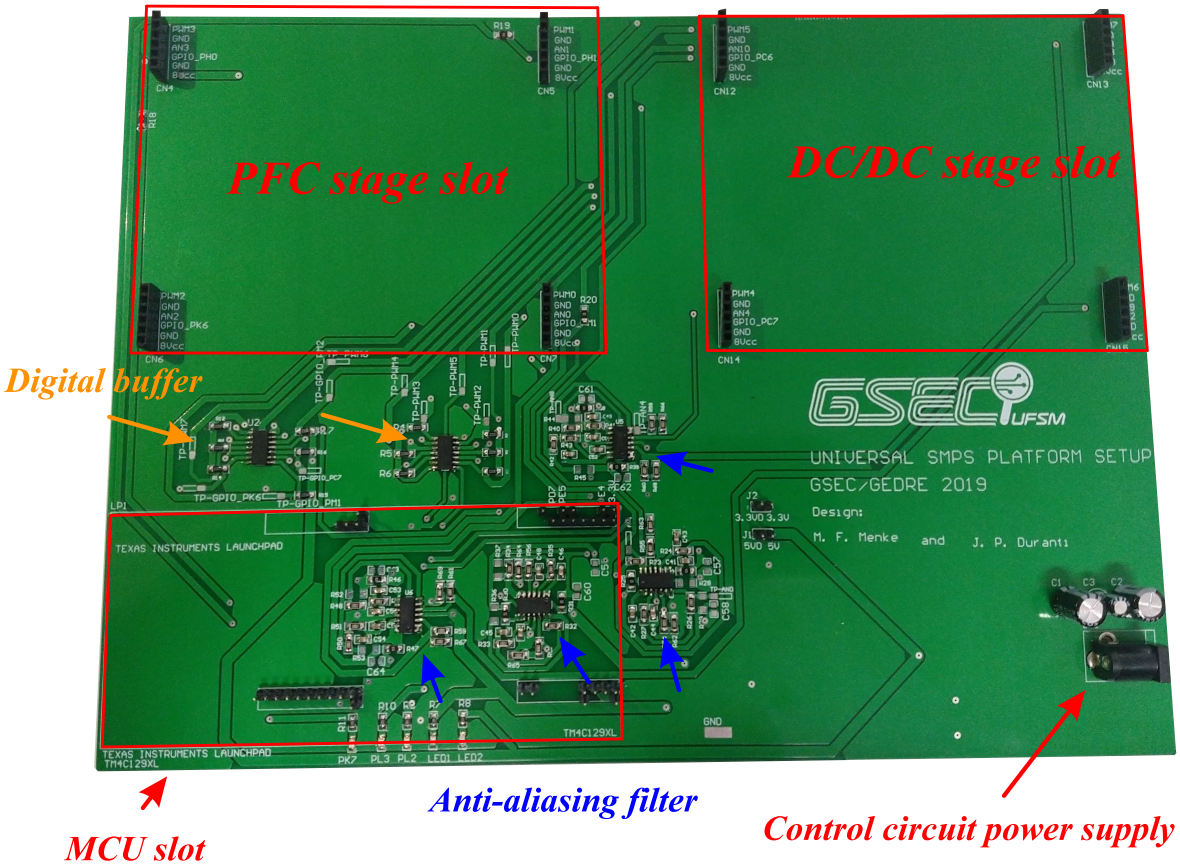
Source: Author.

Figure 128 – Schematic of the digital signal conditioning circuit and power sources in the main control board module.



Source: Author.

Figure 129 – Photography of the implemented main control board module.

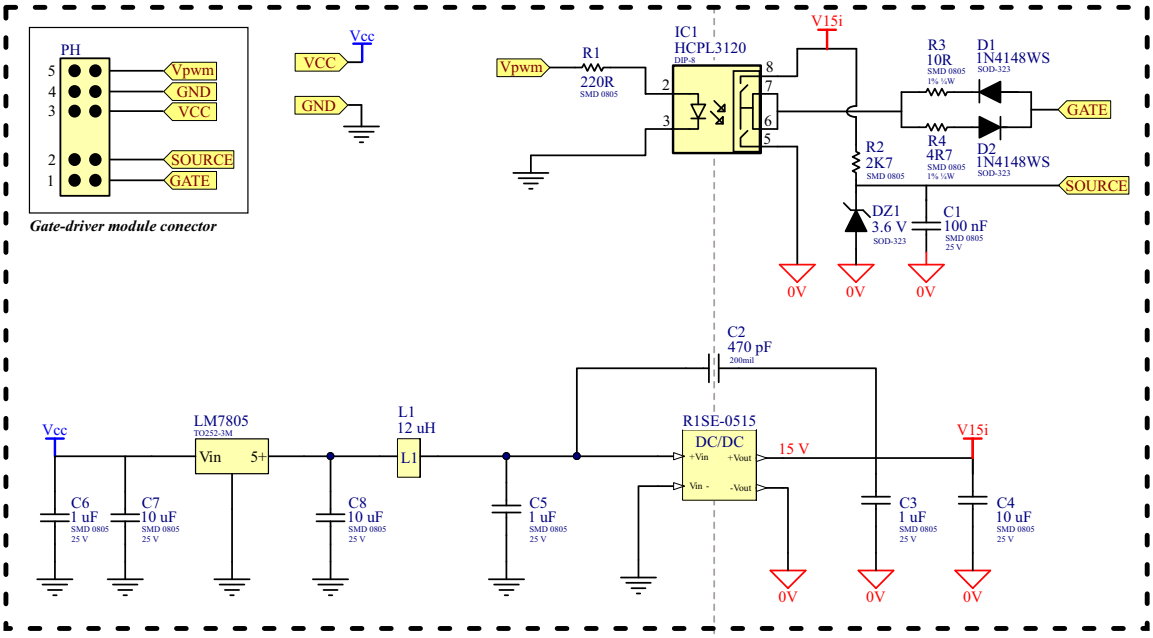


Source: Author.

E.2 GATE-DRIVER MODULE - GDM

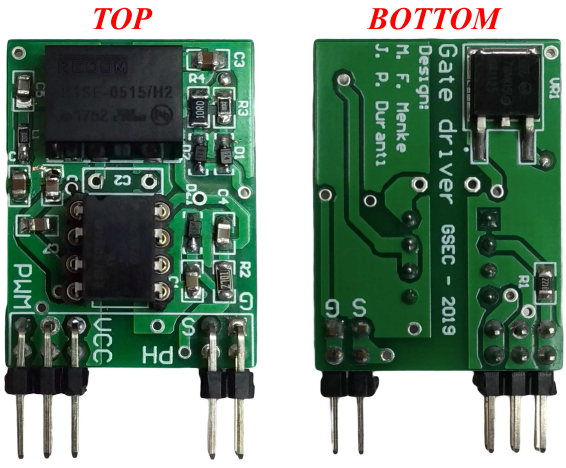
The gate-driver module is responsible for generating the appropriate signal for the MOSFET gate-source network. The GDM, connected directly to the power converter board, receives from the MCBM the PWM signal and the power to supply this module. In the GDM, the PWM signal is isolated and then amplified. The circuit diagram of the gate driver module is shown in Fig. 130. The photography of the implemented GDM is shown in Fig. 131.

Figure 130 – Circuit diagram of the Gate-driver module.



Source: Author.

Figure 131 – Photography of the implemented gate-driver module.



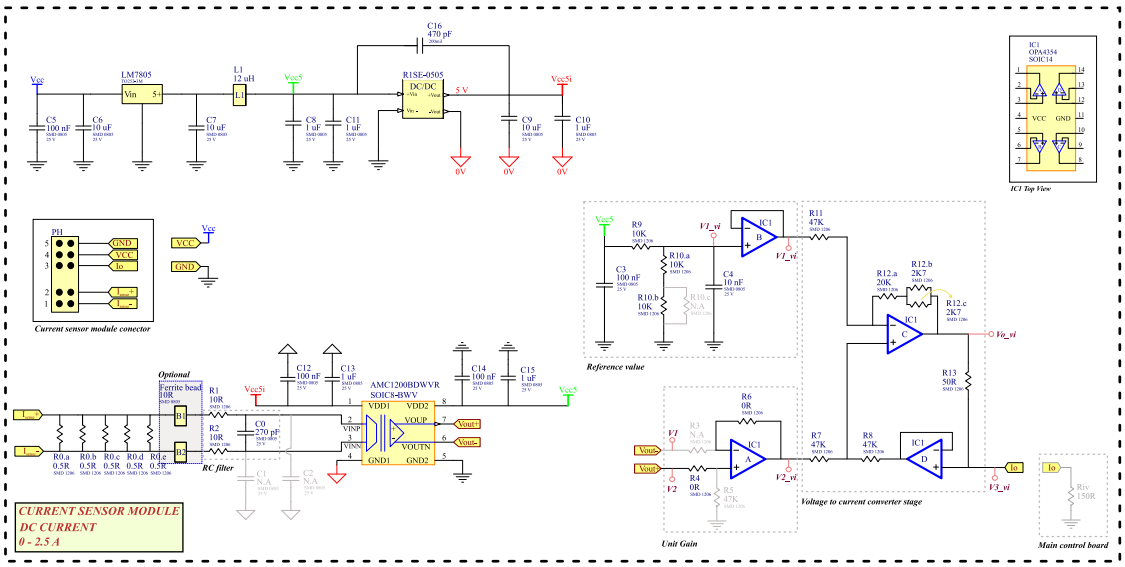
Source: Author.

E.3 CURRENT SENSOR MODULE - CSM

The current sensor module (CSM) is designed to measure the DC output current for the power converter under test. In the CSM, the current is estimated by measuring the voltage drop in a shunt resistor. The voltage drop in the shunt resistor is amplified, isolated, and converted to a current signal (4-20 mA). This 4-20 mA signal is sent to the current-to-voltage conversion found at the MCBM. In the sequence, this voltage signal in the MCBM is filtered by the anti-aliasing filter (Low Pass Filter - LPF) and directed to the MCU pin associated with an ADC.

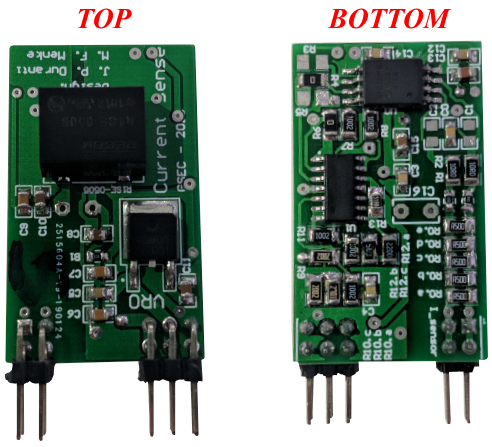
Fig. 132 shows circuit diagram of the current sensor module. The photography of the implemented module is shown in Fig. 133.

Figure 132 – Circuit diagram of the Current sensor module - CSM.



Source: Author.

Figure 133 – Photography of the implemented current sensor module.

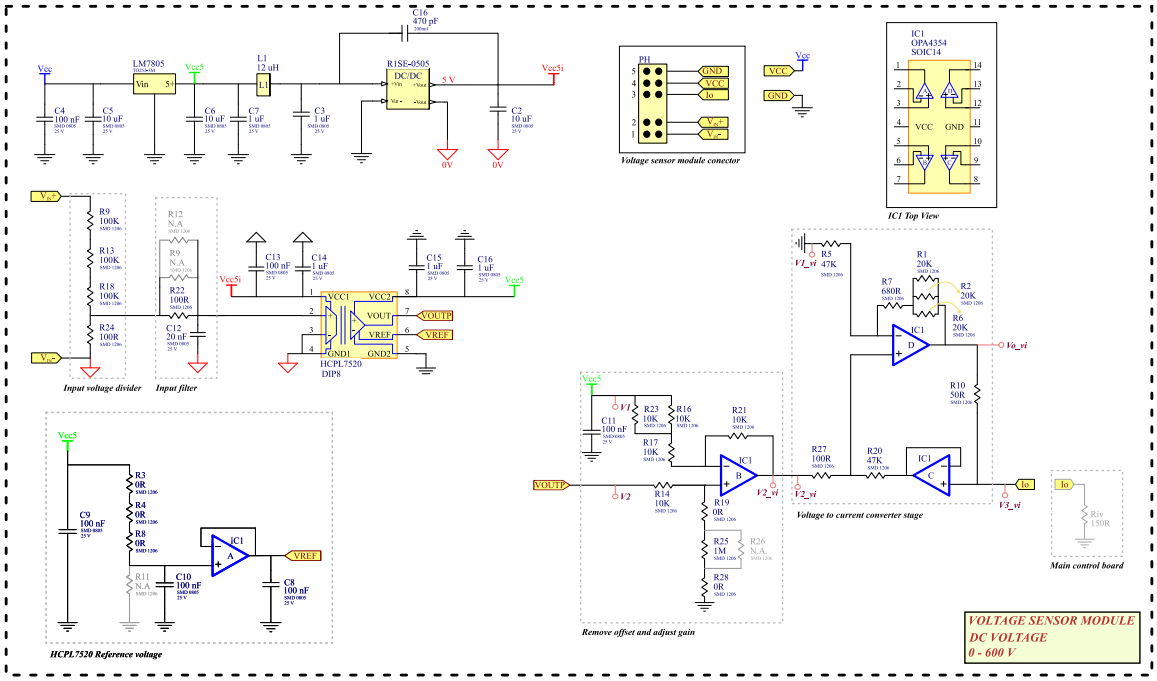


Source: Author.

E.4 VOLTAGE SENSOR MODULE - VSM

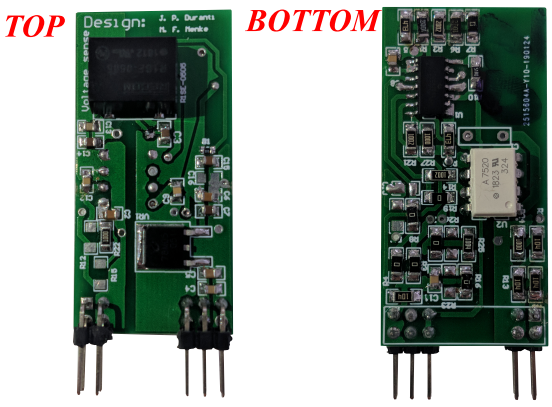
Given the necessity to measure the voltage levels on power electronics converters, a voltage sensor module (VSM) is conceived. In the VSM, the measured signal is converted to a current signal and send to MCBM, where this signal is converted into voltage and filter by the LPF. Fig. 134 shows circuit diagram of the VSM. Fig. 135 shows the photography of the VSM.

Figure 134 – Circuit diagram of the Voltage sensor module - VSM.



Source: Author.

Figure 135 – Photography of the implemented voltage sensor module - VSM.

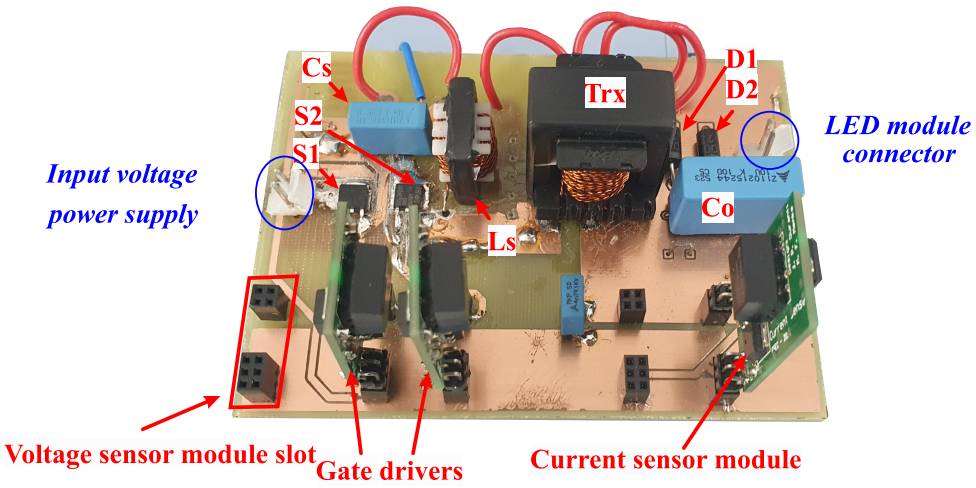


Source: Author.

E.5 POWER CONVERTER MODULE - LLC CONVERTER

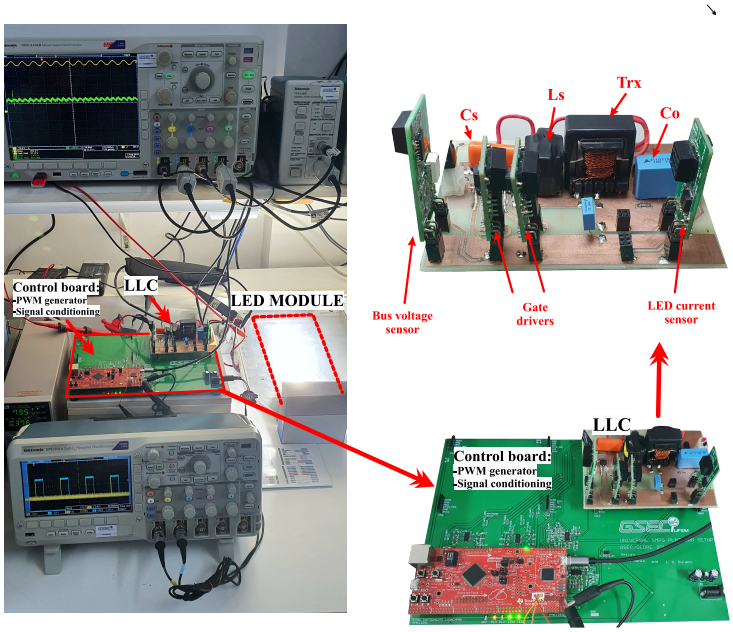
The power converter module is the own converter under test. In this thesis, the LLC resonant power converter is utilized. The photography of the implemented LLC converter is shown Fig. 136. As can be seen, the LLC board is designed to accommodate the gate-driver and sensors modules. Finally, the LLC board is attached to the MCBM, as shown in Fig. 137. Fig. 138 shows the circuit diagram of the power converter module, here given by the LLC resonant converter.

Figure 136 – Photography of the implemented LLC converter.



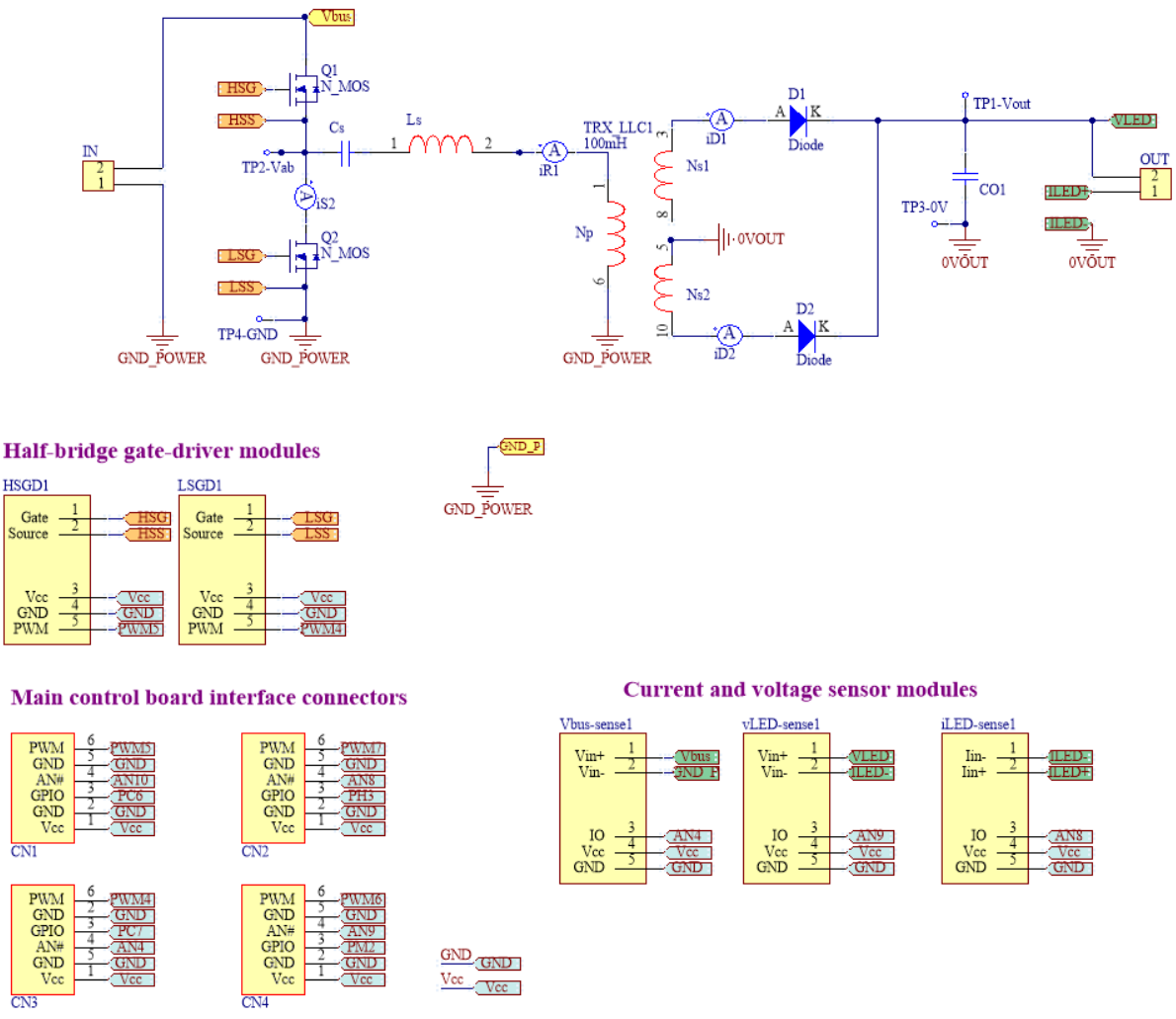
Source: Author.

Figure 137 – Photography of the laboratory test bench.



Source: Author.

Figure 138 – Circuit diagram of the LLC power module.



Source: Author.

APPENDIX F - MODEL REFERENCE ADAPTIVE CONTROLLER

Chapter 6 proposes a new hybrid controller for the LLC resonant LED driver, composed of a conventional PI subsystem and an adaptive periodic disturbance subsystem. This appendix presents the MRAC controller adapted to LLC resonant LED driver and its comparison with the proposed PI&APDR controller. This comparison intends to evaluate the performance of the proposed controller with a system that naturally presents high robustness again parametric variation and disturbances rejection, such as adaptive controllers.

F.1 PLANT MODELING AND ASSUMPTIONS

In order to obtain a discrete-time mathematical model of the plant, needed to design the MRAC controller, the following analysis is developed.

Consider the SISO (Single input Single output) plant in discrete-time given by (F.1). Which $G_p(z)$ represents the modeled part of the LLC resonant LED driver plant; $\mu\Delta_m(z)$ and $\mu\Delta_a(z)$ are the unmodeled dynamics of multiplicative and additive type, respectively; $y(z)$ (in this case, i_{LED}) is the plant output and $u(z)$ is the plant input (in this case, the control action: HB f_{sw} modulation).

$$\frac{y(z)}{u(z)} = G(z) = G_p(z)(1+\mu\Delta_m(z)) + \mu\Delta_a(z) \tag{F.1}$$

The modeled part of the plant is given by (F.2).

$$G_p(z) = k_p \frac{Z_p(z)}{R_p(z)} \tag{F.2}$$

In the same way that is was done in (IOANNOU AND TSAKALIS, 1986), the following assumptions are made for (F.2):
A1: $Z_p(z)$ and $R_p(z)$ are monic polynomials of degree m_p and n_p, respectively;
A2: $Z_p(z)$ is a Schur polynomial;
A3: the relative degree $n* = n_p - m_p$ and the signal of k_p are known.

Besides, for the unmodelled dynamics of the plant it is assumed that:
A4: $\Delta_a(z)$ is a strictly proper and Schur transfer function;
A5: $\Delta_m(z)$ is a Schur transfer function;
A6: The only *a priori* information required of $\Delta_a(z)$ and $\Delta_m(z)$ is a lower bound on the stability margin p of its poles.

F.2 ADAPTIVE CONTROL STRATEGY

The purpose of the MRAC is to automatically determine the parameters of the controller, such that the closed-loop system output (y) behave as close as possible to the predetermined reference model output (y_m), represented by the transfer function $W_m(z)$ (IOANNOU AND TSAKALIS, 1986), (MASSING ET AL., 2012), defined by (F.3).

$$W_m(z) = \frac{y_m(z)}{r(z)} = k_m \frac{Z_m(z)}{R_m(z)} \tag{F.3}$$

Being considered for (F.3) the following assumptions:
A7: $Z_m(z)$ and $R_m(z)$ are arbitrary Schur monic polynomials of degree q_m and p_m, respectively (IOANNOU AND TSAKALIS, 1986).
A8: The relative degree $n_m^* = p_m - q_m$ is the same as that of $G_p(z)$, i.e, $n^* = n_m^*$.

The input of $W_m(z)$ is defined by the reference r, a uniformly bounded signal. The outcome of (F.3) is used to generate the signal y_m, which is the desired value of y (i_{LED}).

For the control system achieve the desired performance, the control law is computed from (F.4) (LOZANO-LEAL ET AL., 1990). Where $\boldsymbol{\theta}^T[k]$ given in (F.2) is the weighting parameters vector, and $\boldsymbol{\omega}^T[k]$ defined in (F.5), is an auxiliary vector.

$$\boldsymbol{\theta}^T[k]\boldsymbol{\omega}[k] + r[k] = 0 \tag{F.4}$$

$$\begin{aligned}\boldsymbol{\theta}^T[k] &= \begin{bmatrix} \boldsymbol{\theta_1}^T[k] & \boldsymbol{\theta_2}^T[k] & \theta_y[k] & \theta_u[k] & \theta_{\sin}[k] & \theta_{\cos}[k] \end{bmatrix} \\ \boldsymbol{\omega}^T[k] &= \begin{bmatrix} \boldsymbol{\omega_1}^T[k] & \boldsymbol{\omega_2}^T[k] & y[k] & u[k] & V_{\sin}[k] & V_{\cos}[k] \end{bmatrix}\end{aligned} \tag{F.5}$$

From (F.2) and (F.5), $u[k]$ is the plant input; $\boldsymbol{\omega}_1[k]$ and $\boldsymbol{\omega}_2[k]$ are filters outputs of matching equation between reference model and closed-loop system; $V_{sin}[k]$ is bus voltage AC in phase component, and $V_{cos}[k]$ is the quadrature component with the sinusoidal disturbance. These two terms are added to the traditional MRAC controller in order to achieve ARC, attenuating the bus voltage ripple transmission to the LED current, allowing the use of long lifetime F-Cap.

Considering (F.4) and its variable definitions, it is possible to solve it for $u[k]$, as given by (F.6).

$$u[k] = \frac{\boldsymbol{\theta_1}^T[k]\boldsymbol{\omega_1}[k] + \boldsymbol{\theta_2}^T[k]\boldsymbol{\omega_2}[k] + \theta_y[k]y[k] + \theta_{\sin}[k]V_{\sin}[k] + \theta_{\cos}[k]V_{\cos}[k] + r[k]}{-\theta_u[k]} \tag{F.6}$$

The vector $\omega_1(z)$ is given by (F.7), and $\boldsymbol{\omega_2}(z)$ by (F.8).

$$\boldsymbol{\omega_1}(z) = \frac{\alpha_f(z)}{\Lambda_f(z)}u(z) = (z\boldsymbol{I} - \boldsymbol{F})^{-1}\boldsymbol{q}u(z) \tag{F.7}$$

$$\boldsymbol{\omega_2}(z) = \frac{\alpha_f(z)}{\Lambda_f(z)}u(z) = (z\boldsymbol{I} - \boldsymbol{F})^{-1}\boldsymbol{q}y(z) \tag{F.8}$$

Where: the pair $(\boldsymbol{F}, \boldsymbol{q})$ is controllable. The magnitude of the matrices $\boldsymbol{F}$ and $\boldsymbol{q}$ is directly related to the controller dynamic. The eigenvalues of $\boldsymbol{F}$ are related to the convergence speed of the adaptive algorithm.

With the control law specified, the automatic adaption of its parameters has to be developed. In this way, the adopted parametric adaption algorithm is given by (F.9).

$$\boldsymbol{\theta}[k+1] = \boldsymbol{\theta}[k] - \alpha\frac{\boldsymbol{\Gamma\zeta}[k]\varepsilon[k]}{m^2[k]} \tag{F.9}$$

Where: α and $\boldsymbol{\Gamma}$ are design positive constants, and ε is the augmented error expressed by (F.10).

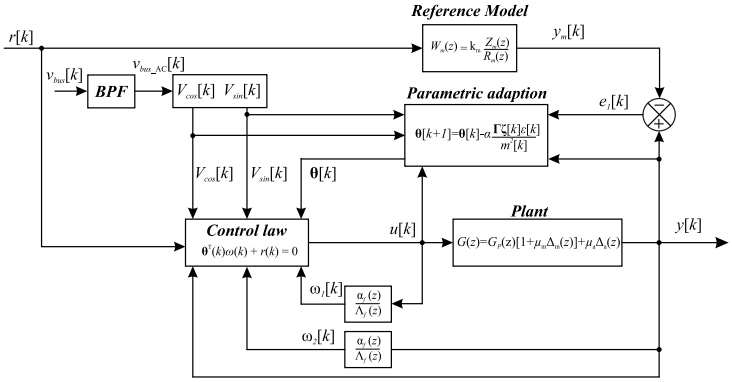
$$\varepsilon(k) = y(k) + \boldsymbol{\theta}^T(k)\boldsymbol{\zeta}(k) \tag{F.10}$$

The augmented error is used to guarantee the convergence of the algorithm. Being, $\boldsymbol{\zeta}[k] = W_m[k]\boldsymbol{\omega}[k]$ an auxiliary vector. The normalized function $m^2[k]$ is expressed by (F.11).

$$m^2(k) = 1 + \boldsymbol{\zeta}^T(k)\boldsymbol{\Gamma\zeta}(k) \tag{F.11}$$

In order to simplify the representation of the MRAC controller, its block diagram is shown in Fig. 139. BPF is a Band Pass Filter implemented to filter the 100 and 120 Hz AC component of the bus voltage. The filtered AC component is defined as the $V_{sin}[k]$ component, being $V_{cos}[k]$ obtained from the derivation of $V_{sin}[k]$.

Figure 139 – Block diagram of the adaptive controller.



Source: Author.

F.3 MRAC DESIGN

The adaptative controller design consists of determining the desired closed-loop performance in terms of the reference model choice. However, it is necessary to know the dynamic behavior of modeled part of the plant .

F.3.1 Discrete-time nominal model of the plant

In order to simplify the MRAC design, the modeled system dynamic behavior for the given operation point will be represented through a TF with reduced order, being neglected the high-frequency dynamics. Besides, in order to satisfy the assumption **A2**, the non-minimum zero of the LLC is neglected since its frequency is close to the switching frequency, in this case, 93.55 kHz. The practice of neglecting the high-frequency dynamics is usual during the MRAC design since it presents high robustness against unmodeled dynamics of the converter (TAMBARA ET AL., 2017). Thus, to obtain a reduced nominal model of the plant, a second-order small-signal approximation for the LLC LED driver is used, given by (F.12).

$$G_p(s) = \frac{\hat{i}_{LED}}{\hat{f}_{SN}} = \frac{K}{(s^2 + as + b)} \tag{F.12}$$

For the operation point where the output current is 1.15 A, the LLC resonant LED driver second-order approximation is given by (F.13).

$$G_p(s) = \frac{\hat{i}_{LED}}{\hat{f}_{SN}} = \frac{-6.847 \cdot 10^9}{(s^2 + 1.335 \cdot 10^4 s + 8.906 \cdot 10^9)} \tag{F.13}$$

Employing the zero-order-hold discretization method with a sampling frequency (f_{sa}) equal to 40 kHz, the discrete-time reduced nominal model of the plant (LLC and LPF) is obtained, given by (F.14), which correspond to the modeled part of the plant (F.2).

$$G_p(z) = \frac{-1.8347(z + 0.8929)}{z^2 - 1.265z + 0.7162} \tag{F.14}$$

F.3.2 Model reference

Since the closed-loop performance of the MRAC is a function of the reference model, to obtain a controlled system that presents a short settling time and no overshoot, a second-order model reference is selected, with quality factor Q = 0.5 and natural frequency $\omega = 10000\ rad/s$ as is given in (F.15).

$$W_m(s) = \frac{{\omega_n}^2}{s^2 + \frac{\omega_n}{Q}s + {\omega_n}^2} = \frac{1 \cdot 10^8}{s^2 + 20000s + 1 \cdot 10^8} \tag{F.15}$$

Discretizing the reference model with ZOH, a second-order system with relative degree $n_m^* = 1$ is obtained, as shown in (F.16). Which is in accordance with assumption **A8**, since the plant (F.14) also has a relative degree $n^* = 1$.

$$W_m(z) = \frac{0.026499(z + 0.8464)}{(z - 0.7788)^2} \tag{F.16}$$

F.3.3 Controller parameters

The controller parameters design consists basically in defining the initial conditions for the controller gains of the adaptive scheme, e.g., $\boldsymbol{\theta}^T(0)$, and the parameters $\boldsymbol{\Gamma}$ and α in order to obtain a short transient period during the converter startup. Table 20 presents the adopted parameters of the algorithm employed in this work. These parameters were chosen after successive simulations and experimental results.

Table 20 – MRAC parameters

Symbol	Parameter	Values
θ^T	Initial gains vector	[-8 -1.7 0.225 8 0 0]
ζ^T	Auxiliary vector	[0 0 0 0 0 0]
Γ	Adaption Matrix	$400 * I_{6X6}$
α	Scalar design	2000

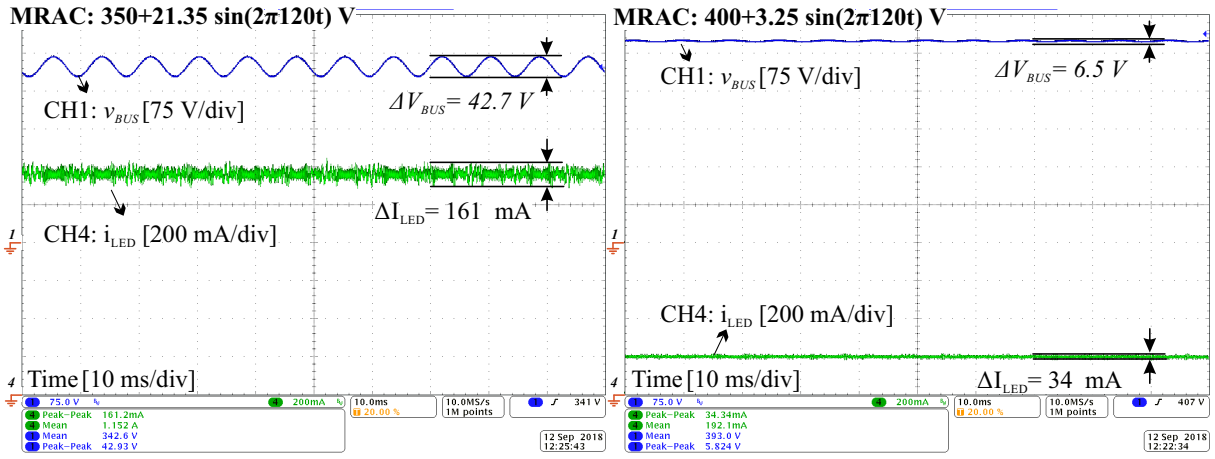
Source: Author.

F.4 EXPERIMENTAL RESULTS

The designed control systems assessment starts with the LLC resonant LED driver steady-state performance at the extreme operating conditions, minimum bus voltage (350 V_{dc}) with maximum power ($I_{LED} = 1.15\ A$), and nominal bus voltage (400 V_{dc}) with minimum output power ($I_{LED} = 0.20\ A$). Fig. 140 shows v_{BUS} and i_{LED} measurement for LLC LED driver operating with the MRAC controller. Fig. 141 shows this same measurement for the proposed PI&APDR controller. As can be seen, a reduced Δi_{LED} is noticed at the extreme operational conditions, being, therefore, the MRAC performance similar to the PI&APDR controller.

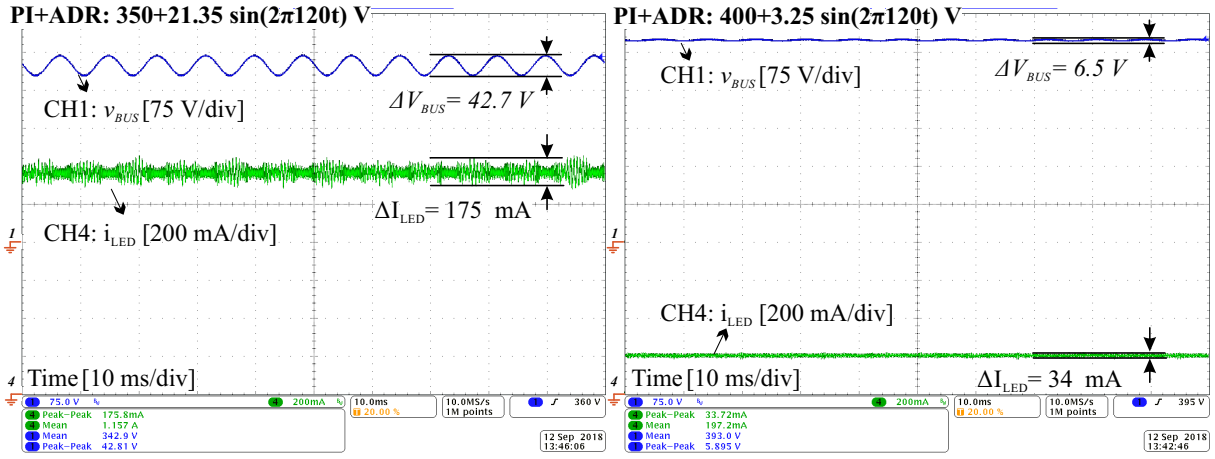
It should be noticed that the PI&APDR presents an impressive performance, which is similar to the MRAC without the drawback of being more complex and demands massive data processing, which allows its implementation in a low-cost MCU. Numerically, the time spent to process each control law calculations over a single step, which period is defined by the sampling frequency, is given by 21.64% for the PI, 25.10% for the IQR, 43.03% for MRAC, and 31.5% for the proposed PI+ADR. Analyzing this

Figure 140 – Steady-state v_{BUS} and i_{LED} of the LLC LED driver at the extreme operational conditions employing MRAC controller.



Source: Author.

Figure 141 – Steady-state v_{BUS} and i_{LED} of the LLC LED driver at the extreme operational conditions employing PI+ADR controller.



Source: Author.

data shows that the PI controller has the shortest time necessary to process all the related sampling and calculus. In contrast, the MRAC needs almost twice more time to finish its calculations. Furthermore, even that the proposed PI&APDR needs more time than the IQR controller, compared with the MRAC, the proposed system is considerably more simple, demanding the shortest time to be computed.

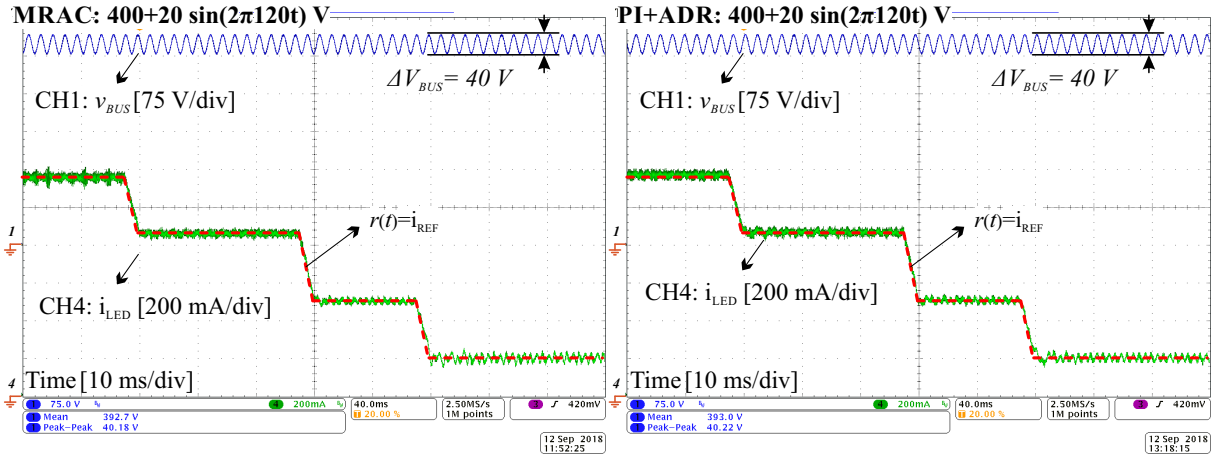
F.4.1 Reference tracking evaluation

In order to evaluate the capability of each controller to track the reference and reduce output ripple at different loads and V_{BUS} conditions, the LED current, its reference, and the bus voltage are evaluated under the same dimming profile as follows.

Fig 142 shows the experimental measurement of v_{BUS} and i_{LED} when the MRAC (left side) or

PI&APDR (right side) controller is employed. As it can be seen, for both cases, the average LED current tracks the reference, and a reduced output current ripple is noticed.

Figure 142 – LLC LED driver v_{BUS} and i_{LED} under dimming conditions operating with the designed IQR controller.



Source: Author.

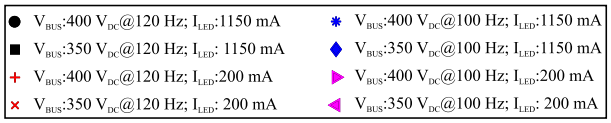
F.4.2 Active ripple compensation evaluation

To obtain a better insight of the LED current ripple attenuation, the driver modulation index (Mod(%)) in comparison to the IEEE Std 1789-2015 (IEEE STD 1789, 2015) limits have to be analyzed. Thus, considering that the LED operates in its linear region, where the output light is directly proportional to the LED forward current, the Mod(%) is estimated (Mod*(%)) from the FFT decomposition of i_{LED}. In this way, each LED current harmonic is translated into the Mod*(%) at different frequencies.

Initially, pay attention to Fig. 143, which summarizes all the operating points tested and gives the respective symbols used to express the Mod*(%) in Fig. 144. These operating points tested covers all the range of possible conditions that the LLC resonant LED driver will be subjected in a system that employs reduced DC-link capacitance and operates with universal input voltage and dimming capability.

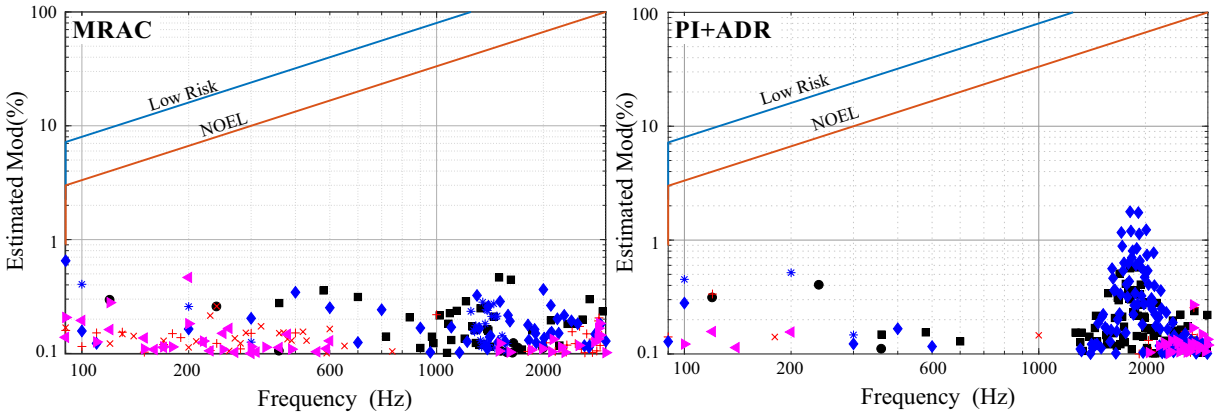
Finally, Fig. 144 shows the Mod*(%) of the LLC LED driver employing the MRAC (left side) and the proposed PI+ADR (right side) controller. As it can be seen, a very small Mod*(%) is noticed around Δv_{BUS} frequency for a universal input voltage LED driver ($100\ Hz - 120\ Hz$).

Figure 143 – Legend of the LLC LED driver estimated modulation index figures evaluation.



Source: Author.

Figure 144 – LLC LED driver estimated modulation index in comparison to the IEEE 1789-2015 recommendations limits.



Source: Author.

APPENDIX G - SUPPLEMENTARY MATERIAL

Throughout this thesis, several simulations and theoretical analyses have been developed. Simulations are mainly developed in PSIM. Theoretical analyses are supported by numerical computation, where MATLAB and Mathematica software have been employed. In this way, for the sake of clarity, the main PSIM simulation files, MATLAB scripts, and Wolfram Mathematica notebooks developed can be accessed and downloaded from the folder shared in Google Drive.

G.1 LINK

The link below gives accesses to the provided files:
https://drive.google.com/drive/folders/1e5RousTB_vBUjXR7b3p7lOTt409ayJmg