Analysis and Design of Isolated SEPIC Converter with Greinacher Voltage Quadrupler Multiplier Cell

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***Abstract*— High step-up converters are required and used in photovoltaic applications, due to low voltage of photovoltaic modules. In this paper, an isolated dc-dc high step-up SEPIC with a Greinacher voltage quadrupler cell is presented. It has the advantage of continuous input current, high efficiency, high voltage gain, isolation and demands a single switch, being suitable for low power grid-tie photovoltaic systems. The operating principles and steady-state analysis are presented, including the detailed analysis of resonant stage, where the value of primary side capacitor is taken into account and plays an important role in the design of the converter, since it directly affects the resonance frequency and RMS current values. Simulation results are presented to validate the analysis and design.**

Keywords*— Isolated SEPIC, Resonant stage, Voltage quadrupler multiplier cell.

I. INTRODUCTION

The increase of photovoltaic systems, specifically low power grid-tie systems with two converters, makes high-step up dc-dc converter very important. These systems, as shown in Fig. 1, are also known as AC photovoltaic modules (module-integrated-converter – MIC), where a high step-up converter, in first stage, provides a high voltage gain and is connected to a grid-tie inverter. Galvanic isolation is desirable to maintain security of the whole system, besides mitigating leakage current and electromagnetic interference (EMI) problems [1].

Single-switch converters are more suitable for lower power applications, reducing volume, costs and complexity. Basic single-switch isolated topologies are: flyback, ZETA, SEPIC and Ćuk. Among these options, isolated SEPIC converter is a very good choice for this application with low input voltage and low output power, since it provides continuous input current and can significantly reduce the dc magnetizing current

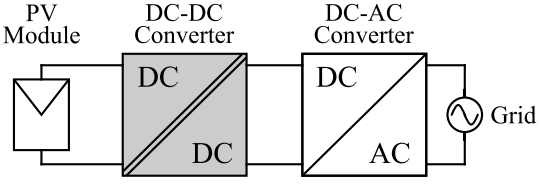

Fig. 1. MIC converter with emphasis on first stage.

with the appropriate choice of voltage multiplier cells (VMCs), allowing to use a transformer instead of coupled inductor [2].

VMCs applied on secondary side provide the advantages of increased converter static gain and clamped voltage spikes on diodes without elevating voltage stress over the switch, unlike VMCs applied on primary side. These VMCs used on secondary side are based on switched-capacitor techniques and the most commonly used are known as voltage doubler (VD) and voltage tripler (VT), with the possibility of expansion to raise voltage gain, although increasing the number of converter components [3], resulting in voltage quadrupler (VQ) and voltage quintupler (VQ5).

The goal of this work, besides showing operating principles, is to deduce the main equations of the selected converter, proving the accuracy of these equations, obtained considering the value of primary side capacitor. Section II briefly shows the reasons to choose the converter topology. In section III, theoretical analysis is made, including principle of operations and equations of resonant stage, besides the equations of current and voltage ripples, RMS and the static gain of converter. Simulation results are presented in section IV, showing converter operation and the accuracy of the equations, comparing theoretical and simulation results. Finally, in section V, some relevant conclusions about the work are made.

II. DERIVATION OF CONVERTER

The isolated SEPIC converter, shown in Fig. 2b is obtained from the classic topology, shown in Fig. 2a. Cantilever model can be used to represent the magnetic element (transformer or coupled inductor) [4]. Fig. 2c shows the converter with VMC on secondary side. Greinacher voltage doubler and quadrupler cells, shown in Fig. 3, can be used on secondary side. As mentioned before, an appropriate choice of VMC can significantly reduce the dc magnetizing current, guaranteeing that the magnetizing inductance, L_m, does not store energy. Thus, a transformer is used for galvanic isolation instead of a coupled inductor, consequently providing a better utilization of BxH curve, reducing its volume and its leakage inductance, L_{lk} [5]. This can be achieved by the use of VD and VQ cells, also known as pairs cells, but it is not possible with VT and VQ5 cells, also known as odds cells. In [6], isolated SEPIC converter

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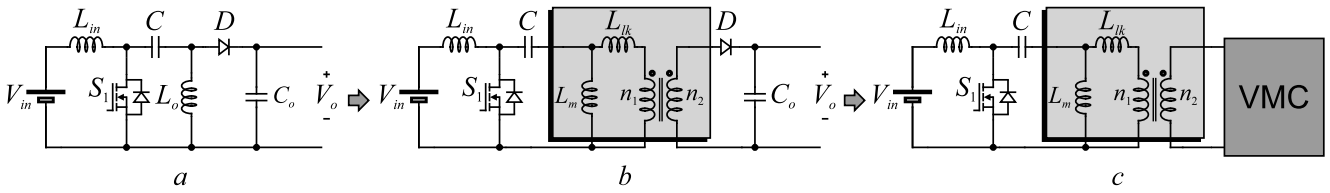

Fig. 2. Isolated SEPIC derivation : (a) Classic SEPIC converter; (b) Isolated SEPIC using cantilever model; (c) Isolated SEPIC with VMC on secondary side.

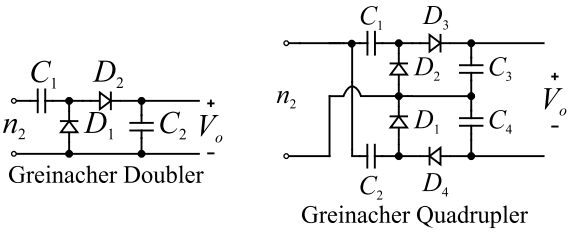

Fig. 3. Greinacher voltage multiplier cells used on secondary.

was analysed using a VD cell on secondary side, using a similar methodology in comparison with this work.

Table I summarizes the voltage gain of cells and the static gain of converters obtained with the insertion of these VMCs, based on [7], [8] and [9], where *D* is duty cycle of converter and *n* is the transformer turn ratio. In Fig. 4 the voltage gains of three converters are compared. In comparison with VDiSEPIC, VQiSEPIC has more components, however, its static gain is higher, allowing to design a transformer with smaller turns ratio and, besides that, the voltage stress across diodes and secondary capacitors are smaller.

TABLE I. VOLTAGE AND STATIC GAIN OF CELLS AND CONVERTERS.

Cell	Voltage gain	Topology	Static Gain (M)
–	–	SEPIC	$D/(1-D)$
–	–	Isolated SEPIC (iSEPIC)	$nD/(1-D)$
Greinacher VD	$1/D$	VDiSEPIC	$n/(1-D)$
Greinacher VQ	$2/D$	VQiSEPIC	$2n/(1-D)$

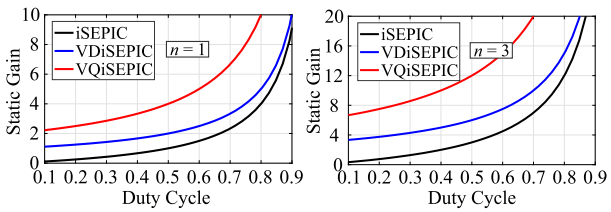

Fig. 4. Voltage gain of converters with and without pairs cells on secondary side.

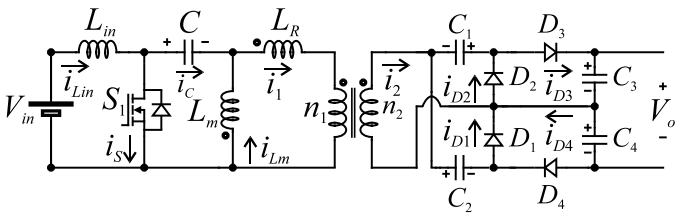

Fig. 5. Topology circuit of VQiSEPIC.

III. THEORETICAL ANALYSIS OF THE CONVERTER

The circuit of isolated SEPIC with VQ Greinacher cell (VQiSEPIC) is shown in Fig. 5. In order to evaluate the theoretical performance of this converter, the following features are approached in this section: principle of operation, voltage gain derivation, voltage stress and current stress.

A. Principle of operation

In order to simplify the steady-state analysis, the following assumptions are made:

1) All power devices are ideal;
2) The magnetizing inductor, L_m, is taken into account on the analysis, however, using a transformer with high quality material and good design, its impact is irrelevant, once its inductance is much higher than leakage inductance, L_{lk};
3) Output voltage is constant, therefore, capacitors C_3 and C_4 are not taken into account on the analysis.

The converter has three different resonant operation modeS, according to resonant period (T_r), switching period (T_s) and duty cycle. This can be better understood with Fig. 6, where these modes are presented. The best option is the first mode, nearly to second mode, where total switching losses are smaller, since that ZCS condition is obtained in all diodes and the value of switch current on turn-off transition is smaller than in third mode. This will receive more attention during the

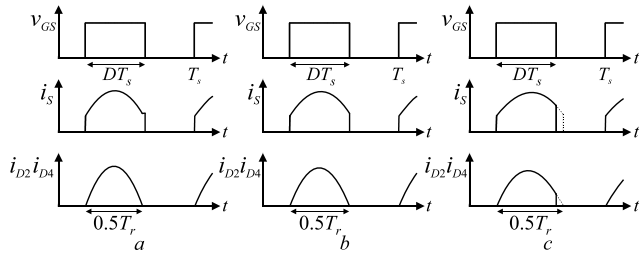

Fig. 6. Converter operation according to variation of resonance: (a) below resonance operation – first mode: $DTs > 0.5Tr$; (b) exactly resonance operation – second mode: $DTs = 0.5Tr$; (c) above resonance operation – third mode: $DTs < 0.5Tr$.

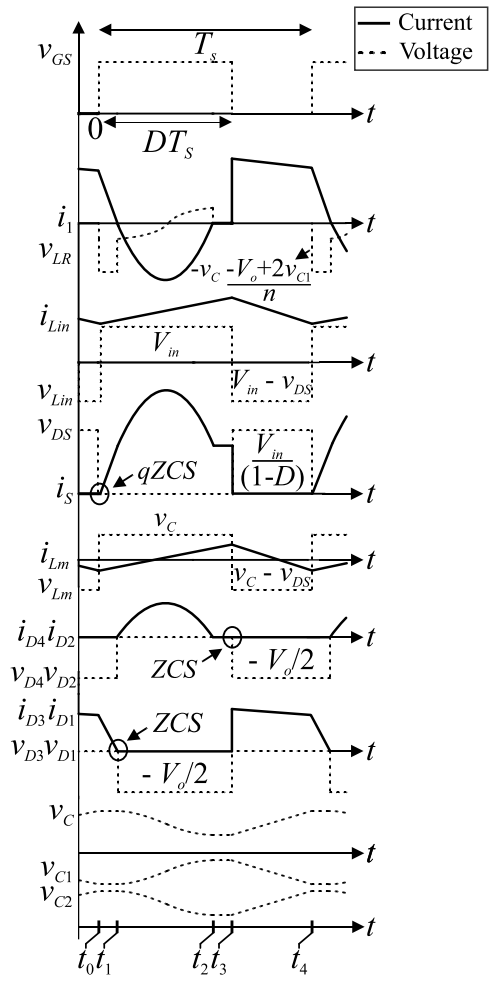

Fig. 7. Key waveforms of VQiSEPIC in CCM operation.

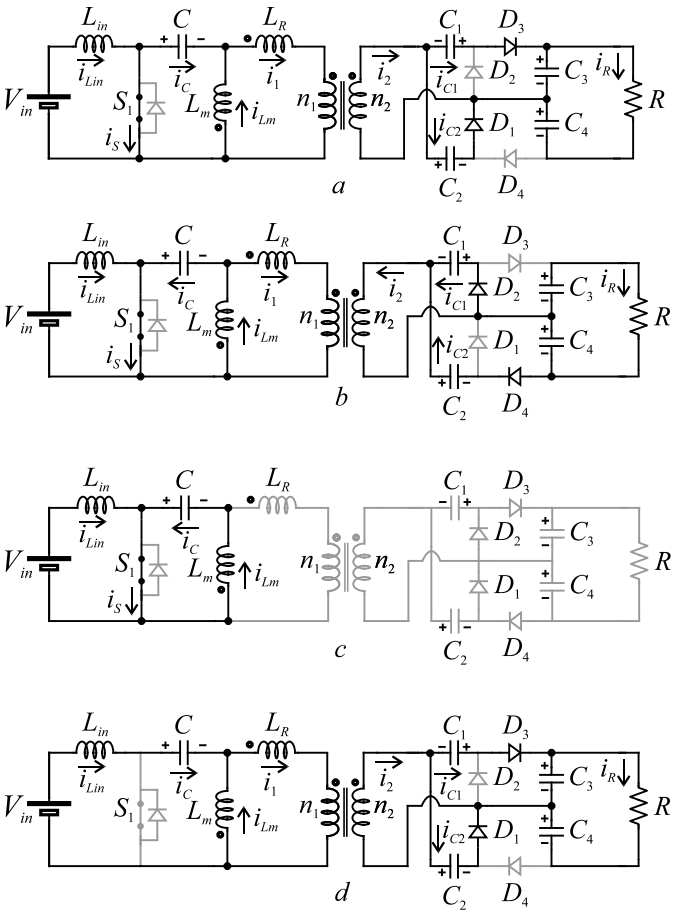

Fig. 8. Current flow path in four stages during one switching period in CCM operation: (a) Stage I; (b) Stage II; (c) Stage III; (d) Stage IV.

description of operation stage II, where this resonance occurs.

Fig. 7 shows the key waveforms of the converter in one switching period, in continuous-conduction-mode (CCM). It is important to mention that these waveforms are obtained for operation below resonance frequency. The converter has four operation stages in one switching period, as shown in Fig. 8. The converter operation is given as follows:

Stage I ($t_0 - t_1$): This stage begins when switch S_1 is turned on, and the primary current i_1 begins its linear decreasing, as well as current i_2, while switch current, i_S, slowly increases also linearly. This results in a quasi-ZCS turn on of the switch. This stage ends when current i_1 reaches 0 A and diodes D_1 and D_3 are turned off under ZCS condition. The duration of this stage is considerably smaller than stage II and, because of this, voltages across capacitors are constant on this stage.

Stage II ($t_1 - t_2$): This stage begins when current i_1 changes its direction, so diodes D_2 and D_4 are turned on. At this instant, a resonance occurs, hence currents and voltages are sinusoidal, charging the capacitor C_1 and discharging C and C_2. Voltage across L_{in} still being equal to V_{in}, and voltage across L_m is equal to v_C, so, both currents are increasing linearly. To analyse this resonance, it is necessary to obtain the equivalent circuit for this stage, shown in Fig. 9.

Magnetizing inductance is significantly higher than leakage inductance, and its ac ripple current is reduced, so, this element can be neglected in resonance analysis. In Fig. 9, inductance L_R is referred to secondary multiplying its inductance by square of turn ratio, n^2, and C is referred to secondary dividing its capacitance by n^2. Impedance Z_{RC3} can be approximated by resistance R. The parallel association with C_4 can be approximated by the capacitive impedance of C_4. So, following the steps shown in Fig. 9, the equivalent capacitance, C_{eq}, resonance frequency, f_r, and resonant impedance, Z_r, are given by

$$C_{eq} = \frac{\frac{C}{n^2}\left(C_4C_2 + C_4C_1 + C_2C_1\right)}{C_4C_2 + C_4C_1 + C_2C_1 + \frac{C}{n^2}C_4 + \frac{C}{n^2}C_2}. \quad (1)$$

$$f_r = \frac{1}{2\pi\sqrt{C_{eq}n^2L_R}}; \quad Z_r = \sqrt{\frac{n^2L_R}{C_{eq}}} \quad (2)$$

Hence, as mentioned before, there are three possibilities of operation regarding to resonant period, switching period and duty cycle. The best choice are values of T_r, T_s and D that make converter operates in first mode, near to second mode. In this

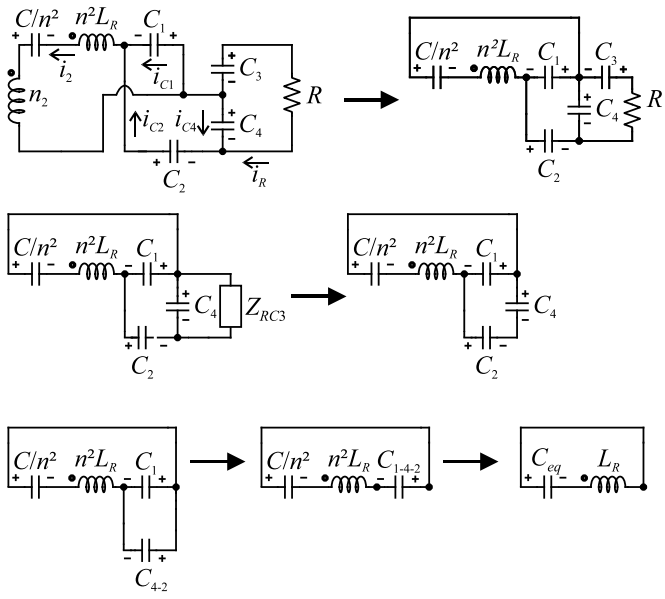

Fig. 9. Steps to obtain equivalent resonant circuit of Stage II.

case, ZCS condition is guaranteed to D_2 and D_4, besides D_1 and D_3, that also have ZCS regardless of operation mode. Besides that, root mean square (RMS) and peak value of i_s, i_{D2} and i_{D4} are considerable smaller than in fist operation mode far away from second mode. Finally, the main problems of third mode are the loss of ZCS on D_2 and D_4 and higher switch current on its turn-off transition, increasing the converter switching losses.

Stage III ($t_2 - t_3$): This stage begins when switch is still on, but there is no current left on transformer and diodes are off, so, voltages v_{C1} and v_{C2} are constant, equal to the value at the end of stage II. Once the duration of this stage is considerable smaller than previous stage, and C is in series with L_m, its voltage, v_C, also can be considered constant. This stage ends when S_1 is turned off, with losses, without soft-switching. Similar to stage I, this stage is very small and it happens in first and second modes of operation, but not in third.

Stage IV ($t_3 - t_4$): This stage begins when switch is turned off and diodes D_1 and D_3 are turned on, and there is current flux on transformer. Differently from stage II, this one occurs without resonance, and, consequently, currents and voltages are not sinusoidal, charging capacitors C and C_2 and discharging C_1. During this stage, the voltage across L_{in} is the difference between V_{in} and V_{DS}, resulting in a linear decreasing of i_{Lin}, while voltage across L_m is the difference between v_C and V_{DS}, also resulting in a linear decreasing of i_{Lm}.

B. Voltage and Current Stress

The voltage stress over the switch is given by

$$V_{DS} = \frac{V_{in}}{1-D}. \tag{3}$$

For all diodes, the voltage stresses are given by

$$V_{D1} = V_{D2} = V_{D3} = V_{D4} = -\frac{V_o}{2}. \tag{4}$$

It can be seen that even with the increase in static gain, voltage stress on switch is the same of classical isolated SEPIC, while voltage stress on diodes is smaller compared to classical isolated and to VDiSEPIC, where voltage stress across diodes are equal to output voltage.

As to RMS current values on diodes, it can be used the theory of general piecewise waveform, where a periodic waveform, composed of N piecewise segments has a RMS value of

$$\text{RMS} = \sqrt{\sum_{k=1}^{N} D_k u_k}, \tag{5}$$

where D_k is the duty cycle of segment k, and u_k is the contribution of segment k. The contribution depends on the shape of the segment.

According to [10], i_{D1} and i_{D3} have a trapezoidal segment, while i_{D2} and i_{D4} have a sinusoidal segment. From analysis of operation stages, it can be affirmed that i_{D2} and i_{D4} are equal to half of i_1 referred to secondary in stage II. In the same way, i_{D1} and i_{D3} are equal to half of i_{Lin} referred to secondary in stage IV. The portion of i_{D1} and i_{D3} during the stage I is neglected, since the duration of this stage is considerably smaller than the duration of stage IV and, therefore, it does not affect the RMS current evaluation. D_k of segment u_k of i_{D2} and i_{D4} is equal to $0.5T_r/T_s$, resulting in a RMS equation given by

$$i_{D2(rms)} = i_{D4(rms)} = \frac{\sqrt{\frac{1}{2} i^2_{1(pk)} \frac{0.5T_r}{T_s}}}{2n}. \tag{6}$$

D_k of segment u_k of i_{D1} and i_{D3} is equal to (1-D), resulting in a RMS equation given by

$$i_{D1(rms)} = i_{D3(rms)} = \frac{\sqrt{\frac{1}{3}\begin{pmatrix} i^2_{Lin(\min)} + \ldots \\ + i_{Lin(\min)} i_{Lin(\max)} + .. \\ + i^2_{Lin(\max)} \end{pmatrix}(1-D)}}{2n}. \tag{7}$$

Finally, as to switch RMS value, it is necessary to use the classical equation of RMS variable, once i_s waveform does not have a defined equation, given by

$$i_{s(rms)} = \sqrt{\frac{1}{T_s}\int_0^{T_s} {i_s}^2 dt} = \sqrt{\frac{1}{T_s}\left(\begin{pmatrix} \int_0^{T_r/2} \left(-i_1 + i_{Lin}\right)^2 dt \end{pmatrix} + .. + \begin{pmatrix} \int_{T_r/2}^{DT_s} {i_{Lin}}^2 dt \end{pmatrix}\right)}. \tag{8}$$

The solution of this equation will give

$$i_{s(rms)} = \sqrt{\frac{1}{T_s}\left(a - \frac{\left(\frac{b+c}{3}\right)}{{L_{in}}^2} + d + e - f - \left(\frac{g+h}{L_{in}}\right)\right)}, \tag{9}$$

where the complete definition of all these parameters can be found in [6], since the primary of both converters are the same.

C. Voltage and current ripples

The voltage and current ripples are obtained by the integral of current on inductor and voltage of capacitor in a switching period, analyzing and rearranging the therms. So, current ripple of i_{Lin} is given by

$$\Delta i_{Lin} = i_{Lin}(DT) - i_{Lin}(0) = \frac{1}{L_{in}} V_{in} DT. \quad (10)$$

Voltage ripple of v_C is given by

$$\Delta v_c = v_c(T) - v_c(DT) = \frac{I_{in}(1-D)}{Cf_s}. \quad (11)$$

Voltage ripple of v_{C1} is given by

$$\Delta v_{c2} = \Delta v_{c1} = v_{c1}(DT) - v_{c1}(T) = \frac{I_{in}(1-D)}{nC_1 f_s}. \quad (12)$$

IV. SIMULATION RESULTS

This section presents simulation results of the VQiSEPIC converter, in order to verify the theoretical analysis approached in this paper. The simulation was performed with the parameters presented in Table II, using a time step of 0.1 ns.

TABLE II. PARAMETERS OF SIMULATION

Parameter	Value
Output power	200 W
f_s	24 kHz
T_s	41.66 µs
V_{in}	37.4 V
V_o	400 V
D	0.44
n	1:3
L_{in}	1 mH
L_R	1 µH
L_m	1 mH
C	50 µF
$C_{1,2}$	2.5 µF
$C_{3,4}$	1 mF
R	800 Ω

Using (2), the calculated resonance frequency is equal to 28.07 kHz, while in simulation it is equal to 28.05 kHz, resulting in a small difference of 20 Hz, less than 1% of error. v_{GS}, i_{D2} and v_{D2} are shown in Fig. 10*a*, while v_{GS}, i_{D4} and v_{D4} are shown in Fig. 10*b*. As can be seen in this figures, converter is operating in first mode, near to second mode. Considering the values of duty cycle, and switching period, the total time that switch is ON is 18.33 µs, while half of resonant period is 17.82 µs. Once converter is operating in first mode, ZCS condition is obtained in D_2 and D_4.

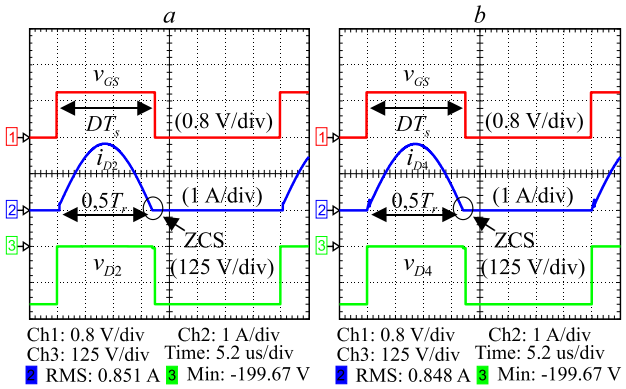

Fig. 10. Simulated waveforms of: (a) v_{GS}, i_{D2} and v_{D2}; (b) v_{GS}, i_{D4} and v_{D4}.

Fig. 11a shows waveforms of v_{GS}, i_{D1} and v_{D1}, while Fig. 11b shows v_{GS}, i_{D3} and v_{D3}, both with zoom on turn-off instant, proving the ZCS condition. The theoretical static gain, using the equation showed in Tab. I, is equal to 10.714, while in simulation it is equal to 10.679, so, V_o is equal to 399.39 V.

Fig. 12 shows waveforms of v_{GS}, i_s and v_{DS}, with zoom on turn-on instant of S_1. This zoom gives a better view of quasi-ZCS condition.

Fig. 13*a* shows waveforms of v_{GS}, i_{Lm}, i_1 and i_{Lin}. Fig. 13*b* shows voltage across L_{in} and ac component of i_{Lin}, to verify the ripple of this current. Finally, Fig. 14a shows voltages of capacitors C, C_1 and C_2, while Fig. 14b shows ac component of v_C, v_{C1} and v_{C2}, to verify the ripple of these voltages.

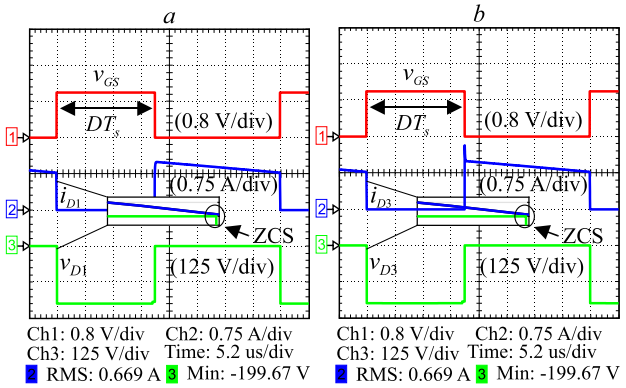

Fig. 11. Simulated waveforms of: (a) v_{GS}, i_{D1} and v_{D1}; (b) v_{GS}, i_{D3} and v_{D3}.

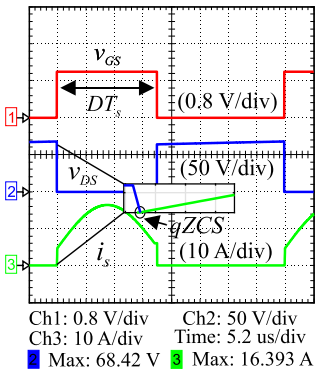

Fig. 12. Simulated waveforms of v_{GS}, v_{DS} and i_S.

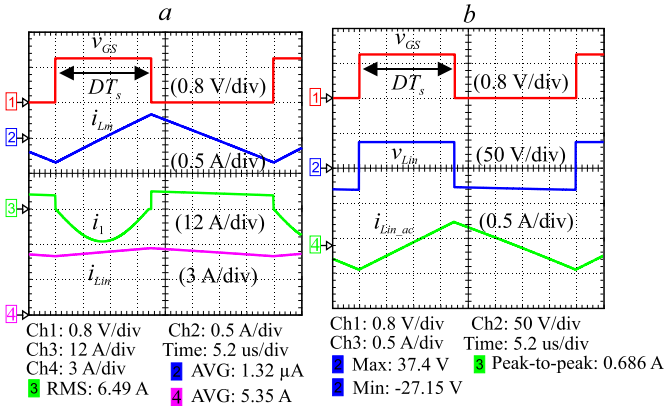

Fig. 13. Simulated waveforms of: (a) v_{GS}, i_{Lm}, i_1 and i_{Lin}; (b) v_{GS}, v_{Lm} and ripple of i_{Lin}.

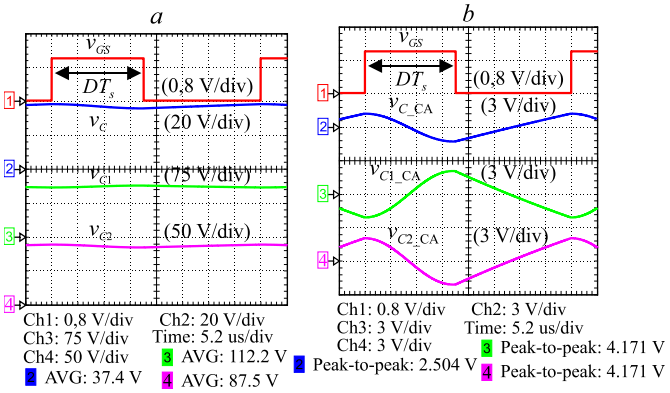

Fig. 14. Simulated waveforms of: (a) v_{GS}, v_C, v_{C1} and v_{C2}; (b) v_{GS} and ripple of v_{C1} and v_{C2}.

Table III shows a comparison of the simulated and calculated main parameters of the converter. These results show that all equations obtained in theoretical analysis have a good accuracy, with a small error, less than 1%, in comparison with simulated results.

TABLE III. COMPARISON OF CALCULATED AND SIMULATED PARAMETERS

Parameter	Calculated	Simulated	Error (%)
f_r (kHz)	28.07	28.05	0.002 (0.071)
M	10.714	10.679	0.032 (0.3)
V_{DS} (V)	66.786	68.42	1.634 (2.45)
i_{D1} (rms) (A)	0.671	0.669	0.002 (0.299)
i_{D2} (rms) (A)	0.8504	0.8509	0.0005 (0.06)
i_{D3} (rms) (A)	0.667	0.669	0.002 (0.299)
i_{D4} (rms) (A)	0.846	0.848	0.002 (0.235)
i_s (rms) (A)	8.406	8.334	0.072 (0.85)
Δi_{Lin} (A)	0.685	0.686	0.001 (0.146)
Δv_C (V)	3.73	3.723	0.007 (0.188)
Δv_{C1} (V)	4.165	4.171	0.006 (0.144)
Δv_{C2} (V)	4.165	4.171	0.006 (0.144)

V. CONCLUSIONS

This work presented a dc-dc high step-up SEPIC with a Greinacher VQ cell, used as primary stage of a MIC converter. Its derivation was made, showing that VD and VQ cells are an appropriate choice. Theoretical analysis was made, showing operating principle of all stages, besides obtaining the equations used for comparison with simulation results, including the resonant analysis considering primary capacitor.

Simulations results were performed and compared with theoretical values obtained from the equations. These results show a high static gain, without using a high turn ratio and high duty cycle. Besides that, all theoretical calculated values show a good accuracy in comparison with simulated results, proving that the analysis are correct.

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