Analysis and Design of an Interleaved Switched-Capacitor Multilevel ANPC Converter

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***Abstract*—This paper presents an interleaved switched-capacitor multilevel ANPC converter (SCANPC) for high power density applications. To demonstrate the feasibility of the idea, the analysis and design of the converter are made initially for one cell and after for the two cells interleaved configuration. In addition, it is used a power loss estimation methodology for the Gallium Nitride switches. Simulations and power loss estimations are shown for a 4kW power prototype.**

***Keywords*—Multilevel converters, high power density, *WBG* semiconductors.**

I. Introduction

With the rise of renewable energy sources and the popularization of electric vehicles, there is also an increase in demand for power converters, which are the interface between the energy source and the application. In many applications, it is important to reduce the weight and volume of the converter, making it even possible to integrate into the application [1]. With a lighter and smaller converter, it is possible to reduce the costs related to installation, maintenance, and operation. Simultaneously, efficiency is a key factor, while reducing power loss can decrease the costs related to heat dissipation [2].

Aiming the development of high power density converters, many design strategies can be adopted related to the switching frequency, voltage and current ripple specifications, semiconductor technology, and topology choice.

About the semiconductor technologies, the current trend is the use of wide-bandgap (WBG) devices, since its superior figures of merit in comparison with silicon counterparts [3]. Regarding the topology choice, it is a wide field with a great degree of freedom, and lately, multilevel topologies have been gaining prominence. One example is the concept of Flying Capacitor (FC), which had success at the Little Box Challenge (LBC) [4].

The flying capacitor is considered a classical topology, together with the Neutral Point Clamped (NPC) and the Cascaded H-bridge (CHB). As an alternative to the classical topologies, hybrid configurations are also being developed. They are a combination of classical approaches aiming to achieve some desired characteristics. A good example of hybrid configuration is the 5-Level Active Neutral Point Clamped - ANPC, which was proposed in [5] and has industrial applications due to the flexibility for voltage stabilization of the FC converter and the simplicity of a single DC-link of the NPC.

Recently, topologies using switched-capacitors (SC) are also gaining attention due to the higher power density of capacitors in comparison to inductors, at the same time that they are easier to manufacture [6].

Therefore, this paper presents the design of the topology proposed on [7], operating in an interleaved manner for high power density applications. This topology consists of a hybrid multilevel converter with SC circuit, seeking the advantages of both multilevel and SC topologies.

The paper is organized as follows: section II shows the operation of the inverter for one and two cells, section III highlights the converter design procedure, section IV shows the power loss estimation methodology, and section V shows simulations and power loss estimations for a 4kW prototype.

II. Operation of the 5L-SCANPC inverter

The operation stages for one cell of the switched-capacitor five level active neutral point clamped inverter (5L-SCANPC), presented in Fig. 1, are shown in this section [7]. Voltage stress on the switches, as well as the modulation strategy are also evaluated.

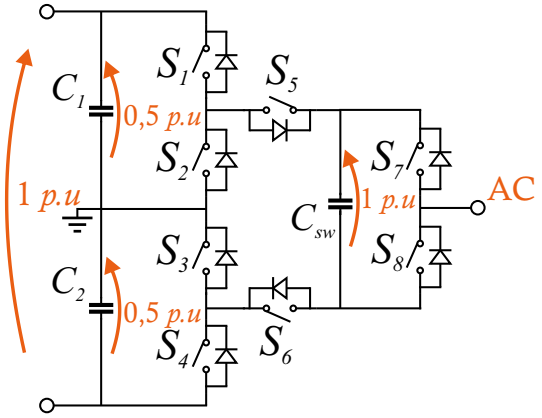

Figure 1: 5L-SCANPC Inverter.

In a similar manner to the 5L-ANPC converter, a single-phase structure of the SCANPC inverter has eight switches and three capacitors. The possible levels that can be synthesized

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are also equal, however, the input voltage of the 5L-SCANPC can be lower by half, in comparison with the conventional 5L-ANPC. This fact is related to the different voltages on capacitors, which requires another operation based on SC technique.

To better understand the operation principles of the converter, Table I shows the possible switching states as well as the voltage levels that can be synthesized. Some considerations are made to obtain these states, such as the switches voltages limited to the capacitor voltages, and turn on switches S_1, S_4, S_5 and S_6, when operating at levels $+0,5$ e $-0,5p.u$, to insert the input voltage in parallel to the SC.

Table I: 5L-SCANPC Inverter Switching States.

Switching State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	v_{AC}
A	0	1	0	1	1	0	1	0	0
B	1	0	0	1	1	1	1	0	$+0,5p.u$
C	1	0	1	0	0	1	1	0	$+1p.u$
D	1	0	1	0	0	1	0	1	0
E	1	0	0	1	1	1	0	1	$-0,5p.u$
F	0	1	0	1	1	0	0	1	$-1p.u$

From these switching states, Table II shows the voltage stress at the switches and the operation frequencies, where f_s is the switching frequency and f_r is the fundamental.

Table II: Stress over the semiconductors.

Device	Blocking Voltage	Switching Frequency
S_1	$0,5p.u$	f_s
S_2	$0,5p.u$	f_s
S_3	$0,5p.u$	f_s
S_4	$0,5p.u$	f_s
S_5	$0,5p.u$	f_s
S_6	$0,5p.u$	f_s
S_7	$1p.u$	f_r
S_8	$1p.u$	f_r

A. Modulation

The modulation strategy used in this paper is the Phase Disposition (PD), with 4 carriers, c_1, c_2, c_3, c_4, and a reference signal v_{ref}. The basic concept can be seen in Fig. 2, where the reference signal is compared with the carriers, and from that, the switching states are chosen.

B. Interleaved Operation

To reduce current stress over the passive and active elements, one can use interleaved operation, using two converter cells in parallel. By interleaving two cells, each cell can process half of the total power [8]. Beyond that, interleaved operation brings the advantage of reducing output filters, given that they can have larger current ripples, once a large portion of ripple is attenuated through modulation [9].

Therefore, this paper analyses the operation of the SCANPC converter operating with two cells in an interleaved manner, as shown in Fig. 3. To operate the converter, the modulation strategy is kept as before, with the difference that carriers of cell b are 180 degrees out of phase in relation to carriers of the cell a. With that, it is possible to attenuate the output current ripple.

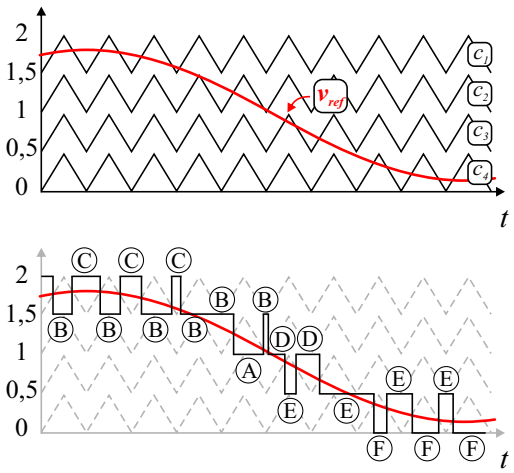

Figure 2: Modulation strategy.

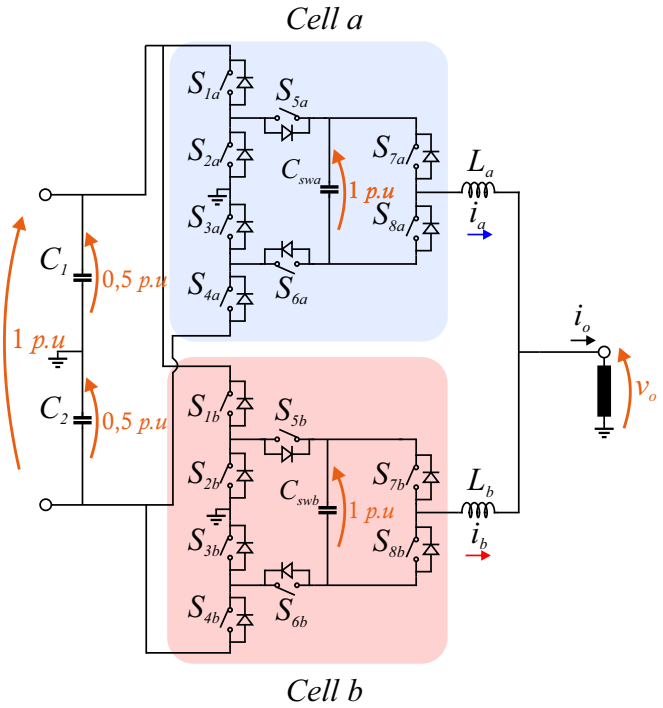

Figure 3: 5L-SCANPC interleaved with two cells.

III. Inverter Design

For the interleaved 5L-SCANPC inverter, the passive components that must be chosen are: DC link capacitors, switched-capacitors and output inductors.

Initially, the equations are made for one cell of the inverter (Fig. 1), and after they are extended for the interleaved operation.

A. DC Link Capacitors

The sizing of these elements can be made through the currents spectrum. Considering the worst case scenario, which all harmonics are in phase, the capacitor design is given through (1), where $\Delta V_{c,max}$ is the desired voltage ripple [10].

$$C \geq \frac{1}{\Delta V_{c,max}/2} \cdot \sum_{h} \frac{I_h}{2\pi f_h} \tag{1}$$

It can be seen that the harmonic components that have the higher impact for design are the ones at lower frequencies, while the ones with higher frequency, which appears due to the switching nature of the inverter, have less impact [10].

Therefore, to be able to define capacitance values, it is necessary to make the current harmonic analysis at the capacitor. This can be made using an analytical method, using double fourier series [11]. To obtain the series coefficients, a unit commutation cell is defined, which depends on the modulation strategy and the converter synthetized levels. As the modulation strategy used is the 5 level PD, the unit cell achieved is shown in Fig. 4 **a)**.

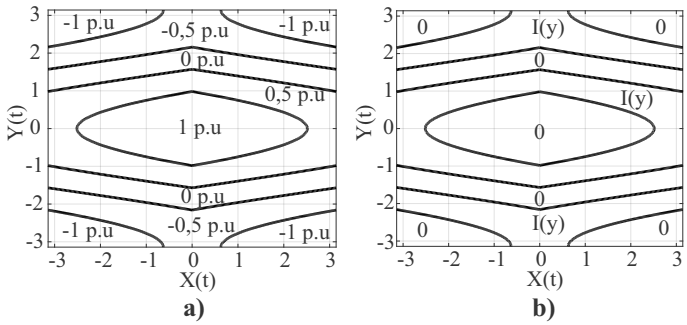

Figure 4: Unit Cells.

However, this method works with the inverter synthetized voltage levels, while it is desired to obtain the current spectrum. Then, it is necessary to have a relation between the voltage levels and the capacitor current. Through the switching states, it was seen that the DC link capacitor charges or discharges, with half the output current, when the inverter synthesizes $+0,5p.u$ and $-0,5p.u$. Thus, the capacitor current is defined as (2),after, it is possible to substitute in the unit cell, resulting in Fig. 4 **b)**.

$$I(y) = \frac{I_{o,max}}{2} \cos y \tag{2}$$

To verify the adopted strategy, it was made a comparison between the analytic analysis and the fast Fourier transform (FFT). The FFT was obtained through an ideal simulation of the 5L-SCANPC converter operating at 4kW in *PSIM*© software. The reference signal frequency was 60 Hz, and the switching frequency (f_s) 60 kHz. Table III compares the results obtained from the analytical method and FFT. The data highlights that exists good relationship between both, showing that it is possible to use the analytical method to calculate the DC link current spectrum and, after, use it for the correct component sizing.

B. Switched-Capacitor

To be able to design the SC circuit, it is necessary to analyze its switching period during the $0,5p.u$ and $1p.u$ levels. It is noted that since SC is connected in parallel with the input source during the $0,5p.u$ stages, the only limiting factor for the SC current is the Equivalent Series Resistance (ESR) of the elements in the path between the input source and the capacitor. In this case, the ESR is formed by the switches S_1, S_4, S_5, S_6 series resistance, beyond the switched capacitor (C_{sw}) ESR.

Table III: DC link Current Harmonics Analysis.

Harmonic	Frequency	*PSIM*©	Analytical	Error
1	60	7,9205	7,9360	0,195%
3	180	1,5611	1,5510	0,651%
5	300	1,2673	1,2670	0,024%
7	420	0,7194	0,7250	0,772%

Varying ESR and C_{sw} parameters, the SC current can admit three different characteristics, which are defined in [12] as: Complete Charge (CC) mode, Partial Charge (PC) mode and, No Charge (NC) mode. These modes are presented in Fig. 5.

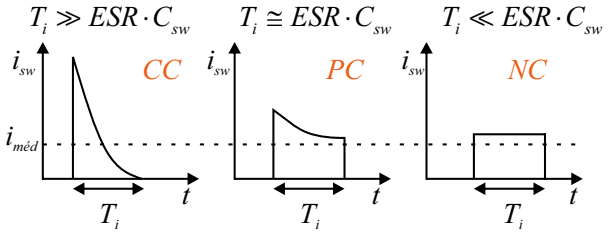

Figure 5: Switched-Capacitor charge modes.

The T_i period can be admitted as the larger SC switching interval. Therefore, the relation (3) is achieved, where the T_i period depends on the switching frequency (f_s) and the modulation index (m_a).

$$T_i = \frac{2m_a - 1}{f_s} \tag{3}$$

As shown, there is no direct equation for the SC because it depends on many factors, as the chosen charge mode, the sum of elements resistances that compose the ESR, the modulation index and the switching frequency. Thus, for an adequate design of C_{sw}, it is necessary to balance the capacitor size, switches series resistance, switching frequency and the losses from the high current peaks.

An interesting choice consists on employing the PC mode, operating with a higher switching frequency. This way, both capacitance value and series resistance can be attenuated without the incident of high current peaks at the switches, consisting in a good cost/benefit relationship [13]. However, the switching losses that arise from the rise of f_s cannot be neglected, making it mandatory to search for an equilibrium point between those two factors.

C. Output Inductor

The output inductor is responsible for the current ripple attenuation as well as to filter the high frequency output current harmonics, making it compatible with the application.

In this work, a simplified design is made for the output inductor, considering only the maximum current ripple specification. In this case the inductor can be calculated by (4) [14]:

$$L = \frac{V_{in}}{8\Delta i_L f_s} \tag{4}$$

D. Considerations for the Design with Interleaved Cells

With the use of two 5L-SCANPC cells operating in an interleaved way, the SC can have its value lower by half, once the current is splitted between the two cells. The same happens with the output inductors. As for the DC link capacitors, there are no significant changes, once the determinant design factor is the processed power and the desired voltage ripple.

The inverter specifications are shown in Table IV. Since it was used power semiconductors with GaN technology for the converter, it was considered to work with switching frequencies that enable to minimize the switched-capacitors and output inductors. For the SC design it was taken into account the series resistance of the chosen switch ($R_{ds(on)}$ = 50 mΩ/switch). The components were chosen following the described design equations, and are given in Table V.

Table IV: Inverter Specifications.

Parameter	Value
P_o	4 kW
V_{in}	400 V
V_o	220 V_{RMS}
f_r	60 Hz
f_s	60 kHz
$\Delta V_{c,max}$	5 %
ΔI_o	20 %

Table V: Inverter Components.

Component	Model	Manufacturer	Value
$S1 - S8$	TP65H050BS	Transphorm	–
C_1, C_2	380LX	Cornell Dubilier	5x470 μF
C_{swa}, C_{swb}	FE52N6J0506KB	AVX Corporation	50 μF
L_a, L_b	P11T60	MPS Industries	65 μH

IV. Power Loss Estimation Methodology for GaN Devices

When it is desired to operate with high power density, it is of great interest to estimate and identify the converter losses, making it possible to verify which components will be subjected to higher stress and probably to high temperature levels. Thus, this section shows a power loss estimation methodology for GaN devices. The LTspice© software was used to estimate the semiconductor losses, where it is possible to use the device's Spice model supplied by the manufacturer. However, as Spice simulations tend to be more precise, they are subjected to take longer simulation times and have convergence problems. Therefore, to avoid the entire converter simulation inside LTspice©, the strategy adopted consists of using the Doble Pulse Test (DPT) method with the Spice model for different currents at the switches.

Based on the DPT simulations, it is possible to plot curves that relate the turning on and off energies with the device current, so that it is possible to generate polynomials. With the polynomials, scripts that receive as inputs PSIM© simulations are implemented in Matlab© software. These scripts can detect the switching transitions and calculate the switching losses from the polynomials.

A. DPT Method

The DPT is a well-known method, which is commonly used in practice to obtain switch losses, being able to evaluate turn-on and turn-off parameters as well as the reverse recovery losses [15].

The method consists on driving a half-bridge arm with two equal semiconductors and an inductor in parallel to the high-side switch, as shown in Fig. 6 **a)**. The gate-driver signals must be programed as illustrated in Fig. 6 **b)**. With that, the inductor current rises in steps, and it is possible to commutate the low-side switch with well-known voltages and currents.

To assess the switching losses, it is necessary to measure the voltage and current over the low-side switch, and with that, compute the switching energy.

In possession of the switching energy data, for turn-on and turn-off events, it can be plotted the relationship between current and energy. Using this method, In Fig. 7 shows energy curves for the switch specified at Table V.

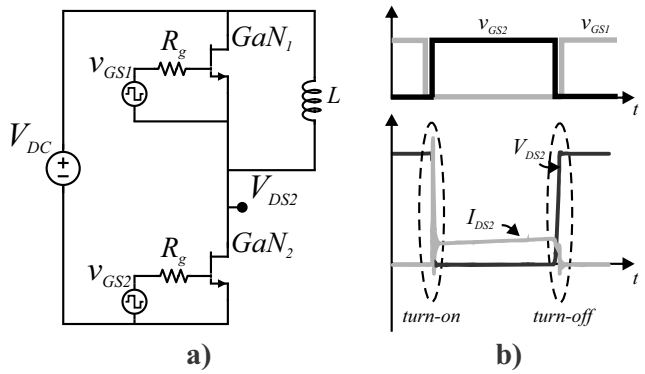

Figure 6: **a)** DPT Circuit, **b)** Gate signals, voltages and currents over the GaN_2.

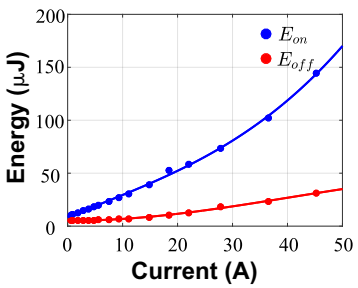

Figure 7: E_{on} and E_{off} Polynomials.

B. Power Loss Evaluation Procedure

The procedure to evaluate the losses is made with the use of Matlab© scripts. At first, PSIM© simulations are gather, with respect to components currents in the inverter. Then, a developed function detects the switch commutation events, at both turn-on and turn-off.

With the commutation points of each switch, one can obtain the switching losses by applying the points in the previously obtained polynomials. To estimate the conduction losses at the switches and passive elements, the rms current of the component is multiplied with its equivalent series resistance.

Through the described procedure, all inverter power stage losses can be estimated, making it possible to identify and quantify the possible losses that will appear in practice.

V. Simulation Results

To verify the operation of the proposed converter, simulation results obtained through PSIM© software are given.

Fig. 8 shows the output currents of cells a and b and the total output current. It is noted that, due to the interleaved operation, the currents in each cell are out of phase and, because of that, the ripple attenuation can be confirmed, as mentioned in section III, which allows operating with higher ripple specifications and, consequently, reducing the inductors physical size.

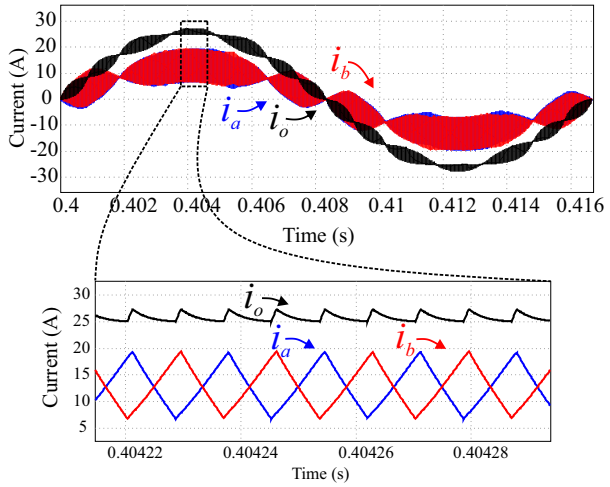

Figure 8: Inductor currents in cell a, cell b and after the filter, under maximum power.

At the DC link capacitors the voltages are kept in equilibrium, as can be seen in Fig. 9.

The switched-capacitors have regulated voltages only through the modulation strategy, as can be seen in Fig. 10. However, as shown in Fig. 11, at the switched-capacitor operation, there are high current spikes, due to the B and E switching states [7], when the switched-capacitors are in parallel to the DC link. This issue appears even with a design aiming to operate in the PC mode, as explained in section III.

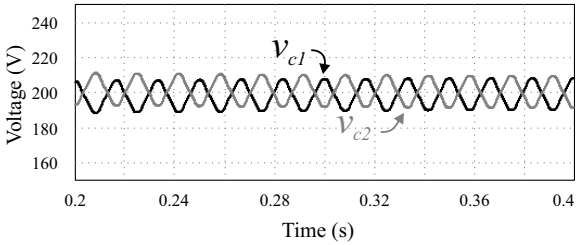

Figure 9: DC link capacitors voltage.

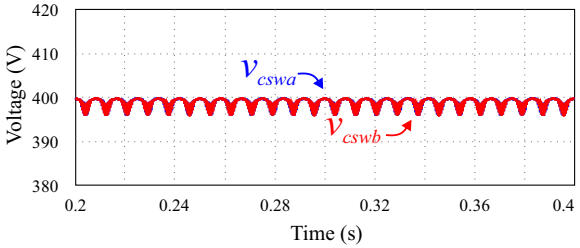

Figure 10: Switched-Capacitors voltage.

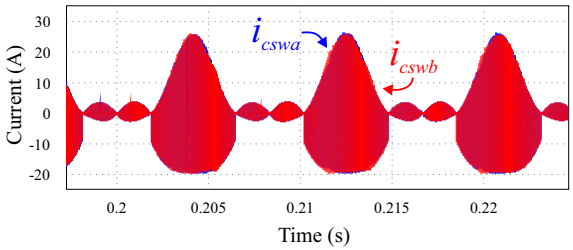

Figure 11: Switched-Capacitors currents.

A. Power Loss Estimative

To estimate the converter losses, it was applied the procedure described in section IV. Therefore, the losses per element were achieved, with the expressive losses situated in the semiconductors.

Fig. 12 shows the switches losses for one inverter cell under maximum power. One can verify that the larger losses are due to the switches conduction, mainly at the switches related to the switched-capacitor operation, S_5 and S_6. For switches S_7 and S_8, the switching losses can be neglected, once they are operated with the reference frequency (f_r) 60 H_z.

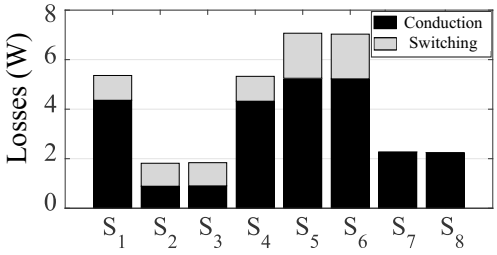

Figure 12: Power Losses in one cell, operating under maximum power.

Fig. 13 shows a theoretical efficiency curve for the presented

inverter. One can say that the curve is practically constant over a wide power range, which is a desired attribute, once it becomes possible to operate the inverter with high efficiency over different loads.

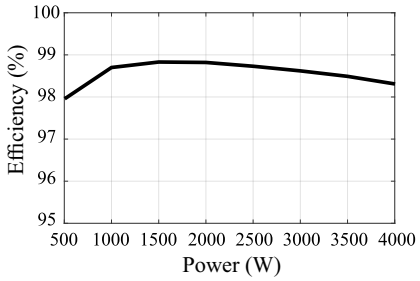

Figure 13: Estimated efficiency curve for the proposed inverter.

VI. Conclusion

This paper proposed an interleaved switched-capacitor multilevel converter aiming high power density applications. To highlight the proposal viability, it was analyzed its design, operating principle, as well as it was collected simulation data. Through the simulation data, it was possible to verify the self-regulation on switched-capacitors voltage only using modulation strategy, without the need for a complex control, the possibility to operate with smaller passive components due to the interleaved operation, and also, the possibility to use GaN semiconductors.

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References

[1] C. W. Halsted and M. D. Manjrekar, "A critique of little box challenge inverter designs: Breaking from traditional design tradeoffs," *IEEE Power Electronics Magazine*, vol. 5, no. 4, pp. 52–60, 2018.

[2] Y. Lei, C. Barth, S. Qin, W. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao, and R. C. N. Pilawa-Podgurski, "A 2-kw single-phase seven-level flying capacitor multilevel inverter with an active energy buffer," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8570–8581, 2017.

[3] S. Qin, Y. Lei, Z. Ye, D. Chou, and R. C. N. Pilawa-Podgurski, "A high-power-density power factor correction front end based on seven-level flying capacitor multilevel converter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 3, pp. 1883–1898, 2019.

[4] K. A. Kim, Y. Liu, M. Chen, and H. Chiu, "Opening the box: Survey of high power density inverter techniques from the little box challenge," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 2, pp. 131–139, 2017.

[5] P. Barbosa, P. Steimer, J. Steinke, M. Winkelnkemper, and N. Celanovic, "Active-neutral-point-clamped (anpc) multilevel converter technology," in *2005 European Conference on Power Electronics and Applications*, 2005, pp. 10 pp.–P.10.

[6] Z. Ye, Y. Lei, and R. C. N. Pilawa-Podgurski, "The cascaded resonant converter: A hybrid switched-capacitor topology with high power density and efficiency," *IEEE Transactions on Power Electronics*, vol. 35, no. 5, pp. 4946–4958, 2020.

[7] W. A. Pineda C. and C. Rech, "Modified five-level anpc inverter with output voltage boosting capability," in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, vol. 1, 2019, pp. 3355–3360.

[8] B. Lin, C. Ho, S. Wang, H. Chiang, and J. Chen, "Interleaved resonant converter with flying capacitor," in *2014 9th IEEE Conference on Industrial Electronics and Applications*, 2014, pp. 1258–1263.

[9] T. Modeer, N. Pallo, T. Foulkes, C. B. Barth, and R. C. N. Pilawa-Podgurski, "Design of a gan-based interleaved nine-level flying capacitor multilevel inverter for electric aircraft applications," *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 12 153–12 165, 2020.

[10] S. M. Sharkh, M. A. Abu-Sara, G. I. Orfanoudakis, and B. Hussain, *DC-Link Capacitor Current Numerical Calculation*, 2014, pp. 281–284.

[11] S. R. Bowes and B. M. Bird, "Novel approach to the analysis and synthesis of modulation processes in power convertors," *Proceedings of the Institution of Electrical Engineers*, vol. 122, no. 5, pp. 507–513, 1975.

[12] S. Ben-Yaakov, "Behavioral average modeling and equivalent circuit simulation of switched capacitors converters," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 632–636, 2012.

[13] M. Schramm Dall'Asta, I. Barbi, and T. B. Lazzarin, "Ac–ac hybrid boost switched-capacitor converter," *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13 115–13 125, 2020.

[14] I. Technologies, "Five-level active neutral point clamped flying capacitor inverter design based on optimos 5 150 v," shorturl.at/fjwBE, 2020, (Accessed on 01/27/2021).

[15] Z. Zhang, B. Guo, F. F. Wang, E. A. Jones, L. M. Tolbert, and B. J. Blalock, "Methodology for wide band-gap device dynamic characterization," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9307–9318, 2017.