A Comparative Study of Recent Discontinuous Modulation Techniques for Three-Phase Impedance Source Inverter

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***Abstract* — Since the Z-Source Inverter (ZSI) was first proposed in 2003, impedance source inverters (ISI) have experienced a rapid progress. This evolution is not limited to developing network topologies, but also involves their modulation and control techniques to improve their performance and efficiency from different aspects. Accordingly, discontinuous PWM (DZPWM) techniques gained substantial attension in the last few years due to their advantages compared with continuous modulation schemes. The aim of this paper is to study, analyse, and compare three recent DZPWM methods for the Z-source/quasi-Z-source inverter (qZSI). The operating principal of each DZPWM technique has been presented and analyzed. Moreover, a comparative investigation based on the inductor current ripple, voltage gain, power loss, and some other factors has been carried-out. Finally, computer simulations using MATLAB/Simulink and PLECS softwares have been performed to evaluate the presented DZPWM techniques. Such a comparative analysis helps researchers and designers to choose for their ISI modulation strategy for their application.**

Keywords—Current stress, discontinuous PWM, power loss, space vector modulation, THD , voltage gain, Z-source/ quasi Z-source inverter.

I. INTRODUCTION

The Impedance source inverter has been increasingly gaining attraction in 1) renewable energy applications such as photovoltaic [1], wind sources [2]; 2) applications such as stand-alone or grid-connected mode [3], and 3) combinations with traditional power converter such as Multilevel inverter [4], and four-legs inverter [5].

The researches have mostly focused on Z-source inverter (ZSI) or quasi-Z-source inverter (qZSI), which are the most popular simple configurations [6], [7]. As a substitute to the traditional voltage source inverter (VSI), the qZSI can be employed with increasing performance and reliability of the system by introducing the shoot-through (*ST*) state, which can boost the DC input voltage to the desired level. Fig. 1 illustrates the generic structure of a three-phase qZSI, which consists of a quasi-Z-source network (qZSN), two-level VSI, *LC* filter, and three-phase inductive load.

The performance of ISI depend on the pulse-width-modulation (PWM) method and based on the inserting of *ST* state in the conventional null states, while maintaining the active states duration for keeping the output voltage waveform [8]. Many modulation strategies were developed to control the three-phase ISIs. Meanwhile, the modulation strategies have a significant effect on the distribution of the power losses, current ripple, voltage/current stresses, as well as output power quality.

Numerous modulation methods can be exploited to control the three-phase qZSI [8]. According to the method used to create the *ST* state, some structures can be divided into two groups, i) three-phase leg ST state such as, simple boost control (SBC), maximum boost control (MBC), maximum constant boost control (MCBC). In this case, the *ST* state is created through the three-phase legs simultaneously. ii) single-phase leg *ST* likes the space vector modulation (SVM) strategy, in this kind, the *ST* state is obtained through only one phase-leg. In the other side, the above-mentioned categories (i and ii) are used in either continuous or discontinuous modulation schemes (CZPWM of DZPWM), this latter (DZPWM) is considered to be the best in terms of reducing the power losses [9].

Several literature reviews explain the CZPWM strategies with both categories of *ST*. In [10] Ellabban *et al.* compared the four sine-wave pulse width modulation SPWMs and modified space vector modulation with four-time for *ST* duration (ZSVM4) in aspects of the inverter voltage gain, voltage stress, power loss and voltage/current harmonics. In [11] Yushan *et al.* compared the four ZSVMx (x = 6, 4, 2 or1) focusing on the total switching device power (SDP) to calculate both the voltage and current stresses, and the relation of inductor current ripple with *ST* duty ratio. In [12], Ping Liu *et al.* investigated the thermal performance and output power quality of different CZPWM methods.

DZPWM is a method of reducing power losses in ISI. It decreases the number of switching transitions of the inverter bridge by switching the only two-phase legs of the three-phase legs. Therefore, in the aim to reduce the power losses, many recent DZPWM techniques have been proposed [13]-[18].

The objective of this paper is to present a comparative study of the DZPWM techniques. Therefore, three DZPWM strategies and another CZPWM for the three-phase qZSI have been studied and analyzed. Simulations based on MATLAB/Simulink and PLECS have been carried out to evaluate the presented modulation techniques in terms of DC-link voltage, inductive current ripples, power losses, and the output voltage/current THD.

The organization of the paper is as follows. In Section II, the operational principle in qZSI is explained. The detailed reviews of the DZPWM strategies of the qZSI are illustrated in section III. In Section IV, the performance evaluation of the presented PWM techniques are provided. The simulation results are presented and discussed in Section V. Finally, in section VI, a conclusion of this work is provided.

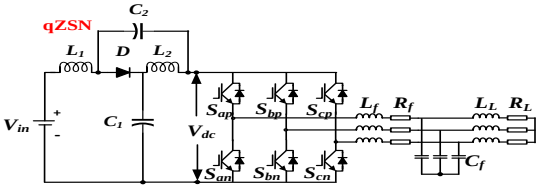

Fig. 1. Configuration of the three-phase qZSI with *LC* filter

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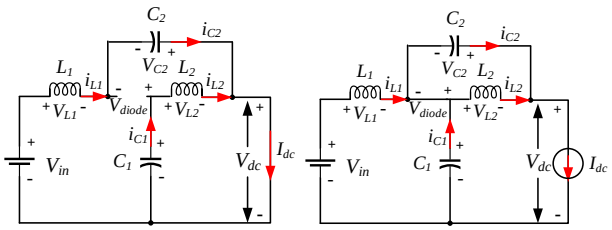


(a) (b)

Fig. 2. Operating modes of the qZSI: (a) shoot-through state and (b) active state.

II. Operational Principle of The qZSI

The configuration system of a three-phase qZSI is shown in Fig. 1. The quasi-Z-source network (qZSN) is a combination of two inductors L_1 and L_2, two capacitors C_1 and C_2 and one reverse diode, where these elements are inserted between the input DC source (V_{in}) and the employed inverter. The qZSI can buck/boost the DC source voltage without any additional DC-DC converter by turning one, two or three legs at the same time, called as the shoot-through state (*ST*), which is unachievable in the traditional (VSIs). Using the *LC* filter at the AC side, the qZSI can operate with different AC loads or can be connected to the grids. Fig. 2(a), (b) shows the equivalent circuit of the qZSI, which can be divided in two working modes. The first mode is shoot-through state (*ST*), the upper and lower switches in the same phase-leg are turned on simultaneously, in this case, the DC input power and the capacitors C_1, C_2 transfer the energy to the inductors L_1 and L_2 at the same time, the diode is blocked because of negative voltage (see Fig.2(a)). The second mode is active state (*ACT*), as shown in Fig. 2(b), the diode *D* is turned-*ON*, the DC input power and the inductors deliver the energy to the AC loads and charge the capacitors. Referring to [6], during the steady-state, the average capacitor voltages V_{C1} and V_{C2} can be obtained as, respectively

$$V_{C_1} = \frac{1-D_{ST}}{1-2D_{ST}}V_{in}, \quad V_{C_2} = \frac{D_{ST}}{1-2D_{ST}}V_{in} \tag{1}$$

The peak DC-link voltage is given by

$$V_{DC} = V_{C_1} + V_{C_2} = \frac{1}{1-2D_{ST}}V_{in} = B.V_{in} \tag{2}$$

Where *B* is defined as the boost factor, $D_{ST} = T_{ST}/T_S$ is the *ST* duty ratio, T_{ST} is the total *ST* duration, and T_S is the switching period.

III. Modulation Techniques: A Review

A. Maximum boost discontinuous SV

In order to increase the efficiency of the three-phase qZSI by reducing the switching losses, the maximum boost discontinuous space vector strategy (MBDSV) with the single-phase leg ST is applied to optimize the switching losses and improving the reliability of power electronics devices. The periodical exploitation in *ST* state for switches is the objective of the MBDSV method [13].

1) Modulation technique

The MBDSV modulation strategy is achieved by modifying the conventional sinusoidal signals and using only three reference signals (V_a, V_b, V_c). The reference waveforms are compared with the carrier-wave to produce the gate signals for the qZSI switches. Fig. 3 shows the operation principle of the MBDSV, taking phase *a* as an example, the MBDSV principle is explained as follows:

- S_{ap} is maintained *ON* when V_a is greater than the carrier wave and S_{an} is maintained *ON* when V_a is smaller than the carrier wave (see Fig. 4).
- In order to achieve the *ST* state, S_{an} is maintained in *ON* state when V_a is smaller than the carrier wave and smallest than V_b and V_c references, as shown in Fig. 4.

Where S_{ap} is the upper power switch and S_{an} is the lower power switch of phase a.

As a consequence of utilizing the MBDSV modulation strategy, the following merits are gained:

1) Reduced number of switch commutations (one-leg in the qZSI is clamped one-third of the fundamental period) compared to the conventional modulation strategies.
2) Single phase-leg *ST*.
3) Only the upper switches commutate to and from the *ST* state.

While, the following demerits exist:

1) *ST* duty cycle is variable
2) Low-frequency element is induced in the capacitor voltages and inductor currents, where, to reduce this effect, a large inductance and capacitance are required.

2) Mathematical derivation

a) ST duty ratio and voltage gain

The *ST* duty cycle (d_{ST}) is variable during the fundamental period, it can be expressed as:

$$d_{ST} = 1 - \frac{\sqrt{3}}{2}M.\sin(\omega t + \frac{\pi}{6}) \tag{3}$$

Where *M* is the modulation index and *w* is the fundamental angular frequency. The average value of d_{ST} for $\pi/6 \le wt \le \pi/2$ can be expressed as follow:

$$D_{ST} = 1 - \frac{3\sqrt{3}M}{2\pi} \tag{4}$$

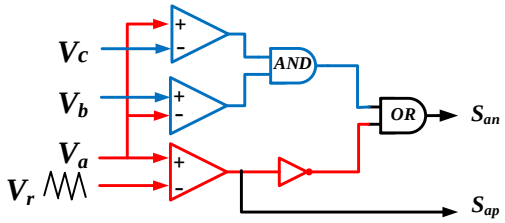


Fig. 3. Flowchart of the MBDSV for phase-a

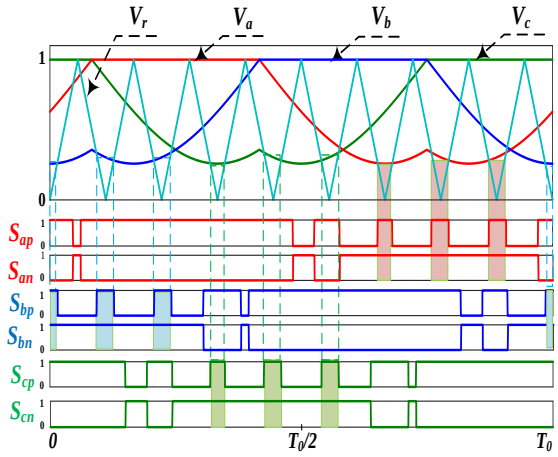


Fig. 4 Switching signal generation for the MBDSV technique (M = 0.7, f_S = 450 Hz).

The average capacitor voltages are given by

$$V_{C_1} = \frac{3\sqrt{3}M}{6\sqrt{3}M-2\pi}V_{in}, \; V_{C_2} = \frac{2\pi-3\sqrt{3}M}{-2\pi+6\sqrt{3}M}V_{in} \tag{5}$$

The peak DC-link voltage is expressed as

$$V_{DC} = \frac{1}{1-2D_{ST}}V_{in} = \frac{\pi}{3\sqrt{3}M-\pi}V_{in} \tag{6}$$

b) Current stress

The current that flows through the qZSI power switches is characterized by two-time intervals, *ACT* state current (i_{ACT}) and *ST* state current (i_{ST}) [14]. The peak currents stress i_{ACT}, i_{ST} during the *ACT* state and *ST* state can be expressed as:

$$i_{ACT}=\begin{cases} i_{ph} & ,S_{ap} \\ 0 & ,S_{an} \end{cases}, \qquad i_{ST}=\begin{cases} 2i_L & ,S_{ap} \\ 2i_L+i_{ph} & ,S_{an} \end{cases} \tag{7}$$

Where, i_L is the peak value of the inductor current and can be expressed as:

$$i_L = I_L + \frac{\Delta i_L}{2} = \frac{\hat{V}_{ph}\hat{i}_{ph}\cos\varphi}{2V_{in}} + \frac{V_{C_2}D_{ST}}{4Lf_S} \tag{8}$$

In which I_L is the DC element of the inductor current, $\hat{\imath}_{ph}$ is the maximum value of the AC output current, $\cos\varphi$ is power factor, f_S is the switching frequency.

B. Discontinuous PWM

In order to solve the limitations defined in the interrelationship of the D_{ST} and M in the traditional modulation techniques, a three-phase leg *ST* discontinuous PWM technique for ZSI (DCPWM) has been introduced, the DCPWM technique based on the separation between the *ST* duty ratio and M, which maintain M at maximum value. The both of *ST* duty cycle and boosting factor based on a new parameter called (K) [15], [16].

1) Modulation technique

The DCPWM technique is synthesized based on the three-phase reference signals V_a, V_b, and V_c (see Fig. 6), which can be calculated using, i) instantaneous average value of the maximum and minimum sinusoidal reference voltages (V_{ao}, V_{bo}, V_{co}) and ii) zero-sequence voltage component (V_{zs}). The following equations (9), (10), and (11) show how the reference signals V_a, V_b, and V_c are obtained.

The reference sinusoidal voltages V_{ao}, V_{bo}, and V_{co} are given as:

$$\begin{cases} V_{ao}=M.\sin(\omega t) \\ V_{bo}=M.\sin(\omega t-2\pi/3) \\ V_{co}=M.\sin(\omega t+2\pi/3) \end{cases} \tag{9}$$

The zero-sequence voltage component (V_{zs}) can be calculated as follows:

$$\begin{aligned} V_{zs} = &\frac{1}{2}\left(1-\text{sgn}\left(\frac{d}{dt}\max(V_{ao},V_{bo},V_{co})\right)\right)\max(V_{ao},V_{bo},V_{co}) \\ &+\frac{1}{2}\left(1-\text{sgn}\left(\frac{d}{dt}\min(V_{ao},V_{bo},V_{co})\right)\right)\min(V_{ao},V_{bo},V_{co}) \end{aligned} \tag{10}$$

Where: "*sgn*" is the sign function, which yields "1" for positive values and "−1" for negative values.

Based on (9) and (10), the modulating reference signals can be expressed as:

$$\begin{cases} V_a=V_{ao}-V_{zs} \\ V_b=V_{bo}-V_{zs} \\ V_c=V_{co}-V_{zs} \end{cases} \tag{11}$$

The two *ST* envelope signals V_p and V_n are needed to create the *ST* state, which can be calculated as given in (12).

$$\begin{aligned} V_p &= \max(V_a,V_b,V_c)+K(1-ceil(\max(V_a,V_b,V_c)) \\ V_n &= \min(V_a,V_b,V_c)-K(1+floor(\min(V_a,V_b,V_c)) \end{aligned} \tag{12}$$

Where: the DC-offset K between (0 and 0.5) (see Fig. 6), "*ceil*" and "*floor*" functions are the nearest higher and lower integer of a real number, respectively.

The DCPWM technique is based on the changing of the K at maximum value M to obtain the desired voltage boost. Usually, the D_{ST} increases as the value of K decreases and the boosting factor also increases. In this case, the M is fixed at its highest possible value ($M=1/\sqrt{3}$). To provide the envelope signals V_p and V_n, the zero periods in the signals of max (V_a, V_b, V_c) and min (V_a, V_b, V_c) should be changed by (K) and ($-K$), respectively. Fig.5 shows the flowchart of the DCPWM technique for phase-a, where the modulation principale method is explained as follows:

- S_{ap}, S_{bp}, S_{cp} are switched *ON* when V_a, V_b, V_c are greater than the carrier wave, while S_{an}, S_{bn}, S_{cn} are turned *ON* when V_a, V_b, V_c are smaller than the carrier wave V_r (see Fig. 6).
- To obtain the ST states, S_{ap}, S_{bp}, S_{cp} are switched in *ON* state when the envelope wave V_p is smaller than the carrier signal V_r, and S_{an}, S_{bn}, S_{cn} are switched *ON* when the envelope signal V_n is higher than the carrier wave, as shown in Fig. 6.

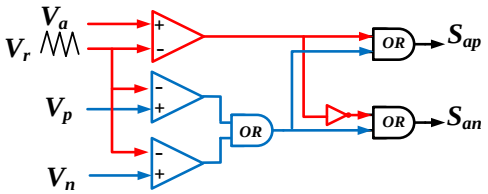


Fig. 5 Flowchart of the DCPWM for phase-a

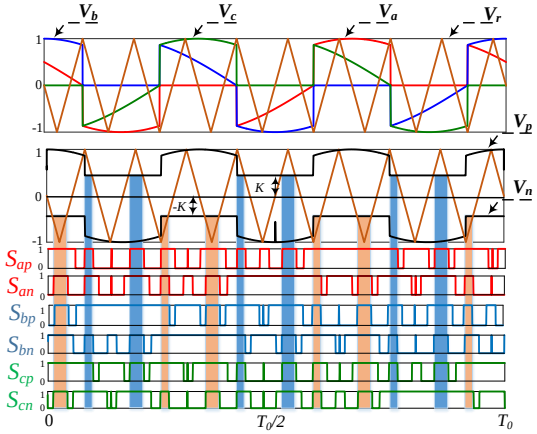


Fig. 6 Switching signal generation for the DCPWM technique ($M=1/\sqrt{3}$, f_S= 450Hz, K=0.4)

As a result of using the DCPWM technique, the following benefits are obtained:

1) The relation between the *ST* duty ratio and M is decoupled, which M is kept at its maximum value.
2) Obtaining high voltage gains without decreasing the modulation index value, this merit enhances the quality of the output voltage.
3) Elimination of the low-frequency element in the inductor current and reduce the voltage drop in DC-link voltage.
4) Reduces the power loss in each switch by locking *ON* state during $\pi/3$ per cycle of the fundamental period.

On the other hand, the following demerits exist:

1) Two auxiliary signals are applied to generate the *ST* state.
2) Low maximum modulation index value ($M=1/\sqrt{3}$) leads to high voltage stress and deteriorates the THD.

2) Mathematical derivation

a) ST duty ratio and voltage gain

As shown in Fig. 6, the *ST* state is repeated periodically every $\pi/3$. The average *ST* duty ratio can be calculated as follows:

$$D_{ST} = \frac{1}{\pi/3}\int_{\pi/6}^{\pi/2}\frac{T_{ST}}{T_S}d\theta = \frac{\pi(2-K)-3\sqrt{3}M}{2\pi} \tag{13}$$

The average capacitors voltage are given by

$$V_{C1} = \frac{K\pi+3\sqrt{3}M}{2\pi(K-1)+6\sqrt{3}M}V_{in}, V_{C2} = \frac{\pi(2-K)-3\sqrt{3}M}{2\pi(K-1)+6\sqrt{3}M}V_{in} \tag{14}$$

The peak DC-link voltage across the inverter bridge is

$$V_{DC} = \frac{1}{1-2D_{ST}}V_{in} = \frac{\pi}{\pi(K-1)+3\sqrt{3}M}V_{in} \tag{15}$$

b) Current stress

In the DCPWM strategy, the three-phase legs are turned in the *ST* state simultaneously. In the *ACT* state, the current that flows across each switch is the same as in the conventional VSI, where the output phase current $i_{ACT} = i_{ph}$. During the *ST* state, the current that flows through the power switches is

$$i_{ST} = \frac{2i_L}{3} + \frac{i_{ph}}{2} \tag{16}$$

C. Discontinuous Space vector modulation

The conventional SVM theory has been changed to be useful for the ISI to benefits the low harmonics and high DC-link voltage utilization [11]. The single-phase leg *ST* discontinuous SVM (DZSVM2) is utilized for three-phase ISI, because it offers a reduced the switching sequences, which reduces the switching losses based on the elimination of one zero state [17]. This means that, one leg of the inverter is locked to the positive or negative DC value, while the other legs are turned during the switching period.

Moreover, the *ST* duration is inserted four-times equally in each switching period, which used one phase leg at a time by embedding every two switches in the switching period. In general, the switching number is reduced. This feature is especially essential in high power medium voltage drive systems, a little savings in switching losses means a large part of total energy saving and, as a result, increased reliability and efficiency of the drive system [18].

1) Modulation technique

The conventional SVM method for the three-phase ZSI has six active vectors (V_1 to V_6), two zero vectors (V_0, V_7) and one ST vector (V_{ST}), which divide the hexagon into six sectors. In the DZSVM2 method, the second and the fifth sectors are divided into two sub-sectors and are set to 30°, which increases the number of sectors to eight. The DZSVM2 strategy has the capability of controlling the ISI at a higher modulation index, which leads to improved THD of the output current. Fig. 7 shows the basic voltage space vectors. In each sector/sub-sector, the suitable switching times of the two adjacent vectors contribute to the reference voltage V_{ref} with *ST* vector, which can be written as

$$V_{ref} = \frac{T_1}{T_S}V_i + \frac{T_2}{T_S}V_{i+1} + \frac{T_0 - T_{ST}}{T_S}V_0 + \frac{T_{ST}}{T_S}V_{ST} \tag{17}$$

where T_s is the switching period, T_1 and T_2 are the application times of the adjacent active vectors V_i and V_{i+1}, respectivety. T_0 is the time of the zero vector, which contains the conventional zero vector V_0 and V_{ST}. In all sectors, the application times are defined as:

$$\begin{cases} T_1 = M.T_S.\sin(\pi/3 - \theta + (i-1)\pi/3) \\ T_2 = M.T_S.\sin(\theta - (i-1)\pi/3) \\ T_0 = T_S - T_1 - T_2 \end{cases} \tag{18}$$

Where '*i*' indicates the sector ranges from 1 to 6, the two sub-sector in the second and fifth sector (i = 2 and 5), respectively. θ is the inclined angle of the reference vector voltage V_{ref}, where the modulation index defined as $(M=\sqrt{3}V_{ref}/V_{DC})$.

The objective of the DZSVM2 method is achieved by eliminating one switching transition in each sector by using only one zero vector (either V_0 or V_7), as well as the proper selection of the distribution of the *ST* state. Due to this elimination, the switching losses can be reduced. In the DZSVM2 strategy, four ST states are embedded inside each switching cycle with a duration of $T_{sh}/4$ without changing the active states (see Fig. 8).

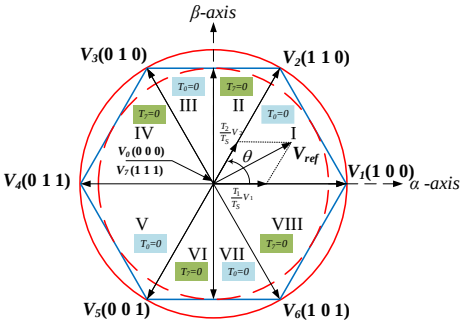


Fig. 7. Voltage space vector for DZSVM2

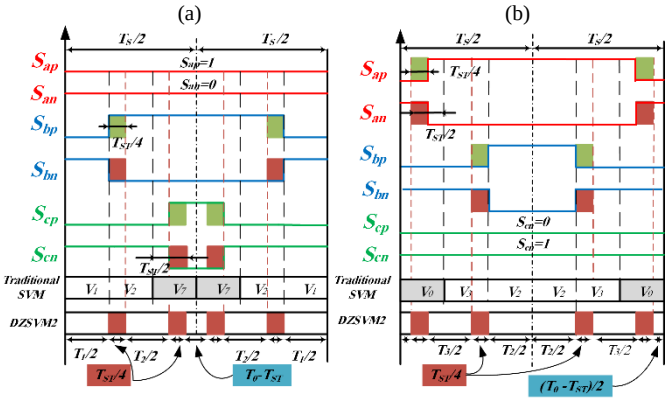


Fig. 8. Switching sequence for the DZSVM2 technique for, (a) the first sector (0< θ <60°), (b) the second sector (60°< θ <90°).

The switching sequences for sector 1 (0°–60°) and sector 2 (60°–90°) as shown in Fig. 8(a), (b), respectively. In the first sector, the upper switch S_{ap} is maintained in *ON* state and the lower switch S_{an} is maintained in *OFF* state. After that, in the second sector, S_{cp} is maintained in *OFF* state and S_{cn} is maintained in *ON* state.This procedure is repeated in all sectors for the other legs. The DZSVM2 technique guarantees the reduction of switching power losses by maintaining one leg in each sector locked.

The DZSVM2 strategy can offer the following merits:

1) Reduced high-frequency component of inductive current and capacitor voltage conforming with the same *ST* duration during the switching cycle;
2) Single commutation in *ST* state;
3) Reduce the switch commutations due to the elimination of one zero state in all sectors.

2) Mathematical derivation

a) Voltage gain

From **(**18), during one cycle, the value of the zero state duty ratio T_0/T_S varies, and every $\pi/3$ keeps repeating periodically. Therefore, in one control period, the average zero state duty ratio can be calculated as:

$$\frac{T_0}{T_S} = \frac{1}{\pi/3}\int_0^{\pi/3}\left[1 - \frac{\sqrt{3}}{2}M.\sin(\pi/3+\theta)\right] = 1 - \frac{3\sqrt{3}}{2\pi}M \tag{19}$$

The maximum *ST* time interval can exploit all the zero state duration with $(T_0/4\text{-}T_{ST}/4)$ should be greater than zero, the *ST* duty cycle can be obtained as:

$$D_{ST} = 1 - \frac{3\sqrt{3}}{2\pi}M \tag{20}$$

In the steady-state, the average capacitor voltages is given by

$$V_{C_1} = \frac{3\sqrt{3}M}{6\sqrt{3}M - 2\pi}V_{in}, \quad V_{C_2} = \frac{2\pi - 3\sqrt{3}M}{-2\pi + 6\sqrt{3}M}V_{in} \tag{21}$$

The peak DC-link voltage is given by

$$V_{DC} = \frac{1}{1-2D_{ST}}V_{in} = \frac{\pi}{3\sqrt{3}M - \pi}V_{in} \tag{22}$$

b) Current stress

Moreover, the one-phase leg is turned *ON* in the *ST* state, where the *ST* current is based on the phase current polarity and inductor current, which can be presented as

$$i_{ST}=\begin{cases}2i_L & i_{ph}\geq 0\\ 2i_L+i_{ph} & i_{ph}\leq 0\end{cases} \quad (23)$$

IV. Evaluation of the Modulations Techniques

To highlight and explain the merits obtained as a result of utilizing the DZPWM strategies, a comparative analysis is summarized in Table I. In order to evaluate the performance of all strategies, they are compared through a CZPWM technique with one leg *ST*. The modified SVM (ZSVM4) proposed in [11] is selected for this comparison. Additionally, in all strategies, the maximum voltage equals the DC-link peak voltage across the switches (see Fig. 2(b)). The voltage stress on the switch then is $V_S = BV_{in}$ and the voltage stress versus the voltage gain can therefore be calculated from Table I.

Fig. 9(a), (b) shows the maximum voltage gain against the modulation index and the normalized voltage stress ratio versus the voltage gain for the presented PWM techniques. At the same modulation index, the MBDSV control makes the most use of the traditional zero states, so it has the maximum modulation index with high voltage gain and the low voltage stress across the inverter bridge compared with ZSVM4, with the same voltage gain (see Table I and Fig. 9).

In the DCPWM, the value of K is set to 0.5. It can be noticed from Fig. 9(a) that the maximum voltage gain of DCPWM is kept constant and at lowest value. Moreover, at the same DC input voltage, the DCPWM has lower voltage stress on the switch and the same voltage gain (see Fig. 9(b)). The ZSVM4 has a distributed uniformly *ST* state, so it does not contain low-frequency ripples associated with output frequency, but its voltage stress across the inverter bridge is the largest with a given voltage gain.

V. Results and Discussions

A. Simulation Results

In order to test the performance of the DZPWM strategies and verify the reported analysis, the reviewed modulation schemes have been implemented through computer simulations using MATLAB/Simulink.

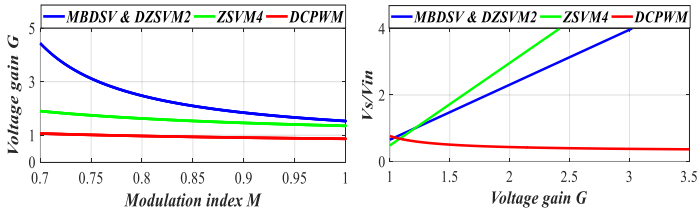
The output of the qZSI is connected to the three-phase inductive load using an LC filter, the system parameters are summarized in Table III. The modulation indexes M and the input voltage V_{in} of the presented modulation strategies have been adapted to achieve the same output *RMS* phase voltage of 170V.

TABLE I
COMPARISON AMONG OF THE MODULATION STRATEGIES

Modulation	MBDSV	DZSVM2	ZSVM4 [11]	DCPWM
ST Type	Single-phase leg ST state			Three-phase leg ST state
N.of reference	3	6	6	5
N.of ST pulses	1	4	6	2
N. of commutations	6	8	12	20
ST duty ratio variation	Variable	Constant	Constant	Variable
G_{max}	$\frac{\pi M}{3\sqrt{3M-\pi}}$	$\frac{\pi M}{3\sqrt{3M-\pi}}$	$\frac{4\pi M}{9\sqrt{3M-2\pi}}$	$\frac{2\pi M}{6\sqrt{3M-\pi}}$
Voltage stress V_S/V_{in}	$\frac{3\sqrt{3}G}{\pi}-1$	$\frac{3\sqrt{3}G}{\pi}-1$	$\frac{9\sqrt{3}G}{2\pi}-2$	$\frac{\pi G}{6\sqrt{3G-2\pi}}$

TABLE II
SUMMARY OF SIMULATED RESULTS IN DIFFERENT STRATEGIES

Modulation	MBDSV		DZSVM2	ZSVM4 [11]	DCPWM
Peak ST current [A]	S_{ap}	S_{an}	26.03	26.29	18.84
	34.07	40.36			
Low frequency Inductive current ripple Δi_L	15		8	9.5	17.5
THD output current %	1.81		0.72	2.1	4.27



(a) (b)

Fig. 9. Comparison between the presented PWM techniques for the qZSI, (a) voltage gain versus the modulation index, (b) voltage stress ratio versus the inverter bridge against the voltage gain.

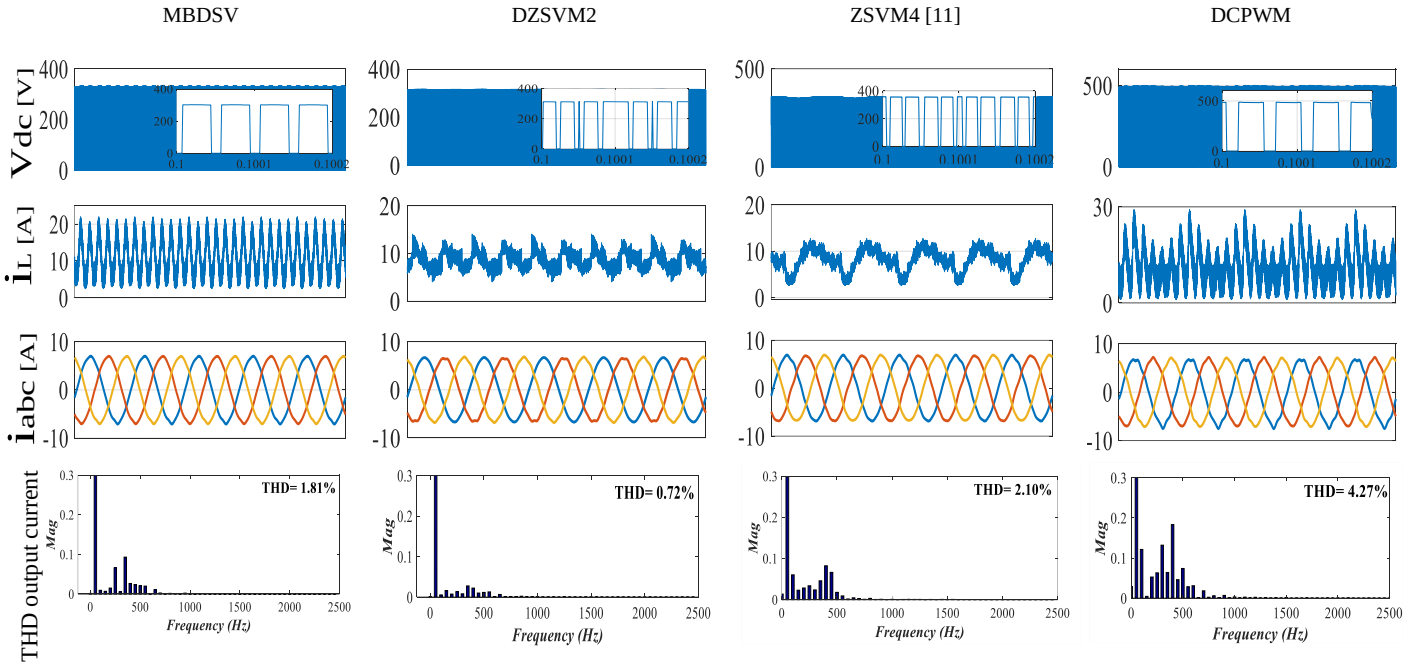
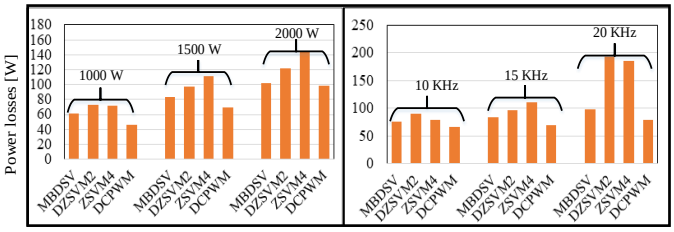


Fig. 10. Simulation results of three-phase qZSI using MBDSV, DZSVM2, ZSVM4, and DCPWM modulation strategies.

TABLE III
SYSTEM SPECIFICATION

Circuit parametres	Value
qZSI network $C_{1,2}$, $L_{1,2}$	2,5 mF, 1mH
Filter inductance *Lf*, *rf*	3mH, 0.1 Ohm
Filter capacitor C_f	50 µF
inductive load *L*, *R*	12mH, 20 Ohm
Switching frequency f_S	10 KHz
Input DC voltage	160V~180V



(a) (b)

Fig. 11. Power losses of the qZSI using the presented modulation techniques: (a) Versus different output power rates (f_s= 10 kHz), (b) Versus switching frequency (output power is set 1500W).

Fig. 10. demonstrates the simulation results of the obtained DC-link voltage (V_{dc}), the inductor current (i_{L1}), and the three-phase output current (i_{abc}). The peak current through the switch and low frequency inductive current ripple Δi_L for each modulation strategy are listed in Table II.

As it can be seen from Table II, the DZSVM2 has the lowest inductor current ripple (Δi_L=8A) due to the equal distribution of the *ST* states, while the DCPWM suffers from the largest value of the inductor current ripple at low-frequency (Δi_L=17.5A) as confirmed by Fig.10. From Table II, the MBDSV, DZSVM2 and ZSVM4 have the high peak current though the switches due to the single-phase *ST*. Meanwhile, the DCPWM used the three-phase *ST* as it provided the lowest value (18.84 A).

To obtain the same output RMS phase voltage, a lower DC-link is used in the MBDSV, DZSVM2 and ZSVM4, while a higher DC-link utilized in the DCPWM strategy, which leads to high voltage stresses applied on the switches according to the used D_{ST} value (see Fig. 10). It is clearly shown in Fig.10, that the MBDSV, DZSVM2 and ZSVM4 methods provide low THD values of the output currents compared to the DCPWM technique.

B. Power loss calculation

In order to evaluate the impact of all modulation strategies on the inverter efficiency, the power losses in the converter switches for the qZSI are measured using PLECS and are shown in Fig. 11.

The discrete IGBT with antiparall diode F4-50R06W1E3 model is used. It can also be noticed that among the modulation strategies mentioned, the DCPWM and MBDSV provide the smallest total power loss than the others, while the ZSVM4 has the highest power loss under different output power values.

Additionally, for the different switching frequencies, the ZSVM4 and DZSVM2 suffer from higher power losses compared to the other modulations, while the DCPWM presents the lowest power losses (see Fig. 11).

VI. CONCLUSION

In this paper, three discontinuous modulation strategies (MBDSV, DZSVM2, DCPWM) have been presented and analyzed for the three-phase qZSI. The switching sequences, the maximum voltage gain, and the maximum voltage stress across the switch of the presented methods were investigated. The comparative study was done to evaluate the presented DZPWM as well as the continuous ZSVM4, in terms of DC-link utilization, inductive current ripple, current stresses, power losses, THD of output current.

The following remarks can be derived:

- The MBDSV and DZSVM2 have a higher voltage gain with a lower voltage stress in the switch than the DCPWM;
- The DCPWM presents the lowest current stresses due to the three-phase legs *ST* compared to the MBDSV, DZSVM2, ZSVM4;
- The DZSVM2, ZSVM4 led to lower inductor current ripples than the MBDSV and DCPWM;
- The MBDSV, DZSVM2, ZSVM4 presented lower harmonics compared to the DCPWM due to the limitation of the modulation index;
- The DCPWM presents lower power losses with increasing the switching frequency and output power levels.

VII. REFERENCE

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