Test-Driven Design of Modulation Approaches for Grid-Tied Inverters

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***Abstract*—The paper presents an approach to evaluate modulation techniques in a Grid-Tied two-level Inverter using Test-Driven Design (TDD). It presents a set of tests that collect and calculate performance, harmonic, and power metrics of the inverter, based on IEEE Standards. The results are obtained by a Hardware-In-the-Loop (HIL) simulation and the TDD is applied with the pytest framework and Python language. The results of TDD procedure offer a structure to analyze different characteristics of the modulation approaches considering the Half-Bridge converter and the Space Vector, Sinusoidal and Carrier-Based algorithms.**

***Keywords* – Modulation, Grid-Tied Inverters, Test-Driven Design**

I. Introduction

The quick insertion of distributed generated systems in market create a demand for the power electronics industry. User generating and consuming from these resources brought new challenges for the engineering and engineers to build more reliable, safe, high-fidelity, and durable products in a shorter period of time, forcing guidelines and grid codes in order to manufacture and sell inverters.

In that scenario, it became necessary to establish experiments for certification and validation of power converters, with reduced lead times. FPGA-based Hardware-In-the-Loop (HIL) are one of the most advanced simulation tools for power electronic devices, helping engineering companies to develop their products in a shorter time, compared with solutions running only in processors of general purposes, such as the personal computers (Processor-In-the-Loop) [1], [2].

Increase continuous integration, delivery and time-to-market are possible with these new technologies to apply automation of tests as a feature for the development process [3]–[5]. With test automation, you can choose a list of one or more tests to evaluate and certify controllers, PV systems, converters, passive and active filters in several operation scenarios. Some of these tests are very difficult to perform using Supervisory Control and Data Acquisition (SCADA) systems or in bench experiments.

The Test-Driven Design (TDD) presented in [5]–[7] is a methodology based on Test-Driven Development used in test automation for verification and validation into the software process. Beck is one of the first to discuss and document the methodology [8] also explored by several authors [9]–[11] and popularized by the software Extreme Programming (XP) community. As a package, Test-Driven Development philosophy is presented as a framework in Java, C#, and Python working accordingly to the structures displayed in the book xUnit Test Patterns [12].

The design analysis using TDD is a new approach for power electronics. To deploy Grid-Tied Inverter can apply to the controllers a wide range of adversities, like disturbances, faults, and changes to the grid impedance. Tests were developed to compute the system metrics, measuring and calculating these conditions during the TDD procedure.

The computation of these metrics are done offline, after simulation, using the array package provided on Python, called Numpy. Numpy assures results with fast and high-resolution precision provided by the HIL simulation [13].

The tests for Grid-Tied Inverters introduced to evaluate modulation algorithms will be presented in Sections II and III, the figures of merit considering grid codes and IEEE Standard approaches will be presented in Section IV, and the summarization of TDD results and discussion of the approach will be presented in Section V and VI.

II. Test-Driven Design

The first testing approach known by the development community is the Waterfall method presented by Royce [14]. In this model, the test is placed to develop and evaluated at the end of the workflow, as a highlight in Fig. 1.

The method is a difficult way to proceed, where the product specification cannot be verified until the end of the developing process. After Waterfall method, the literature shows testing models closer to design, as the V-model introduced as an industrial development method [15].

V-model is similar to Waterfall in the steps definition but at the same time built more connection between each step, attaching each other with layers with different levels of abstraction.

The Test-Driven Development is cycle as depicted in Fig. 2, inspired by the TDD mantra of Beck [8]. The method starts with the test implementation, where the developer needs to write some test code that makes sense for the application, compile it and run without errors. In the first run, the test

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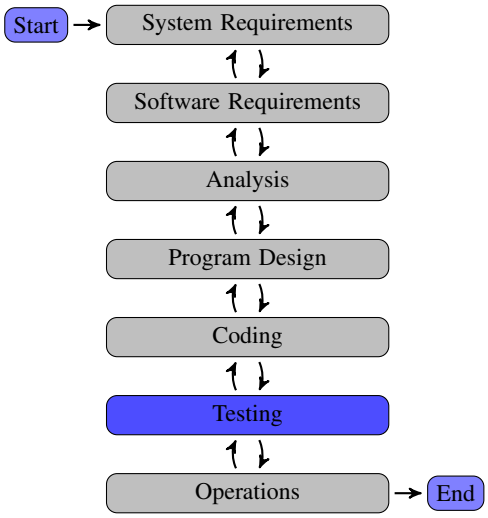

Fig. 1. Flowchart of Waterfall method [14].

result will probably fail, which is not a problem considering the approach has a refactoring stage.

In refactoring step, the design is improved until the results are satisfactory, attending the test requirements. If, after refactoring, the tests pass the user can return to the evaluation step and write more code to make sure that all application requirements are satisfied. If the new tests fail, the product can be refactored to implement necessary changes to make it pass.

The test structure described by Hackenberg and Mund [6] is very close to Test-Driven Development, presenting a structure more flexible to industrial and Engineering applications. The Test-Driven Design (TDD) introduces not only the notion of increments during the developing process but also an extra phase in the Test-Driven Development.

The TDD is divided into two steps (Fig. 3). The first one, highlighted in green, is called preparation phase, and the second, implementation phase.

The preparation phase is where all the project requirements are defined, the interface with the device to be tested, as well as the first set of tests necessary to build the design. After preparation, the implementation flow follows the Test-Driven

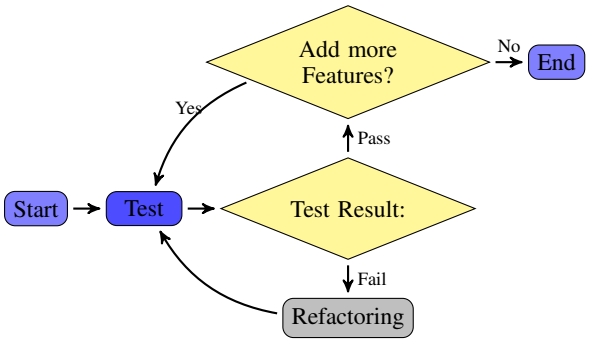

Fig. 2. Flowchart of Test-Driven Development.

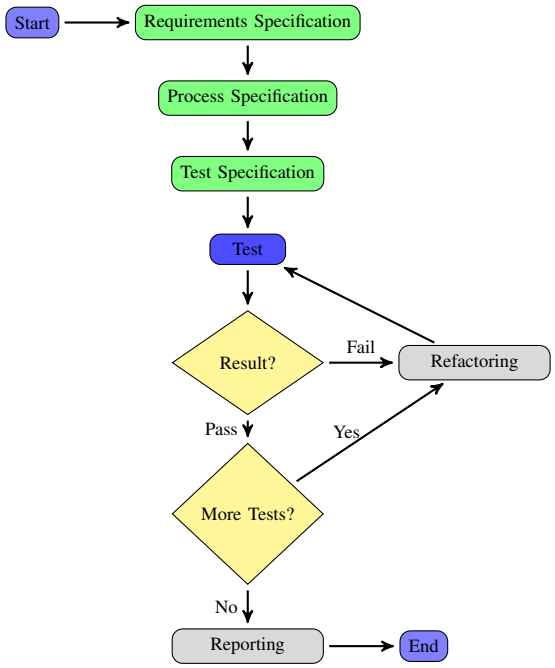

Fig. 3. Flowchart of Test-Driven Design [6].

Development rules, and at the end offers a final report with the test results.

III. Methodology

In the preparation phase it is defined the inverter, filter and grid parameters as depicted in Fig. 4. The system has three open parameters in a manner to create different test scenarios for the device under test, in this case, the modulation algorithms. The equation that corresponds with the R_g and L_g are

$$Z = \frac{V_{nom}^2}{P_{nom}/3}$$
$$R_g = \cos(\phi) \times Z$$
$$L_g = \frac{\sqrt{Z^2 - R_g^2}}{2\pi f_{nom}},$$

where $\cos(\phi)$ is the power factor and Z is the impedance calculated by the voltage and nominal power reference.

It is also defined the three-phase Half-Bridge as inverter topology (Fig. 5), the nominal power of the system, and the DC Bus voltage (Section V), which tests need to be evaluated in other to ensure a good functionality of the power system. Table I shows these tests, the second column table links the test with the settable parameters of Fig. 4.

The Test 1 ranges modulation index and grid power factor, with nominal power, measuring the number of commutation in a second, the WTHD, and the average value of TRD. Test 2 ranges the nominal power and grid power factor, with unitary modulation index, the metrics are the same as Test 1. Test 3 verifies the converter linearity by applying different modulation index and measuring the output voltages to extract

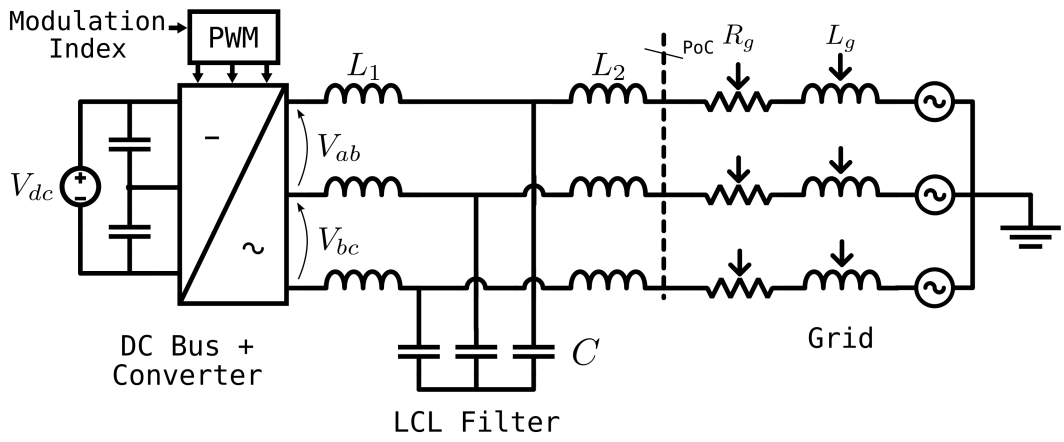

Fig. 4. Grid-Tied Inverter, and the R_g, L_g and converter modulation index parameters.

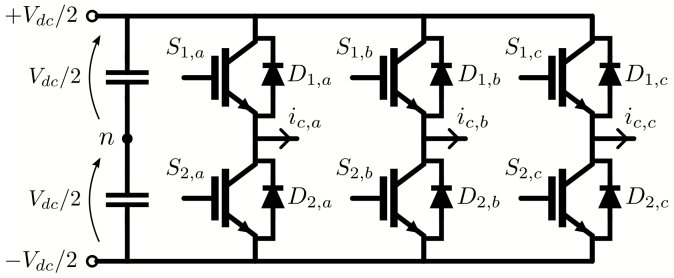

Fig. 5. The three-phase Half-Bridge converter.

TABLE I
LIST OF TESTS EVALUATED BY THE TDD.

Test Name	Parameters	Figures of Merit
Test 1	Modulation Index, Power Factor	Number of commutations per second, WTHD, and TRD
Test 2	Nominal Power, Power Factor	Number of commutations per second, WTHD, and TRD
Linearity (Test 3)	Modulation Index	V_{ab} and V_{bc} Fundamental Amplitudes
Power Losses (Test 4)	Modulation Index, Power Factor	Switching and Conduction Losses per component

the fundamental wave of V_{ab} and V_{bc}. And Test 4 ranges the power factor with nominal power and unitary modulation index, and calculates switching and conduction losses for each leg component based on energy curves, extracted from manufactures' datasheets.

Table II shows the value constraints for the tests. Standards and the application are used to define these requirements and verify expected performance behaviors of the converter. These threshold values assert if the tests pass or fail.

IV. FIGURES OF MERIT

The next sections describe the metrics to evaluate the Table I tests. The number of commutations of the top switch in each phase of the half-bridge on Section IV-A, the Weighted Total Harmonic Distortion (WTHD) on Section IV-B, the average value of Total Rated-current Distortion (TRD) on Section IV-C, the Linearity test on Section IV-D, and the power losses calculation on Section IV-E.

TABLE II
CONSTRAINTS DEFINED FOR THE TDD VALIDATION.

Figure of Merit	Threshold
Number of commutation per second	20000 (ad.)
WTHD	5%
TRD	5%
Total Power Losses	2000 W

A. Number of commutation per second

With this metric it is possible to compare the switching distribution between the phases and the modulation approaches. Excessive commutation in a short period of time is a dangerous behavior for the switching modules life spam.

Algorithm 1 shows briefly how this computation is done. First, the code replicates the switch signal in two variables, S_{1y} and S_{1z}, and shifts one of these signals. Second, these two signals are subtracted and taken the absolute value, placing in $S_1^{'}$, and representing all S_1 commutation events. The algorithm has described and developed in this way to use the power of Numpy array functions.

Algorithm 1 Number of commutation per second

procedure COMMUTATIONS_PER_SEC(S_1, total_time)
  $S_1 = \{S_{1,1}, S_{1,2}, ..., S_{1,N}\}$ ▷ Only 0s and 1s
  $S_{1y} \leftarrow \{S_{1,1}, S_{1,2}, ..., S_{1,N-1}\}$
  $S_{1z} \leftarrow \{S_{1,2}, S_{1,2}, ..., S_{1,N}\}$
  $S_1^{'} \leftarrow |S_{1y} - S_{1z}|$ ▷ Switching instants
  $n_{sw} \leftarrow \sum S_1^{'}$
  $n_{sw,sec} \leftarrow \frac{n_{sw}}{total\_time}$
  return $n_{sw,sec}$
end procedure

B. Weighted Total Harmonic Distortion

In order to calculate the WTHD, TRD, and linearity test has introduced in TDD the methodology of *"very short time harmonic measurements"* from IEEE 519-2014 [16]. The standard establishes a measurement on an interval of three (3) seconds with a sliding-window of 15 samples, each one with 12 cycles, for 60 Hz, or 10 cycles, for 50 Hz, equals 200 ms. In TDD these parameters are totally configurable to shorten the refactoring cycle.

Equation (1) computes the WTHD [17] of one window (j)

$$WTHD_j = \frac{\sqrt{\sum_{h=2}^{\infty}\left(\frac{V_{h,j}}{h}\right)^2}}{V_{1,j}}. \quad (1)$$

And the final WTHD is an average value of all windows

$$WTHD\ (\%) = \frac{1}{N}\sum_{j=1}^{N} WTHD_j \times 100,$$

where N is the number of windows.

The signal used to calculate the WTHD is a relation between the output inverter voltages. The value of $2V_{ab} + V_{bc}$ describe the behavior of the current through LCL filter connected to the converter [18].

C. Average Total Rated-current Distortion

The Total Rated-current Distortion (TRD, equation (2)) presented on IEEE 1547-2018 [19] considers all harmonic content, including sub-harmonics and inter-harmonics, of the current measured, except the fundamental.

$$TRD_{abc} = \frac{\sqrt{I_{rms,abc}^2 - I_{1,abc}^2}}{I_{rated}} \quad (2)$$

where $I_{rms,abc}$ is each phase RMS value, $I_{1,abc}$ is the RMS value of the fundamental components, and I_{rated} is the nominal current of the converter. For three-phase converters, I_{rated} is calculated as

$$I_{rated} = \frac{P_{nom}}{3\ V_{nom}}. \quad (3)$$

Considering that TRD is calculated for each phase current, it is possible to compute the average as

$$TRD_{av}(\%) = \frac{TRD_a + TRD_b + TRD_c}{3} \times 100. \quad (4)$$

As presented in the previous section, the TRD procedure as the same of WTHD considering the *"very short time harmonic measurements"* of IEEE 519-2014.

D. Linearity

The linearity test uses the Fast-Fourier Transform (FFT), available in Numpy library, with the signals V_{ab} and V_{bc} (Fig. 4 and Fig. 6) to extract the fundamental values.

The result of this test is the linearity plot with the amplitude of fundamental component for each modulation index tested.

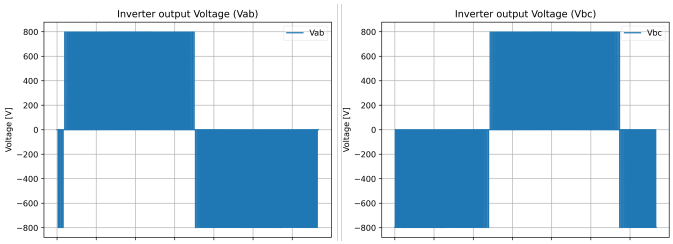

Fig. 6. Output voltages of Half-Bridge inverter.

TABLE III
SWITCHING LOSSES TABLE FOR HALF-BRIDGE

S_1	$i_c/\|i_c\|$	S_1	D_1	S_2	D_2
⌐	-1	0	0	E_{off}	0
	+1	E_{on}	0	0	E_{rr}
⌙	-1	0	E_{rr}	E_{on}	0
	+1	E_{off}	0	0	0

E. Power Losses

The losses considered for this metric are the conduction and switching ones for each component of the inverter. The procedure developed to calculate is present in [20]. The total power losses can be described as

$$P_{total} = P_{cond} + P_{sw}, \quad (5)$$

where P_{cond} is the conduction losses contribution and P_{sw} the switching losses.

1) Switching Losses: Table III shows in the first columns the converter states, with the top-switches ($S_{1,\{a,b,c\}}$ of Fig. 5) represented by the commutation waveform for opened and closed stages. The second column ($i_c = i_{c,,\{a,b,c\}}$) makes a reference to the current direction through the converter leg. When a commutation occurs the algorithm measures the current direction and applies the absolute value into the correct energy curves. The energy curves depend on the switches used for construction or simulation of the converter topology chosen (in this case, the Half-Bridge). They are E_{on} that corresponds to the IGBT turn-on, E_{off} for the IGBT turn-off, and E_{rr} for the diode turn-off or, more usual, the diode recovery. Turn-on losses for the diode are, in general, not taking into account because of its low contribution for total losses. These curves can be interpolated from the manufactures' datasheet or can be processed from SPICE simulations using a validated by the manufacture model and algorithms to compute the power, and the curve area for the energy contributions. At the end of signal processing the algorithm sums all the contributions and measures the switching losses.

2) Conduction Losses: The conduction losses can be calculated directly using the equations (6) and (7) accordingly with the current through each component. The parameters $V_{o,igbt}$, $R_{o,igbt}$, $V_{o,diode}$ and $R_{o,diode}$ are defined by the datasheet, Pou [20] in his article also describes how to calculate these values by measuring and interpolating the datasheet curves.

TABLE IV
GENERAL CONVERTER SPECIFICATIONS

DC Bus Voltage (V_{dc})	800 V
Nominal Convert Power (P_{nom})	100 kW
Nominal Converter Voltage (V_{nom})	220 V
Rated Current Capacity (i_{rated})	151.52 A
Nominal Converter Frequency (f_{nom})	60 Hz
Switching Frequency	10 kHz
Filter Inductor (L_1)	160 μH
Filter Capacitor (C)	183.7 μF
Filter Inductor (L_2)	340 μH

$$P_{cd}(S_{ix}) = V_{o,igbt}\ \bar{i}(S_{ix}) + R_{o,igbt}\ i^2_{rms}(S_{ix}) \quad (6)$$
$$P_{cd}(D_{ix}) = V_{o,diode}\ \bar{i}(D_{ix}) + R_{o,diode}\ i^2_{rms}(D_{ix}), \quad (7)$$

where S_{ix} and D_{ix} are the three-phase components ($i = \{1, 2\}$ and $x = \{a, b, c\}$) of half-bridge (Fig. 5), and $\bar{i}$ and i_{rms} are the average and the RMS current across the components, respectively.

V. RESULTS

The TDD simulation time considered in this section was the same of IEEE 519-2014 standard to calculate the harmonic distortion. Table IV shows the converter parameter used by the tests in all scenarios, except when changed by the test (Table I).

The results presented are from a report built at the end of the test procedure using a self-document tool to extract and compare the test results. The tables have a color scheme based on how far the values are compared to their thresholds (Table II).

In Fig. 7 it is possible to analyze the reduced inverter effort when the modulation index is bigger than the unit, close to the overmodulation region. The figure also shows a difference, caused only by the Sinusoidal modulation, to distributed equally the commutation rate between the phases.

Phase A
Power Factor

Modulation Index	0.64
0.5	20000
1.0	18480
1.1	14280
1.15	13240
1.2	12360

Phase B
Power Factor

Modulation Index	0.64
0.5	20000
1.0	18440
1.1	14240
1.15	13200
1.2	12400

Phase C
Power Factor

Modulation Index	0.64
0.5	20000
1.0	18440
1.1	14240
1.15	13160
1.2	12400

Fig. 7. Test 1: Number of commutation per second. Columns for each converter phase using the Sinusoidal modulation with the same scenarios.

Fig. 8 shows different TRD scenarios that can be contrasted with the result of Fig. 7. The overmodulation flattens the voltage output increasing the current through the phases. The Space Vector and the Sinusoidal results fail for modulation

Average value of TRD in %. Threshold = 5

Space Vector
Power Factor

Modulation Index	0.64	1
1.0	0.288970	1.225133
1.1	0.321480	1.334746
1.15	0.363311	1.970044
1.2	1.282038	5.073074

Carrier-Based
Power Factor

Modulation Index	0.64	1
1.0	0.344076	1.037011
1.1	0.339384	1.052101
1.15	0.358245	1.639300
1.2	1.380339	4.660338

Sinusoidal
Power Factor

Modulation Index	0.64	1
1.0	0.373342	1.313764
1.1	2.012580	8.720287
1.15	2.860604	11.982654
1.2	3.380129	13.756540

Fig. 8. Test 1: Average TRD. Tables for all approaches tested, values in the same scenarios.

wTHD computed using 2*Vab + Vbc in %. Threshold = 5
Power Factor

Modulation Index	0.1	0.46	0.64	1
0.1	0.156136	0.174482	0.121039	0.171768
0.5	0.104606	0.095884	0.060515	0.109349
1.0	0.120876	0.105186	0.077925	0.092905
1.1	0.708405	0.688169	0.599552	0.676069
1.15	0.965983	0.961793	0.884001	0.976588
1.2	1.112732	1.112828	1.056718	1.158908

Fig. 9. WTHD for Sinusoidal modulation.

index equal to 1.2, the maximum modulation index for three-phase systems is 1.15, and in presence of a purely resistive load ($\cos(\phi) = 1$). The Carrier-Based and Space Vector offer some safety with TRD values under 2%. Fig. 9 shows the worst WHTD results between the modulations tested, after the unitary modulation index the values jump but still under standard control, below 5% [19].

Fig. 10 shows the linearity test for Sinusoidal and Space Vector modulations and can be noticed that Space Vector (graphically the same result as Carrier-Based) sustains a linear behavior even with a modulation index equal to 1.2.

Fig. 11 shows the total power losses for all modulation approaches with resistive power factor. The results are measured in Watts and the losses are sum by each component for the three phases.

Besides the total power losses be homogeneous for all algorithms, the consuming differences between S_1 and S_2, and

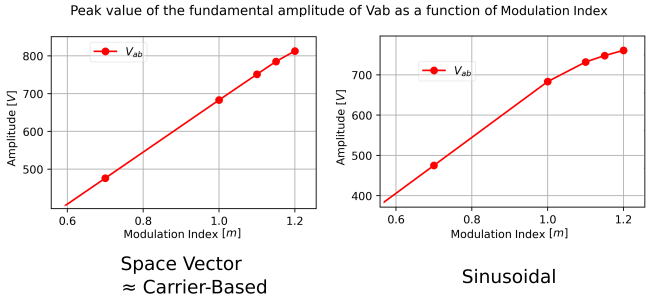

Fig. 10. Linearity results for $m = \{0.7\ 1\ 1.1\ 1.15\ 1.2\}$.

Losses table calculated offline

	S1	S2	D1	D2	
$P_{Total\ Car.-Bas.}$	634.223194	640.595894	157.940278	160.822019	Carrier-Based
$P_{Total\ SV}$	641.333613	649.355036	154.433832	157.171672	Space Vector
$P_{Total\ Sin.}$	636.418367	642.565498	156.337505	158.976868	Sinusoidal

Fig. 11. Total Power Losses for $\cos(\phi) = 1$ and modulation index $= 1$, in Watts.

D_1 and D_2 can be discussed. This difference has a direct relation with the commutation per second table (Fig. 7) showing that Space Vector implemented presents a bigger difference than the other methodologies. The table also points that the Sinusoidal and Carrier-Based modulations have very similar results and are more efficient in this simulation scenario.

VI. Conclusion

The tests developed using TDD offer a complete understanding of how the modulation on Grid-Tied Inverters affects the performance and behavior of the converter, as well the power system. With this and other test techniques, it is possible to build an incremental development to verify constantly the design and applied improvements in a short period of time.

The reporting and testing approaches can be applied beyond Grid-Tied Inverters and modulation algorithms. The procedure can be used for any non-HIL simulation as well for other applications that are necessary verification or validation based on project or standard requirements.

The choice for Python is fundamental because of your practicality to work in any programming methodologies like structural, object-oriented, or functional, being welcome for developers of many programming backgrounds. Also, the good use of Python libraries like pytest framework and Numpy can help the user to calculate huge amounts of data in a few seconds. Python allows for the user multi-platforms integration with several tools like PSIM, Matlab, Typhoon-HIL API, serial connections, communication protocols, spreadsheets, web applications, and more.

The next step of this work is to evaluate and document the same test cases for the Neutral-Point Clamped converter, a three-level converter topology.

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