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TÉCNICAS PARA REDUÇÃO DE CONSUMO EM CONVERSORES ANALÓGICO-DIGITAIS POR APROXIMAÇÃO SUCESSIVA E COMPARTILHAMENTO DE CARGA

DISSERTAÇÃO DE MESTRADO

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TÉCNICAS PARA REDUÇÃO DE CONSUMO EM CONVERSORES ANALÓGICO-DIGITAIS POR APROXIMAÇÃO SUCESSIVA E COMPARTILHAMENTO DE CARGA

por

Taimur Gibran Rabuske Kuntz

Dissertação apresentada ao Curso de Mestrado do Programa de Pós-Graduação em Informática da Universidade Federal de Santa Maria (UFSM, RS), como requisito parcial para a obtenção do grau de **Mestre em Computação**

Orientador: Prof. Cesar Ramos Rodrigues

Co-orientador: Prof. Jorge Manuel dos Santos Ribeiro Fernandes

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elaborada por
Taimur Gibran Rabuske Kuntz

como requisito parcial para obtenção do grau de
Mestre em Computação

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Santa Maria, 16 de março de 2012.

DEDICATÓRIA

Ao Seu Vitor...

The show must go on!
I'll face it with a grin!
I'm never giving in!
On with the show!

— FREDDIE MERCURY

E à pessoa a quem devo tudo, e não tive tempo de retribuir...

Je ne te vois pas,
je ne t'entends pas,
tu n'es pas ici,
tu n'es plus ici.
Néanmoins, maman,
je t'aimerai tous le jours.

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"Um homem precisa viajar. Por sua conta, não por meio de histórias, imagens, livro ou TV. Precisa viajar por si, com seus olhos e pés, para entender o que é seu. Para um dia plantar suas próprias árvores e dar-lhes valor. Conhecer o frio para desfrutar do calor. E o oposto. Sentir a distância e o desabrigo para estar bem sob o próprio teto. Um homem precisa viajar para lugares que não conhece, para quebrar essa arrogância que nos faz ver o mundo como imaginamos e não simplesmente como ele é ou pode ser. Que nos faz professores e doutores do que não vimos, quando deveríamos ser alunos, e simplesmente ir ver... Il faut aller voir - é preciso ir ver! É preciso questionar o que se aprendeu. É preciso ir tocá-lo".

— Amyr Klink

RESUMO

Dissertação de Mestrado
Programa de Pós-Graduação em Informática
Universidade Federal de Santa Maria

TÉCNICAS PARA REDUÇÃO DE CONSUMO EM CONVERSORES ANALÓGICO-DIGITAIS POR APROXIMAÇÃO SUCESSIVA E COMPARTILHAMENTO DE CARGA

Autor: Taimur Gibran Rabuske Kuntz
Orientador: Cesar Ramos Rodrigues, Dr.
Co-orientador: Jorge Manuel dos Santos Ribeiro Fernandes, Dr.
Local e data da defesa: Santa Maria, 16 de março de 2012.

As novas tendências e tecnologias emergentes motivam o projeto de conversores analógico-digitais (ADCs) que precisam suprir especificações cada vez mais restritivas. Nesse contexto, uma métrica de projeto que é constantemente forçada em direção à redução é o consumo de potência, fato esse que leva à concepção de melhorias tanto em nível arquitetural como em nível de circuito elétrico. Este trabalho tem como objetivo elevar a eficiência energética dos ADCs por aproximações sucessivas e compartilhamento de carga, visto que essa é uma arquitetura relativamente nova e inexplorada. Portanto, três ADCs completos são projetados ao longo deste trabalho, e cada um traz inovações que ajudam a reduzir o consumo de potência. As técnicas concebidas aqui incluem maneiras novas de efetuar a captura do sinal de entrada e um circuito para reduzir a potência drenada no ciclo de pré-carga. Além disso, três arquiteturas diferentes de controlador digital para essa topologia de ADC são expostas. Mais, um novo circuito de chave com *bootstrapping* é apresentado, o qual apresenta um número de dispositivos menor e uma eficiência energética extremamente alta.

Palavras-chave: Conversores analógico-digitais, Eficiência energética, Conversores por registrador de aproximação sucessiva, Compartilhamento de carga.

ABSTRACT

Master's Dissertation
Computer Sciences
Universidade Federal de Santa Maria

TECHNIQUES FOR POWER REDUCTION IN SUCCESSIVE APPROXIMATION CHARGE SHARING ANALOG-TO-DIGITAL CONVERTERS

Author: Taimur Gibran Rabuske Kuntz
Advisor: Cesar Ramos Rodrigues, Dr.
Coadvisor: Jorge Manuel dos Santos Ribeiro Fernandes, Dr.

New trends and emerging technologies motivate the design of analog-to-digital converters (ADCs) which must fit in increasingly constrained environments. Within this context, one design metric which is constantly forced towards reduction is the power consumption, leading the designers to come up with improvements in both the architecture and circuit levels. This work aims to push forward the energy efficiency of the successive approximation charge sharing ADC, which is a relatively new and unexplored architecture. Therefore, three complete ADCs are designed throughout this work, each one bringing novelties that help decreasing the power consumption. The techniques devised here include novel manners of dealing with the tracking of the input signal and a circuit to reduce power drained in the pre-charge cycle. Also, three different architectures of digital controller for this ADC topology are designed. Moreover, a novel bootstrapping switch circuit is presented, which provides lower devices-count and a extremely high energy efficiency.

Keywords: Analog-to-digital conveters, energy efficiency, successive approximation register converters, charge sharing.

SUMÁRIO

1 INTRODUÇÃO

É trivial perceber um grau crescente de onipresença de elementos computacionais no cotidiano humano. O homem contemporâneo tem uma grande parcela das suas tarefas diárias guiadas ou intermediadas por computadores e sistemas eletrônicos. Esta afirmação pode ser clareada se recorrermos ao exemplo da trajetória evolutiva de dois aspectos fundamentais da vida moderna: os meios de comunicação e a economia.

Em (CLARK, 2007), o autor sumariza de maneira extremamente interessante a evolução da velocidade de propagação da informação no decorrer dos séculos. De acordo com o autor, antes da revolução industrial, as pessoas viviam em um mundo onde a informação se propagava tão lentamente que muitos morriam guerreando por questões que já haviam sido resolvidas. A Batalha de New Orleans, lutada aos 8 de janeiro de 1815 por britânicos e estado-unidenses, resultou em mais de mil mortos e ocorreu porque os comandantes de ambos os exércitos não sabiam que o Tratado de Gante havia estabelecido a paz entre os países em 24 de dezembro do ano anterior. Ainda de acordo com o autor, a informação viajava em velocidades da ordem de poucos quilômetros horários naquela era, barreira que veio somente a ser quebrada com a introdução do telégrafo em 1844 e da linha telegráfica submarina entre Inglaterra e França em 1851. Ainda no fim do século XIX, com a difusão dessa tecnologia pelo mundo, o grande terremoto de Nobi, no Japão, foi publicado em Londres com em torno de um dia de atraso desde o seu acontecimento, apesar dos mais de 9 mil quilômetros que separam os países. No entanto, por mais que essa evolução soe surpreendente, uma velocidade nessa ordem de grandeza soa ínfima se comparada aos padrões contemporâneos. Para exemplificar, informações sobre o terremoto na costa leste do Japão, ocorrido em 11 de março de 2011, estavam disponíveis em telefones móveis ligado à internet de praticamente todo o mundo minutos após o seu acontecimento.

Outro aspecto global que sofreu drástica mutação possibilitada pelas tecnologias eletrônicas diz respeito à economia. A história do sistema monetário se estende por milênios, partindo de sistemas arcaicos de troca (escambo), passando por sistemas baseados na ausência de reciprocidade explícita (denominadamente economias de doação), evoluindo para moedas de troca padronizadas(CLARK, 2007). No entanto, uma grande parcela das transações de capital atuais acontece sem troca de propriedade de bens físicos, como metais preciosos ou papel-moeda. O capital passou a ser abstraído por *bytes* em bancos de dados de instituições bancárias. Atualmente, é absolutamente plausível depender exclusivamente de meios de troca virtuais para comprar e vender (transferências bancárias *on-line*, compras por cartão de crédito ou pagamento por débito bancário). O dinheiro físico deixou de ser vital e deu espaço ao dinheiro eletrônico, sem qualquer impacto negativo ao sistema capitalista e, pelo contrário, facilitando e agilizando transações comerciais.

Essa tendência de crescente dependência de computadores para as tarefas diárias sugere que os sistemas eletrônicos sofram uma progressiva redução de volume visando ao conforto de seus usuários. De fato, as tecnologias emergentes em sistemas eletrônicos cada vez mais se focam em miniaturização e portabilidade. Um acessório eletrônico portátil típico é alimentado por baterias, mas o objetivo máximo destas aplicações é que elas operem autossuficientes em termos de energia, retirando a potência elétrica necessária do próprio ambiente. Para alcançar este fim, torna-se necessário recorrer a transdutores para transformar energia de diversas formas em corrente elétrica. Como exemplos, podem ser citados células solares e transdutores piezelétricos e termoelétricos. Ultimamente, o uso da energia cada vez mais abundante no espectro eletromagnético de radiofrequência aparece como uma alternativa viável de suprimento. O projeto de sistemas autossuficientes é atualmente inviabilizado pela incompatibilidade da potência gerada por essas fontes alternativas com a potência necessária para alimentar sistemas convencionais. Portanto, a redução de potência dos blocos de circuito nesses sistemas eletrônicos portáteis é de evidente benefício, pois maximiza o tempo de vida das baterias nos sistemas dependentes destas e pode, idealmente, viabilizar a concepção de sistemas autossuficientes em energia.

Um dispositivo requerido para uma larga gama de aplicações de baixa potência é o conversor analógico-digital (ADC). ADCs são circuitos capazes de transformar uma

grandeza física do mundo real e analógico em uma representação abstrata aproximada no domínio digital. De um lado, o domínio analógico representa fielmente uma variedade de situações do mundo real, enquanto o domínio digital sofre desenvolvimento massivo em tecnologias para processamento de sinais e transmissão e armazenamento de dados. Existem diversas topologias de ADCs, cobrindo diferentes gamas de especificações, em torno da tríade de requisitos: frequência de amostragem, potência e resolução.

Os conversores *flash*, por exemplo, apresentam baixa latência, fruto do funcionamento altamente paralelizado. São utilizados $2^N - 1$ comparadores, onde N é o número de *bits* do conversor, e todos são ativados ao mesmo tempo para cada conversão. Disto, decorre que o consumo de potência dos conversores *flash* é relativamente alto se comparado às demais topologias. Por outro lado, é uma boa opção para aplicações que demandam taxa de conversão alta e resolução baixa.

Outras topologias populares são a sigma delta ($\Sigma\Delta$), capaz de efetuar conversões a resoluções mais altas com taxas de amostragens moderadas; os conversores *pipeline*, que desempenham bem em resoluções e taxas de amostragem médias; e os conversores por aproximações sucessivas, que são explicados na próxima seção.

1.1 Conversores por redistribuição e por compartilhamento de carga

Entre as diversas topologias de ADCs atualmente disponíveis, os conversores por registrador de aproximações sucessivas, ou *successive approximation register* (SAR), são conhecidos pela sua elevada eficiência energética. Eles são muito atrativos em aplicações que demandam baixas taxas de amostragem e com requisitos de potência restritivos, sobretudo por causa da sua dependência logarítmica de complexidade com relação à resolução. Baseados em um laço de realimentação, os conversores SAR convergem iterativamente à palavra digital final, comparando o valor de um conversor digital-analógico (DAC) com uma representação amostrada do sinal de entrada, capturado por um circuito de *track-and-hold*. O ciclo de conversão é guiado pelo algoritmo da busca binária.

Os conversores SAR mais utilizados se baseiam no método da redistribuição de carga, proposto em (MCCREARY; GRAY, 1975), chamado assim devido à topologia de DAC que eles empregam. Nesta abordagem, o DAC capacitivo é também usado como

track-and-hold, e a cada passo do algoritmo de conversão, um dos capacitores de peso binário é conectado ao nó de terra ou tensão de referência, fazendo a tensão de erro diminuir em direção a zero.

Em (CRANINCKX; PLAS, 2007), os autores apresentam um método para implementar conversores SAR capacitivos baseando-se em compartilhamento de carga, ao invés de redistribuição de carga. Como vantagem, o DAC é totalmente pré-carregado uma vez no início do ciclo de conversão, ao invés de interações com as linhas de alimentação na resolução de cada *bit*. Além disso, os requerimentos de tempo de acomodação para o DAC podem ser relaxados durante o ciclo de projeto e, ainda mais importante, tornando desnecessário o emprego de um amplificador operacional como *buffer* da tensão de referência. Erroneamente, esse amplificador é geralmente desconsiderado nas medições de potência de conversores por redistribuição de carga, embora possa ser significante e até mesmo dominante. O princípio de funcionamento dessa topologia de ADC é explicado com mais detalhes nos Capítulos 3 e 4.

Em (GIANNINI et al., 2008), um ADC por compartilhamento de carga com desempenho superior em termos de ruído térmico é apresentado. A robustez do projeto é garantida com um ciclo a mais na conversão, um comparador com nível de ruído programável e um pequeno processamento digital.

De fato, (CRANINCKX; PLAS, 2007) e (GIANNINI et al., 2008) são as únicas publicações de maior relevância tratando dessa arquitetura. O ADC por aproximações sucessivas e compartilhamento de carga é uma arquitetura relativamente recente, com aproximadamente cinco anos desde a sua concepção em (CRANINCKX; PLAS, 2007). Deste modo, esta é uma topologia parcamente explorada que, por consequência, oferece grande margem para desenvolvimento tecnológico e científico.

1.2 Escopo deste trabalho

Este trabalho foca-se em otimizar o consumo de potência em ADCs por aproximações sucessivas utilizando compartilhamento de carga. Para isso, são apresentadas inovações em nível de topologias e circuitos.

Os elementos textuais deste trabalho são apresentados na forma de artigos científicos. Esta modalidade é prevista em (UNIVERSIDADE FEDERAL DE SANTA MARIA. Pró-Reitoria de Pós-Graduação e Pesquisa, 2010), sendo que cada capítulo corres-

ponde a um artigo científico publicado, submetido ou escrito para periódico indexado. A produção científica relativa a conferências internacionais foi incluída no formato de apêndices, e deve ser considerada como parte importante deste trabalho.

O Capítulo 2 apresenta a topologia de conversor analógico-digital explorada neste trabalho, e explica o seu funcionamento.

O Capítulo 3, publicado no periódico *Springer Analog Integrated Circuits and Signal Processing* sob o título de *A 54.2µW 5MSps 9-bit Ultra-low Energy Analog-to-Digital Converter in 180nm*, propõe um ADC por compartilhamento de carga que faz uso de escalonamento de tensão e ciclo de pré-carga iterativo para aumentar a eficiência energética. Também é apresentado um circuito de controle eficiente projetado utilizando *standard cells*.

O Capítulo 4, entitulado *A 5MSps 13.25µW 8-bit SAR ADC with Single-Ended or Differential Input*, corresponde ao artigo aceito para publicação no periódico *Elsevier Microelectronics Journal* (carta de aceitação no Anexo A). O artigo traz um ADC que faz uso de um circuito de *track-and-hold* que ajusta automaticamente o nível de modo comum da saída recorrendo a técnica de capacitores comutados. Esta técnica foi apresentada anteriormente em conferência (Apêndice C). A topologia de ADC é fortemente baseada no trabalho anteriormente publicado em conferência e incluído no Apêndice B. O circuito de controle para esse ADC foi também apresentado anteriormente em conferência e é incluído no Apêndice A.

Por último, o Capítulo 5 apresenta uma discussão geral a respeito dos resultados obtidos e o Capítulo 6 conclui este trabalho e propõe trabalhos futuros.

2 CONVERSORES DE APROXIMAÇÃO SUCESSIVAS POR COMPARTILHAMENTO DE CARGA

De forma similar aos conversores analógico-digitais por redistribuição de carga, a arquitetura baseada em compartilhamento de carga requer um controlador, um comparador de tensão e um conversor digital-analógico. Entretanto, devido ao seu princípio de operação, um circuito de *track-and-hold* é necessário, visto que o sinal capturado não pode ser mantido apenas pelas capacitâncias do conversor digital-analógico. A topologia é ilustrada na Figura 2.1, para um conversor de 10 bits.

Uma conversão se dá na borda de descida da entrada $\overline{\text{reset}}$. Enquanto esta entrada

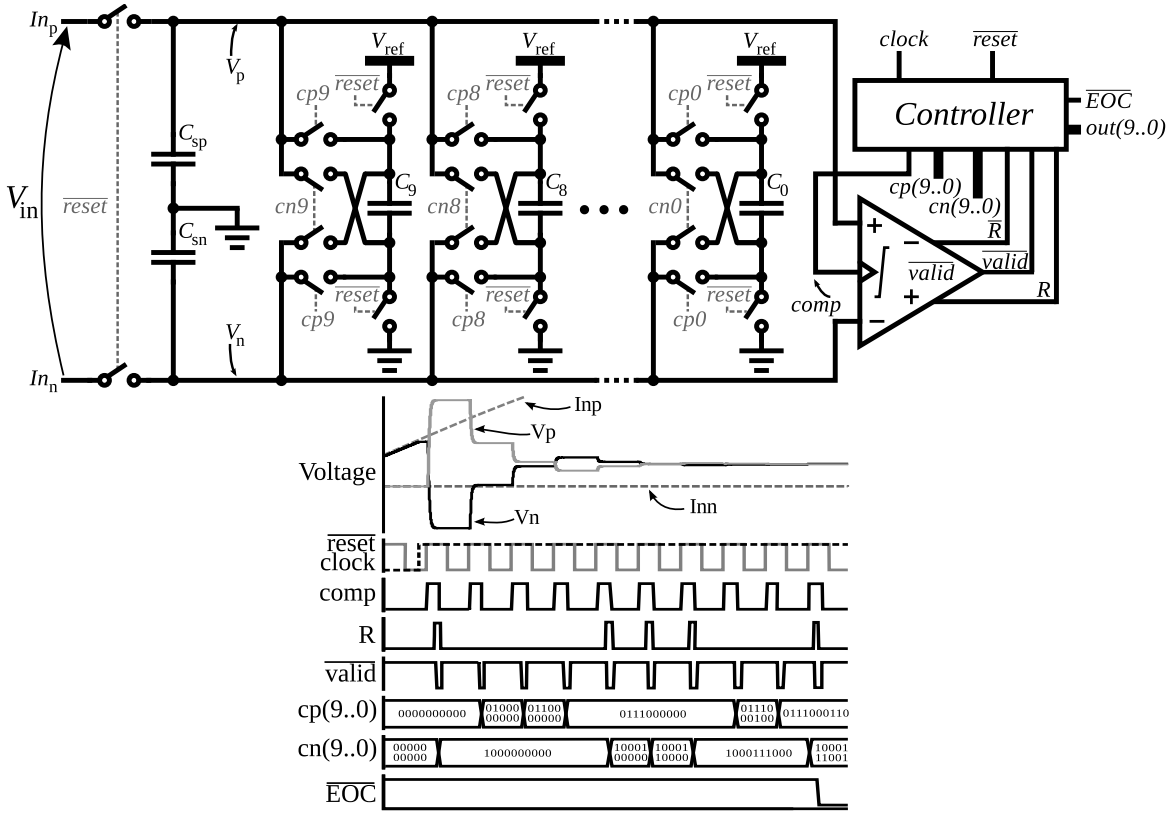

Figura 2.1: Diagrama de blocos do SAR por compartilhamento de carga e formas de onda ilustrativas.

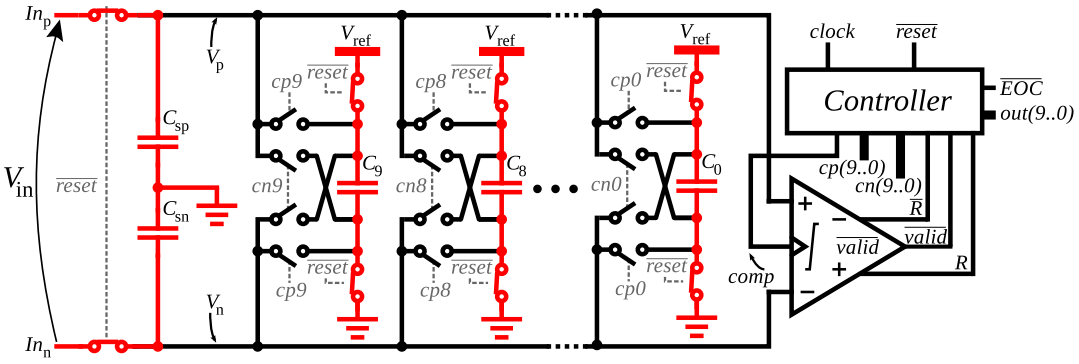

Figura 2.2: Ciclo de pré-carga do DAC e amostragem da entrada

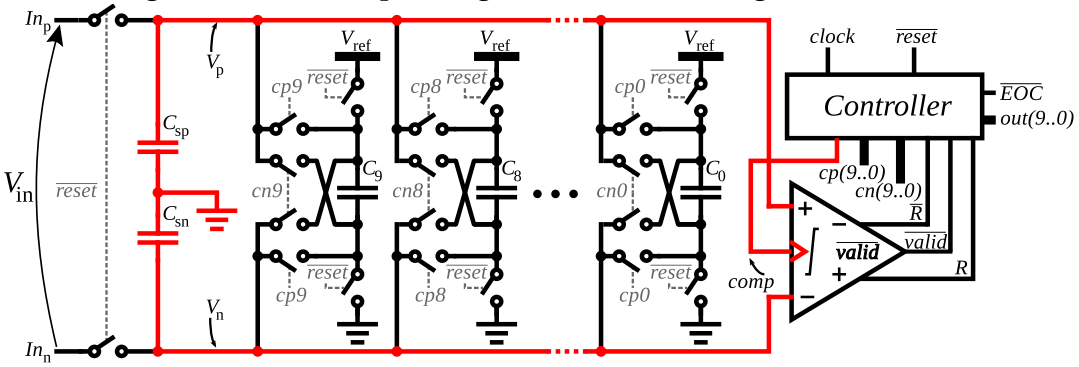

Figura 2.3: Ciclo de decisão do bit mais significativo

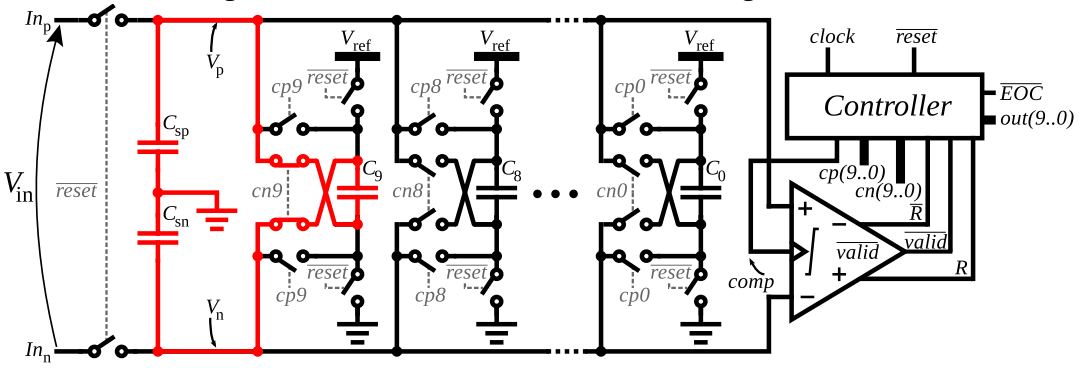

Figura 2.4: Arranjo dos capacitores para MSB=1

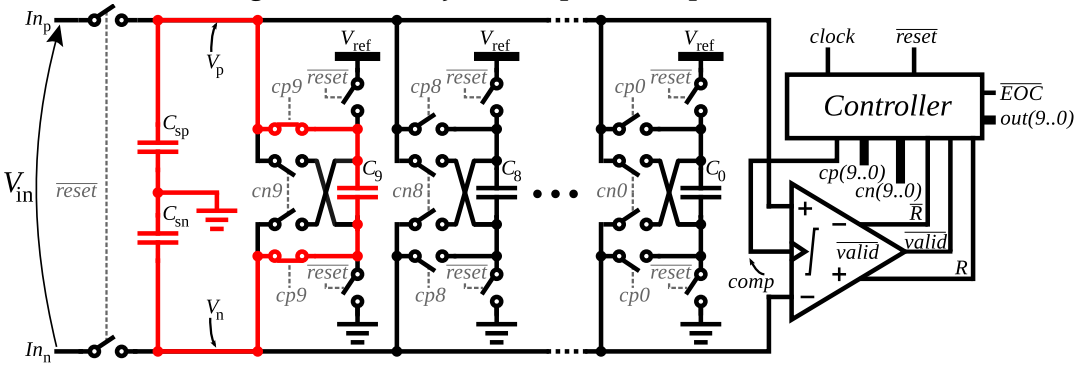

Figura 2.5: Arranjo dos capacitores para MSB=0

está baixa, o circuito *track-and-hold* está acompanhando a entrada; enquanto isso, o conversor digital-analógico está sendo pré-carregado (Figura 2.2). Para o conversor de 10 bits aqui descrito, o conversor digital-analógico é constituído por 10 capacitores com valores de carga definidos conforme pesos binários. Durante o processo de pré-carga, estas capacitâncias são ligadas à referência de tensão V_{ref}, e desconectadas dos capacitores de *track-and-hold* e entre si. Quando $\overline{\text{reset}}$ retorna ao nível lógico alto, o sinal acompanhado pelo *track-and-hold* é mantido estável, e o conversor digital-analógico é desconectado de V_{ref}.

Após, o circuito SAR (registrador de aproximação sucessiva) começa a executar o algoritmo de busca binária, adicionando ou subtraindo carga nos capacitores de amostragem. Na próxima borda de subida do *clock*, o comparador é inicializado de forma a comparar as tensões V_p e V_n (Figura 2.3). O resultado da comparação é o bit mais significativo (MSB) da conversão. Após, alguma carga precisa ser adicionada ou subtraída das capacitâncias do *track-and-hold*, de forma a fazer a diferença de tensão (erro de tensão) entre V_p e V_n menor. Se, por exemplo, V_p for mais alta que V_n, nós removemos a quantidade de carga equivalente a um MSB (bit mais significativo), ativando o sinal de controle $cn9$ (Figura 2.4). Assim, o capacitor C_9 seria conectado em antiparalelo com a combinação em série de C_{sp} e C_{sn}. Se, por outro lado, V_p fosse menor que V_n, a mesma quantidade de carga seria adicionada a C_9, por meio da ativação do sinal de controle $cp9$ (Figura 2.5). O processo repete-se progressivamente para os outros bits, adicionando ou subtraindo carga da carga amostrada em V_{in}. Ao final, $cn(9...0)$ representa a saída de 10 bits desejada.

3 ARTIGO I: A 54.2μW 5MSps 9-BIT ULTRA-LOW ENERGY ANALOG-TO-DIGITAL CONVERTER IN 180nm TECHNOLOGY

RABUSKE, T. G.; NOOSHABADI, S.; RODRIGUES, C. R. A 54.2 μW 5 MSps 9-bit ultra-low energy analog-to-digital converter in 180 nm technology. **Analog Integrated Circuits and Signal Processing**, Springer. doi:10.1007/s10470-011-9821-4. Pré-publicado em dez. 2011.

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A 54.2 µW 5 MSps 9-bit ultra-low energy analog-to-digital converter in 180 nm technology

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Abstract This paper aims to address the growing need for ultra-low power analog-to-digital converters (ADC). For this purpose, we pushed the limitations of conventional successive approximation register ADCs through the use of deep voltage scaling, a novel iterative precharging scheme, and topological improvements over recent works. From the simulations results we achieve a figure of merit of 31 fJ per conversion step, with an 8.45 effective number of bits, working at 5 MSps.

Keywords SAR ADC · Ultra-low power · Ultra-low energy · Step-wise · Charge sharing

1 Introduction

Lower system power consumption is a requirement for an ever increasing range of applications. Beyond the energy critical health applications, like pacemakers or hearing aids, there are new application frontiers where power budgets are becoming very tight. One example is wireless sensor networks, where sometimes the only energy available for the nodes to work comes from scavenging, or lossy inductive coupling with a radio-frequency source. Also, the concept of wearable computing demands power-aware solutions, in order to increase battery lifetime.

In the field of analog to digital data converters, the successive approximations register (SAR) topology has been proved to be very attractive for low data rates, in applications where power is the main constrain. Part of the merit comes from the presence of a single comparator independently of resolution. Few approaches have been tried to extend the power efficiency further. In [11] authors present a low energy successive approximation charge-redistribution (CR) analog-to-digital converters (ADC) focusing on distributed sensor networks, where both active and standby power must be minimized. In [8], the design of an ADC working at 0.6 V that relies on a time-domain comparator is presented. In [13] a very energy efficient SAR ADC is designed that realizes the CR process based on a multi-step charging.

This paper extends the traditional energy-efficient SAR ADC, with improvements on the topological level and other circuit-level novelties. In the inspiring work in [3], the authors present a method to increase the efficiency of a successive approximation converter by doing the signal processing using charge sharing (CS), instead of CR. As a consequence, low output impedance operational amplifiers can be eliminated on the input and reference signals, indirectly reducing the power consumption of the ADC itself. In this paper, we will present a further improvement to this methodology, in a way which the area is substantially reduced. Further, the power drained from input signal is also reduced. The CS methodology made another innovation possible, that could push the limits of standard SAR further, reducing the amount of energy necessary to precharge the same values of capacitance.

Further improvements on the circuit implementation level are also made towards power reduction. We have

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implemented the logic control circuit with both gate-level optimization and deep voltage-scaling, and proved this choice to have a great overall impact on ADC power efficiency.

We describe the operating principle in Sect. 2, together with the architectural innovations. The circuit level implementation is discussed in Sect. 3, where a more detailed description of each circuit block is provided. The proposed layout is presented and explained in Sect. 4. The simulation results including transient noise and further information on the simulation environment are both described in the Sect. 5. Section 6 concludes this work.

2 Operating principle

A successive approximation ADC converts a continuous analog waveform into a discrete digital representation via a binary search algorithm. In practice, binary search can be implemented based on a comparator, that compares at each step a sampled representation of the input signal to the output of a digital-to-analog converter (DAC) fed with a register representing a successively evaluated digital value, as in Fig. 1.

Conventional SAR ADCs rely on the CR method, so-called due to the DAC topology they employ. In that approach, the capacitive DAC is also used as tracking

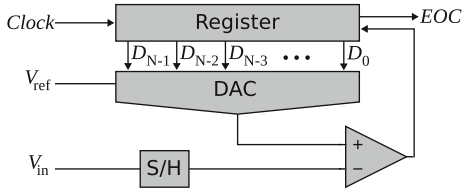

Fig. 1 SAR ADC topology

circuit, and at every step, one of the binary-weighted capacitors is tied to ground or reference terminal, leading the error voltage to diminish towards zero.

In [3] authors present a method to implement capacitive SAR based on CS, rather than CR. As an advantage, the DAC is totally precharged once in the beginning of a conversion cycle, instead of per bit active interactions with the supply lines. Still, the settling requirements for DAC can be relaxed during design cycle, and most importantly, avoiding any power-hungry opamp buffering the reference signal. Misleadingly, this opamp is often not accounted for in the energy measurement of a given converter, which could be significant, or even dominant.

In this paper, we extended the passive CS ADC with topological improvements. Figure 2 shows a schematic representation of the architecture together with illustrative waveforms.

The circuit is composed of a digital controller, a voltage comparator, an analog multiplexing track and hold and a DAC with its pre-charge circuitry. Notice the DAC is made by binary weighted capacitive network and associated MOS-switches.

Assume that the DAC capacitive matrix in Fig. 2 is initially pre-charged to V_{ref}. Also, assume all *cn* and *cp* switches are off. One of the capacitor pairs between C_{pA}–C_{nA} and C_{pB}–C_{nB} is tracking the input signal, while the other pair is connected to DAC. The conversion cycle is started by a pulse on the *start* input pin. The analog multiplexer then switches the capacitor pair that was initially in tracking mode to the *Qp* and *Qn* nodes. A pulse on the *comp* pin signals the comparator to compare the sampled voltages on *IN+* and *IN−* nodes. The output from comparator forms the most significant bit (MSB) of the conversion. This bit is fed back into the controller. This first bit can also be treated as the sign (positive or negative) of the

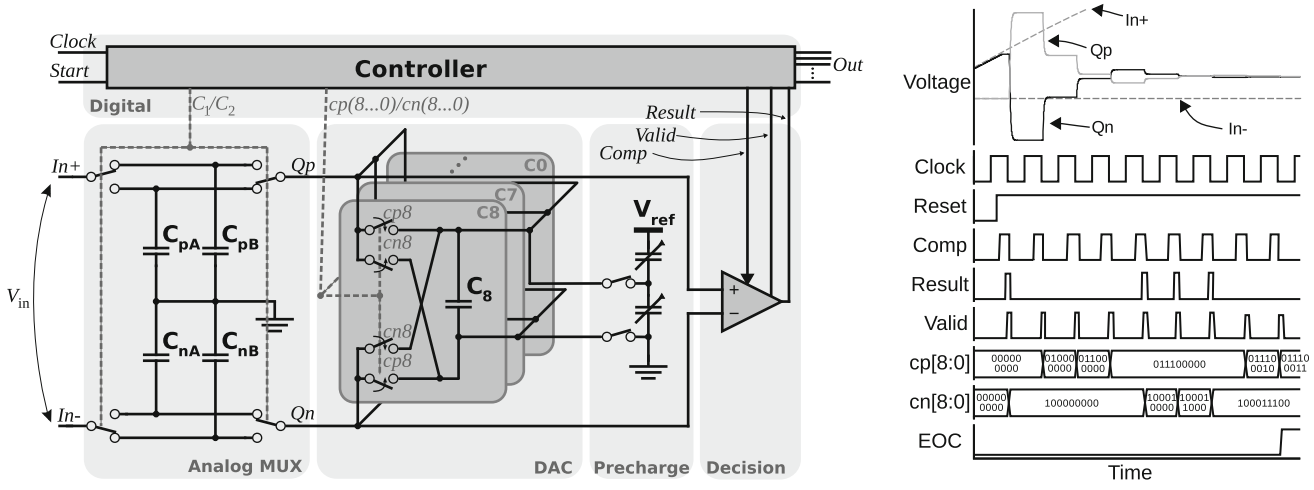

Fig. 2 Block diagrams and corresponding waveforms for the proposed ADC topology

input signal. The controller uses this bit to set the controlling pairs of switches *cn*8 and *cp*8 to add/subtract charge to the input capacitor in order to converge the voltage difference between *Qp* and *Qn* nodes to zero. If the first resolved bit was an 1, the switches *cn8* are turned on, forcing an amount of charge equal to half of the input range ($\pm V_{ref}C_8$) to be subtracted from the equivalent capacitance formed by input capacitance pair and C_8. Otherwise, in the case of MSB resolved as 0, *cp*8 switches turn on, adding charge to the equivalent capacitance. The operation is continued for all the other bits of the converter and, at the end, an *N*-bit representation of the sampled input is available at the output.

In conventional CR ADCs, an offset voltage in the comparator results in an offset of the transfer function of the converted signal, and does not manifest as non-linearity in the converter. On the other hand, for the passive CS topology, this is not the case. One can see that the total equivalent capacitance is different for each step during the search algorithm. Initially, the only capacitance connected to the comparator is one of the sampling capacitor pairs (C_{pA}–C_{nA} or C_{pB}–C_{nB}). During the course of binary search, more capacitors are added in parallel to the sampling pair, increasing the equivalent capacitance. Even though the whole processing happens in the charge domain, the comparator is only able to make decisions regarding voltage levels on *Qp* and *Qn* nodes. The voltage forced on the terminals of a capacitor due to electrical charge is given by $\frac{Q}{C}$. However, *C* varies at each step of the search. Therefore, any mismatch on the comparator manifest as non-linearity in the converter.

Nevertheless, conversion in CS domain has some important advantages over the standard CR. The first advantage is at the input track and hold side. On CR scheme, the DAC capacitors are also used to sample the signal. So, for the input signal to be sampled in a sufficiently short time, generally voltage buffers with low output impedance are needed on the input signal. This indirectly increases the overall power consumption, reducing energy efficiency. In the proposed modified architecture, with the use of an analog multiplexer, one input capacitor pair is used to perform the conversion, while other pair is made to track V_{in}. So, signal source impedance on the input can be relaxed to reduce the settling time to one conversion period.

Another important characteristic of CS architecture is with regard to the DAC pre-charge. In the CR scheme, on each step of the search, one capacitor is charged or discharged to reference voltages. Once again, for this charging to happen in a short time requires a buffer on the reference signal. However, for the CS scheme, the whole DAC is pre-charged only once per conversion, in the beginning of the cycle. This feature allows us to increase the energy efficiency further, using a novel pre-charge mechanism, as be presented next.

2.1 Pre-charge cycle

A significant part of energy spent by the ADC is due to pre-charge of capacitive DAC in the beginning of conversion cycle. To save energy we employ the stepwise pre-charge technique proposed in [12].

Consider a simple circuit composed by a capacitor being charged by a voltage source, through a simple switch. For the sake of simplicity, the switch is represented by a single resistor. At time $t = t_0$, the switch is turned on, and some charge is drained off the source towards the capacitor, and after some *RC* time constants, the current flow virtually stops. The total energy dissipated in the voltage source is given by,

$$E_{T,\,conventional} = E_S + E_C \tag{1}$$

where E_S and E_C are the energies dissipated in the switch and capacitor, respectively.

On the situation above, resistance of the switch only affects the settling time, and does not change the energy needed to completely charge the capacitor. The energy drawn from the voltage source is equally distributed among the switch and the capacitor as,

$$E_S = E_C = \frac{1}{2}CV^2 \tag{2}$$

Since the energy is quadratic function of the voltage value, one can reduce the power dissipated in the switches performing the charge in multiple steps, as presented in [12]. This way the power dissipation is reduced at the cost of decreased circuit speed.

Figure 3 shows a basic implementation of this stepwise charging scheme. A bank of *N* equidistant voltage supplies is used, for an *N*-step pre-charge. To charge the load capacitance to *V*, all the sources are connected in succession to the load, in a non-overlapping manner.

For each charge step of $\frac{V}{N}$, the dissipation on the switch is given by,

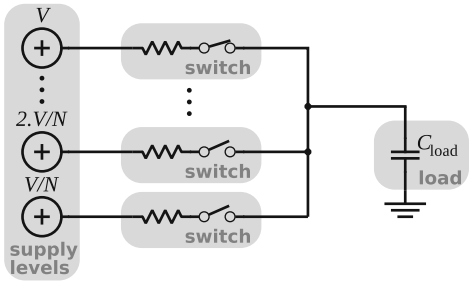

Fig. 3 Pre-charge cycle schematic diagram

$$E_{S,\,step} = \frac{1}{2} C \frac{V^2}{N^2}. \tag{3}$$

The energy lost in the switch for the complete charge cycle is equal to

$$E_{S,\,stepwise} = N \cdot E_{S,\,step} = \frac{E_S}{N}. \tag{4}$$

Therefore, it is N times smaller than in the conventional 1-step charging. Putting it all together, the total energy dissipated in the pre-charge process is

$$E_{T,\,stepwise} = \frac{E_S}{N} + E_C. \tag{5}$$

These calculations exclude the energy required by the logic circuit overload necessary to perform multiple steps charging. The benefits and drawbacks of this implementation technique are discussed in Sect. 3.

3 Circuits implementation

In this section, we will plunge deeper in the circuit level implementation of each one of the blocks that together make up the proposed SAR ADC. The low energy nature of the proposed ADC also implies an low average power. This is typically achievable eliminating any source of static power. An energy-efficient circuit must be able to dissipate power only when doing something useful, and the standby power needs to be small compared to active power. All the circuits that are presented here satisfy these requirements, providing an ADC where the power consumption is a linear function of sampling rate for a wide range of operation.

3.1 Capacitive array

In this presented topology, size of the capacitive array is limited by two factors: noise and mismatch. For the given accuracy, mismatch is the dominating factor over noise, and dictates the minimum size of the binary weighted capacitors matrix. The capacitors are implemented with metal–insulator–metal layers, available in the process.

In order to satisfy linearity constraints, the MSB capacitor is sized to meet the constraint $3\sigma_{INL} < 1$, where σ_{INL} is the standard deviation for integral non-linearity (INL). This corresponds to around 99.73% of the dies satisfying the INL constraints. With the MSB capacitor dimensioned to be 1 pF, minimum values for LSBs are impractical due to technology design rules and low tolerance to charge injection effects from the switches. To avoid this problem, for the 4 LSBs we implemented the circuit proposed in [3] (Fig. 4). This comes at the expense of a more complex pre-charge cycle.

The pre-charge cycle can be described as follows. The MSB capacitors (C_8–C_3) are pre-charged to reference voltage, while the least significant bits capacitors (C_2–C_0) are discharged. Next, the charge from the C_3 is shared among the LSB capacitances iteratively. When the *step2* signal is pulled high, half the charge from C_3 goes to C_2, since they have the same capacitance value. In the next step, the resulting charge from C_2 is shared with C_1. The process is repeated for C_0 also, and in the end, the amount of charge in each capacitor is proportional to its weight in the SAR algorithm. This behavior is also shown in the waveforms of Fig. 4.

The increased complexity in the pre-charge cycle does not come at the cost of more complex control logic, as the controller is quite simple, and was implemented using a simple shift register and glue logic generating a sequence of non-overlapping signals. As a further simplification of the controller, energy-smart stepwise pre-charge circuitry uses the same logic control signals used for the LSB capacitors precharging.

The intermediate voltage steps are assumed to be available inside the chip. To keep the energy gain close to the theoretical relation derived before in (5), the intermediate voltage steps would have to be made close to the theoretical steps derived. However, the intermediate steps does not affect any linearity or accuracy aspect of the ADC, being responsible only for increasing the energy

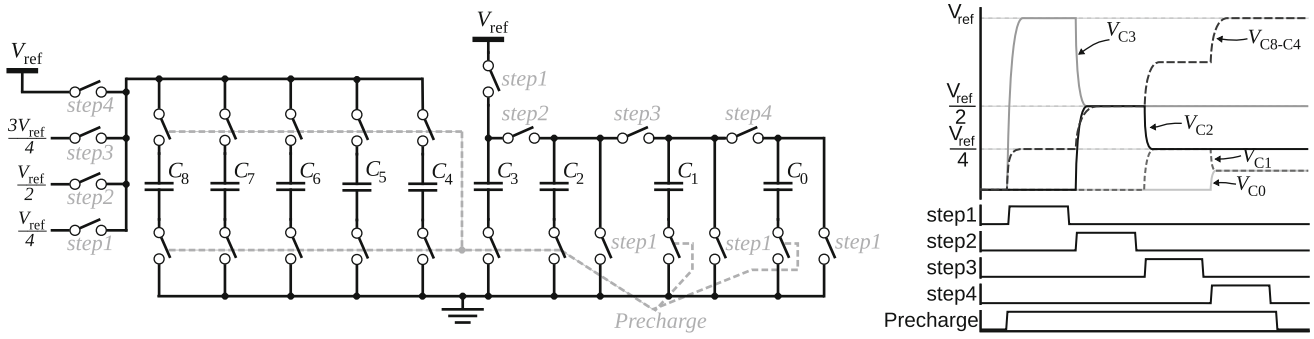

Fig. 4 DAC circuitry

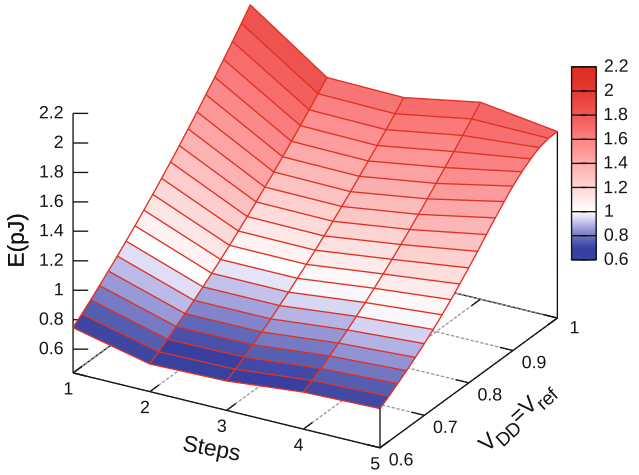

Fig. 5 Pre-charge energy as a function of supply voltage and steps

efficiency. So one can relax the precision of the intermediate steps or even ignore them (tie to ground) towards reduced design complexity, paying with a increased power consumption.

Figure 5, plots the total energy spend on the pre-charge cycle as a function of supply voltage and number of steps. The measured energy includes the energy consumed for the *N*-step capacitors divider network, logic overhead, level converters and of course the DAC itself. One can see that it is not a linear function of the number of steps. This is because the introduction of more voltage steps increases the number of the level converters, the register width, and the controller complexity. Unfortunately the the power consumption of level converters is not a linear function of the supply voltage.

3.2 Input sample and hold

The sampling circuit in our architecture has a distinct advantage over the work in [3]. Consider the schematic shown in Fig. 6(a), representing the standard approach in [3] for tracking and holding the input signal on CS ADCs. Initially, the switch S_{track} is closed, while S_{sample} is opened. This way, the input signal is tracked by capacitors C_{tp} and C_{tn}. When a conversion is requested, S_{track} is opened and S_{sample} is closed after some short delay (non-overlapping control signals). Tracking and sampling capacitors are made the same size, and half the charge held in C_t is transferred to C_s. Switch S_{sample} is opened again, and the charge in C_s is used for the ADC conversion. Note that since C_{sp} and C_{tp} are not tied together anymore, S_{track} can be closed again and start tracking V_{in} early in preparation for the next conversion cycle. The settling time is not a critical factor anymore, relaxing any requirement for the switches, and more importantly, avoiding an opamp for the input signal.

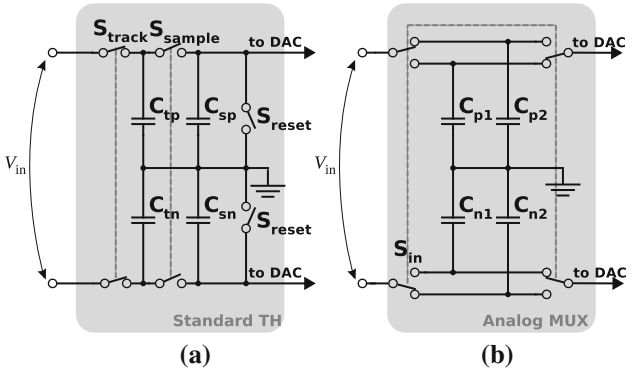

Fig. 6 Track and hold schemes. **a** Standard approach. **b** Novel input multiplexer sampling approach

One caveat of this topology is the voltage swing of the sampling circuit. Since the charge is divided between C_t and C_s, the voltage swing available for processing is half the voltage swing on the input. This reduces the signal to noise ratio (SNR) on the DAC.

The size of the capacitors on the standard approach, is a function of the size of the DAC capacitors, which in turn are limited by noise and mismatch. To maintain the binary weight relations during the conversion steps, the charge kept on the MSB capacitance of the DAC (C_{MSB}) must be half the charge kept on C_s, if the input sampled was full scale signal,

$$\left.\frac{Q_{sampled}}{2}\right|_{V_{in}=V_{ref}} = C_{MSB} \cdot V_{ref} \tag{6}$$

since just half the charge tracked on the input is transferred to the sampling capacitor,

$$Q_{sampled} = \frac{Q_{tracked}}{2} \tag{7}$$

Looking at the circuit in Fig. 6(a), one can see that the charge is tracked on the two capacitors $C_{tp} = C_{tn}$. However, the capacitance seen from the input is $\frac{C_{tp}}{2}$, and then

$$Q_{tracked} = \left.\frac{C_{tp}}{2} V_{ref}\right|_{V_{in}=V_{ref}} \tag{8}$$

Combining (6), (7) and (8) results in,

$$C_{tp} = C_{tn} = C_{sp} = C_{sn} = 8C_{MSB} \tag{9}$$

Next consider our novel multiplexer sampling scheme shown in Fig. 6(b). The circuit works as follows. Initially, one capacitor pair is tracking the input, while the other one is tied to the DAC. So, when a conversion starts, the capacitor pairs switch roles, and the tracked input signal is fed to the DAC for further processing, while the other capacitor pair starts tracking the input signal again. In doing so, we have maintained the benefits of the standard

track and sample circuitry; the constraints on the switches are relaxed due availability of longer settling time, and the absence of the opamp to buffer the input signal. However, in our design, the voltage swing for the sampled signal is the same that of the input signal, therefore resulting in an improvement in the SNR. To appreciate the benefit of this we need to examine the size necessary for the sampling capacitances. Having the same relation as in (6) the sampled charge is given by,

$$Q_{sampled} = Q_{tracked} \tag{10}$$

Now, combining (6), (8) and (10), it leads to (11).

$$C_{p1} = C_{n1} = C_{p2} - C_{n2} = 4C_{MSB} \tag{11}$$

Reducing the input capacitance by half results in 50% area saving in the input capacitance, which is responsible for the larger area portion in this type of converter. Also, there is no need for a reset on the sampling capacitor; as the charge left from earlier conversions just present as an energy gain, since less energy must be drawn from the input signal for the sampling.

3.3 Comparator

From the energy point of view, the comparator must consume very little or no power while not performing a comparison. The other requirements include a minimum offset, since the CS SAR is much more sensitive to this non-ideality as it manifest as non-linearity. Moreover, the noise will limit the size and power consumption of the comparator. As a design trade-off, the noise was kept under quantization noise, as in (12), following the design guidelines for dynamic comparators and estimation techniques presented in [7, 9].

$$P_{noise} < \frac{(V_{LSB})^2}{12} \tag{12}$$

As discussed before, unlike conventional active CR SARs, this ADC topology has it linearity performance degraded due to comparator offset. To rectify this problem the comparator topology chosen for this design has a programmable binary array of capacitors which has been used for the purpose of offset calibration. A binary search for the optimal point permits the offset to be kept under very low voltage levels (hundreds of μV). The comparator offset is very sensitive to the common-mode (CM) voltage in its input terminals. Although, the ADC topology guarantees that the CM fed into the comparator is the same of the input sampled signal for every conversion cycle. Thus, if the input CM is kept constant, the offset is also kept constant. Moreover, the simulations show that, for the 9-bit converter, temperature and voltage supply variations cause just subtle variation on the offset and does not lead to significant non-linearity in the

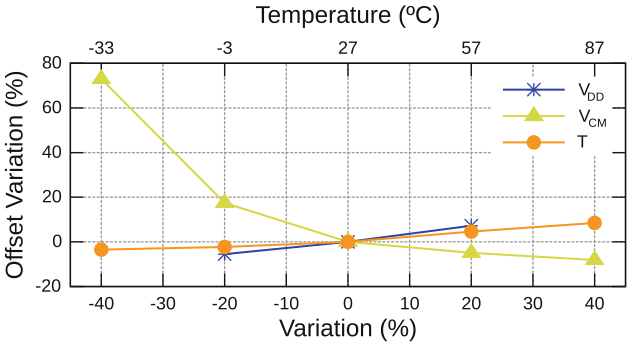

Fig. 7 Percent offset deviation as function of percent change in V_{DD} and V_{CM} and absolute temperature T, normalized for typical operation conditions $V_{DD} = 1.8$ V, $V_{CM} = 450$ mV and $T = 27$°C

ADC. Then, if the input CM is made constant, the calibration procedure is performed just once before the start of circuit operation. In Fig. 7 we plot the standard deviation of the variation on the offset voltage after calibration as function of the supply voltage V_{DD}, the CM voltage V_{CM} and the temperature. The results are extracted from Monte-Carlo simulations and normalized for the typical operating conditions: $V_{DD} = 1.8$ V, $V_{CM} = 450$ mV and at the temperature of 27°C.

The topology chosen is shown in Fig. 8.

3.4 Control Logic

For the execution of the SAR conversion algorithm, a digital control block is needed. In the conventional synchronous SAR topologies, the frequency of the clock signal is, at least, N (number of bits) times faster than the sampling rate. This is required because the algorithm works iteratively, with N comparisons and decisions. For our work, we need additional clock cycles for the pre-charging scheme. The number of additional cycles needed due to the iterative pre-charge is equal to the number of DAC pre-charge steps. This work employs a 4-step pre-charge scheme, that are executed while the input signal is tracked. Therefore, the designed ADC requires a total of 13 clock

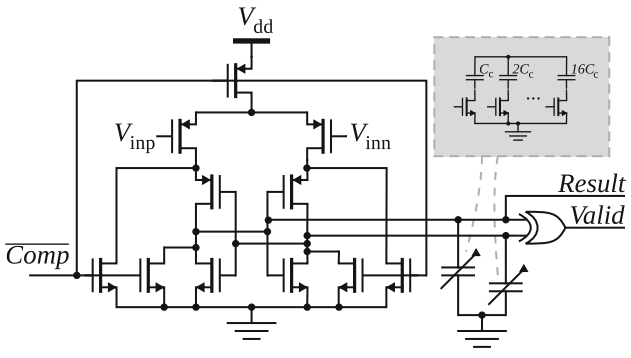

Fig. 8 Comparator schematic

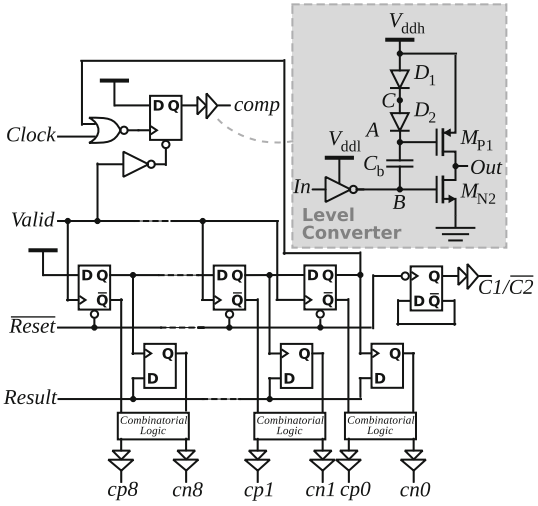

Fig. 9 Logic circuit schematic with the level converter

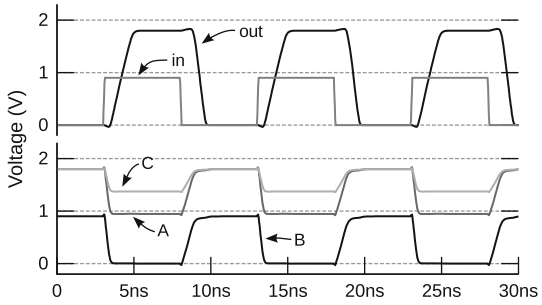

Fig. 10 Voltages levels during level conversion, with $V_{DD_L} = 900$ mV

cycles per conversion. With no step-wise pre-charging the number of conversion clock cycles reduces to 10. In terms of maximum sampling frequency, the actual 5 MSps would increase to 6.5 MSps if no step-wise pre-charge was employed.

A simplified schematic of the logic block implementation is shown in Fig. 9. The switching power dissipated by a digital circuit using static CMOS gates is approximated as [10],

$$P_{SW} = C \cdot V^2 \cdot f \tag{13}$$

with C the total capacitance switched per clock cycle, V the supply voltage and f the switching frequency. So, there is a significant power saving in reducing the supply voltage. Also, the short-circuit power and leakage currents reduce at lower supply voltages, specially in the situation where voltage swing is less than the sum of P and N transistor thresholds. For this reason, low power MOS technology with higher threshold voltages have been employed. In applications where energy is critical, one can scale down digital supply voltage and accept a slower circuit operation. However, scaling down the supply for the whole circuit increases the DAC (capacitive matrix) noise sensitivity, with an effect on the resolution of the ADC. One solution is to use a higher supply voltage for the DAC and a scaled down voltage for digital controller. For this to work across the interfaces, we have employed voltage shifters to connect the digital controller and the ADC. The topology chosen was proposed in [5], and shown together with the logic circuit in Fig. 9.

The circuit performs voltage shifting as follows: considering the input node transitions from high to low level; node B at the output of the inverter transitions to V_{DD_L}, switching node A to $V_{DD_H} - 2{\cdot}V_{diode} + V_{DD_L} \approx V_{DD_H}$, due to bootstrap effect across the C_b capacitor. Note that C_b was already charged to $V_{DD_H} - 2{\cdot}V_{diode}$ before the transition. After, the transition diodes D_1 and D_2 are reverse biased, and gate of M_{P1} is tied to V_{DD_H}, turning this transistor off. M_{N2} is on because of the inverter, and the output node is pulled down to ground. During this process, bootstrap capacitor is charged to $V_{DD_H} - V_{DD_L}$. When input node transitions to high, node B will pull to ground, turning the diodes on, and causing the voltage at node A to settle to $V_{DD_H} - 2{\cdot}V_{diode}$. M_{N2} turns off, and M_{P1} pulls up output node to V_{DD_H}, and the bootstrap capacitor voltage charges to $V_{DD_H} - 2{\cdot}V_{diode}$. The whole process is energy efficient and the circuit does not show static power consumption. Figure 10 plots the voltages waveforms during the operation of the ADC. The input is switched at a frequency of 100 MHz in the plot.

The limit on the voltage scaling in the digital voltage supply is set by the minimum voltages required at the input of voltage level-converters, and needed for the proper operations of the logic gates. Table 1 shows the propagation delays from V_{DD_L} to V_{DD_H} for transition from 0 to 1 and 1 to 0 in the level-converter. The propagation delay grows exponentially as the value of V_{DD_L} drops, and the circuit is unusable for the ADC sampling at 5 MSps when V_{DD_L} drops below 0.8 V. With a digital supply of 900 mV, power dissipation (with level converters included) for the same sampling rate is more than twice smaller than using the typical 1.8 V.

4 Layout

In Fig. 11 we present the proposed layout for the ADC, with some routing omitted for clarity. The input capacitors

Table 1 Delays as function of V_{DD_L}

V_{DD_L}	$t_{d,0\to1}$ (ns)	$t_{d,1\to0}$ (ns)
0.9	1.27	1.62
0.8	1.43	3.04
0.7	1.82	9.45
0.6	3.75	62.09

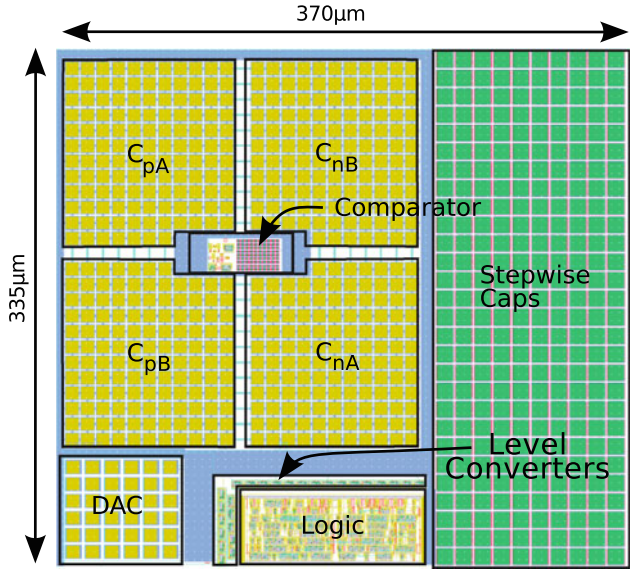

Fig. 11 Proposed layout

were placed in a common-centroid form, in order to reduce the effects of fabrication gradients. The DAC just occupies a small portion of the whole design. The logic controller, surrounded by the voltage shifters on the layout, was designed using standard cells methodology. Stepwise capacitors, even though have a much larger capacitance than the input capacitors, have a total area not much larger than one third of the whole ADC area. This was possible because we used MOS transistor thin oxide for their implementation. The dimensions are shown in the figure, and the total area is 0.124 mm^2.

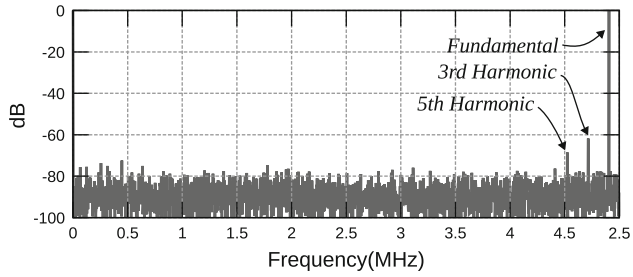

Fig. 12 FFT plot with the input near Nyquist frequency

5 Simulation results

In order to characterize and measure converters performance, a set of simulations were performed. A 0.8 V peak-to-peak input signal with a frequency of about 2.45 MHz was applied to the converter, with a sampling frequency of 5 MSps. This rate was achieved with a clock frequency of 65 MHz. Transient noise had been included in the simulation, in order to account for thermal noise. Transient noise feature has been used before, as in [2] to determine an ADC performance. Since transient noise simulation relies on statistical data, 10 runs has been performed. Also, packaging parasitics were included to the extracted layout, to achieve a more accurate test condition.

A total of 4,096 samples per run has been simulated, and the FFT frequency spectrum for one of these runs is shown in Fig. 12, with more significant harmonics. An effective number of bits (ENOB) mean μ_{ENOB} of 8.45 is achieved (with the standard deviation $\sigma_{ENOB} = 0.02$), reflecting a mean signal to noise and distortion ratio of 52.63 dB. Third and fifth harmonics are 61.76 and 68.51 dB under the fundamental signal, respectively, for this run.

Under the test conditions, power is distributed among the blocks as follows; the largest power consumption comes from the logic controller, contributing to 41.5% of the consumption of the whole chip. The next dominant component of power dissipation comes from the comparator, with 39.21%. The reference voltage circuitry and the voltage shifter array contribute 13.86 and 1.5%, respectively. The input signal drains the other 3.93% of the power needed for the circuit operation. The total power consumed is 54.2 µW.

A common figure of merit (FOM) in ADCs, is expressed in terms of energy necessary per conversion step, and is expressed as,

$$FOM = \frac{P}{2^{ENOB} F_s} \tag{14}$$

with P being the total power consumed by the circuit and F_s the sampling frequency. The converter designed achieves a mean FOM of 31 fJ/conv. step. Table 2 shows a comparison between recent SAR ADC works and our design.

Table 2 Comparison with state-of-the-art designs

Parameter	[3]	[4]	[14]	[13]	[1]	[6]	This work
Technology (nm)	90	140	180	65	180	90	180
Bits	9	12	12	10	10	8	9
ENOB	7.8	10.99	10.55	8.75	9.4	7.8	8.45
Sampling rate	50 MSps	6.25 kSps	100 kSps	1 MSps	100 kSps	10 MSps	5 MSps
FOM (fJ/conv. step)	65	66	167	4.4	56	30	31

6 Conclusion

We have presented a extremely energy-efficient ADC. The limits of the current SAR topology were pushed towards the maximum power saving employing several innovative design techniques. The achieved results are close to similar designs in more advanced silicon processes. The use of a non-state-of-the-art mature 0.18 µm technology, can also reduce the production cost.

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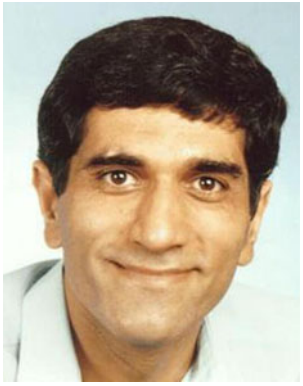

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4 ARTIGO II: A 5MSps 13.25μW 8-BIT SAR ADC WITH SINGLE-ENDED OR DIFFERENTIAL INPUT

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A 5MSps 13.25μW 8-bit SAR ADC with Single-Ended or Differential Input

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Abstract

An ultra-low energy analog-to-digital converter (ADC) able to process single-ended and differential signals, with a flexible wide-range common-mode voltage is presented. This ability has been made possible through a novel track-and-hold (TH) circuitry, which provides a differential output with a fixed common mode voltage for the ADC, and relies on switched-capacitors technique for operation. The ADC is designed in a 90nm technology and simulated for both single-ended and differential inputs. The ADC consumes 13.25μW from a 1V source, while providing 6.86 and 7.95 effective bits, when acquiring single-ended and differential signals, respectively. The proposed technique contributes to improve power consumption and compactness, eliminating the requirements of a power-hungry amplifier and external components.

Keywords: ADC, ultra-low power, SAR, single-ended to differential conversion.

1. Introduction

A tight power budget is present in an ever increasing range of applications. New trends and emerging technologies often focus on miniaturization and portability, bringing devices which are mostly battery-powered. Therefore, in order to increase battery lifetime, every block in a system in this environment must consume the minimum possible energy.

One required circuit for a wide range of low-power applications is the analog-to-digital converter (ADC). Among the diversity of available topologies, the successive approximation register (SAR) is well-known for its energy efficiency. It is very attractive in applications which demand low data-rates, with tight power constraints, mainly due to the logarithmic dependence of architecture on the resolution. Based on a feedback loop, the SAR converter converges iteratively to the final digital word, comparing the value of a digital-to-analog converter (DAC) to a sampled representation of the input signal, captured by a track-and-hold (TH) circuit. The conversion cycle is guided by the binary search algorithm.

Conventional SAR ADCs rely on the charge redistribution (CR) method, so-called due to the DAC topology they employ. In this approach, the capacitive DAC is also used as tracking circuit, and at every step of the conversion, one of the binary-weighted capacitors is tied to ground or reference terminal, leading the error voltage to diminish towards zero.

In [1], the authors present a method to implement a capacitive SAR based on charge sharing (CS), rather than CR. As an advantage, the DAC is totally pre-charged once in the beginning of a conversion cycle, instead of per bit active interactions with the supply lines. Moreover, the settling requirements for DAC can be relaxed during design cycle, and most importantly, avoiding any power-hungry opamp buffering the reference signal. Misleadingly, this opamp is often not accounted for in the energy measurement of the CR converters, which could be significant.

Additionally, three common structures exist for the construction of ADCs: fully-differential input, pseudo-differential input, and single-ended (SE) input [2]. The input signal source (e.g. sensor) and the ADC structure must be consistent, imposing severe limitations on the choice of ADC in a given application. Performing the signal processing of the sampled signal, past the TH block, differentially presents some advantages over the single-ended processing, including increased noise rejection and dynamic range. However, most sensors and transducers only produce a single-ended output or a differential output with an incompatible common-mode (CM) voltage with that of the succeeding signal processing block. Traditionally, in order to match the signal types, designers have been relying on more complex coupling circuits, that may include electromagnetic transformers [3] or power-hungry programmable amplifiers [4].

We present a novel TH circuit that is able to maintain a desired stable CM voltage at its output, independent from the changes at the input CM voltage. This is a significant circuit design advantage when the TH is connected to a circuit block (e.g. comparator) that requires a stable CM voltage for its proper operation. Another advantage of these circuits is that it readily performs TH on both single-ended and differential voltage inputs, yet producing differential output around the desired output CM voltage.

This paper presents the design of a SAR ADC based on the CS principle, that employs the proposed novel TH. Thus, the ADC is very flexible in terms of input signal type, allow-

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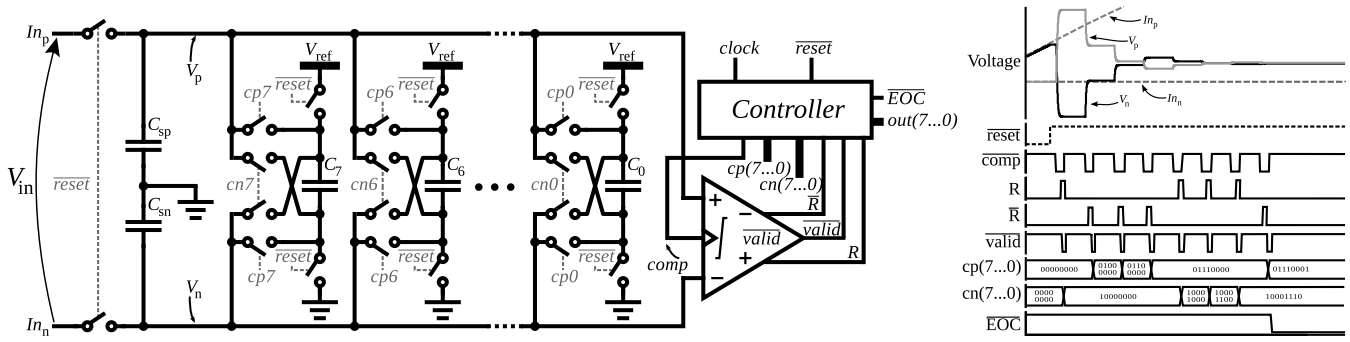

Figure 1: Charge Sharing ADC blocks diagram and illustrative waveforms

ing the conversion of signals coming from a wide range of sources, and yet eliminating the requirement of any matching circuitry.

Section 2 describes the ADC architecture. In Section 3 we present a background on TH circuits, the motivation for the proposed novel circuit, its topology derivation and implementation. In Section 4, we show in detail the circuit implementation of the remaining blocks of the ADC. The simulation results are presented in Section 5, and Section 6 finally concludes this work.

2. ADC Working Principle

The employed CS-based architecture comprises a controller, a comparator, a switched capacitor DAC and a TH circuitry, as depicted in Fig. 1. Moreover, the circuit is differential to increase noise tolerance and dynamic range [5].

A conversion cycle begins on the falling edge of the $\overline{reset}$ input. While this input is low, the TH circuit is tracking the input, and the DAC is being pre-charged. For the 8-bit converter, the DAC consists of 8 binary-weighted capacitors. During the pre-charge cycle, these capacitors are tied to reference voltage V_{ref}, and disconnected from TH capacitors and from each other. When $\overline{reset}$ is returned to high logic level, the input signal tracked on the TH is held steady, and DAC is disconnected from V_{ref}.

Next, the SAR circuit starts performing the binary search algorithm adding or subtracting charge to or from the sampling capacitors. Triggered by the logic controller, the comparator is requested to compare voltages V_{p} and V_{n}. The comparison result is the most significant bit (MSB) of the actual conversion. Subsequently, some charge must be added to or subtracted from these nodes, in order to make the voltage difference (error voltage) between V_{p} and V_{n} smaller. If, for instance, V_{p} is evaluated larger than V_{n}, we remove an MSB-equivalent (one half) amount of charge from sampling capacitors, by turning on control signal $cn7$. Therefore, capacitor C_7 would be connected anti-parallel to the capacitors of TH, C_{sp} and C_{sn}. If, on the other hand, V_{p} is smaller than V_{n}, the same amount of charge should be added placing C_7 in parallel to the sampling capacitances, by turning the control signal $cp7$ on. The process progressively repeats for the other bits, adding to or subtracting charge from the sampled charge from V_{in}. At the end, $cn(7...0)$ represents the desired 8-bit output.

3. Track and Hold Circuit

3.1. TH Background

Fig. 2 presents two operation phases of the $\overline{reset}$ signal in an ideal TH circuit. In the tracking phase, the circuit works like a closed switch, passing the input signal to the output, ideally not affecting it. During the hold phase, the magnitude of the input, captured in in the preceding phase, is kept steady until the next tracking phase. Also, during hold phase the circuit block that feeds from TH processes the sampled signal. An ideal TH has a zero output impedance, and an infinite input impedance.

In differential signaling, there are two quantities of primary interest (see Fig. 3). The first is the differential amplitude itself, that is given by

$$V_{\text{diff}} = V_{+} - V_{-} \tag{1}$$

where V_{+} and V_{-} are the analysed signal amplitudes.

The other quantity is the common-mode voltage V_{cm} which is the DC offset of the signal, or in other words, the mean amplitude of V_{+} and V_{-}, as given by

$$V_{\text{cm}} = \frac{V_{+} + V_{-}}{2}. \tag{2}$$

The CM voltage sets the operating point of the circuits. As an example, Fig. 4 shows the case where the TH feeds a comparator directly (e.g. 1-bit ADC). In this circuit the transconductance of the transistors in the differential pair at the comparator input, is set by the CM voltage of the TH circuit. The transconductance parameter determines some of the performance metrics of the comparator, such as speed, offset and

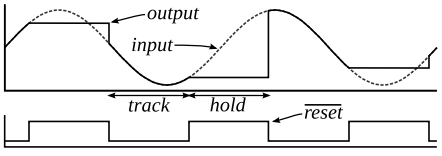

Figure 2: Working principle of a TH

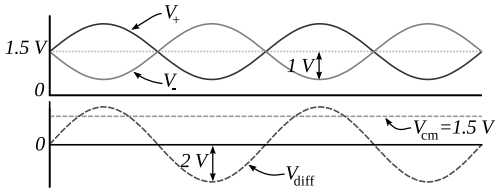

Figure 3: Decomposition of differential and common-mode levels in a differential signal

noise susceptibility [6, 7] and, therefore, should remain stable for every comparison.

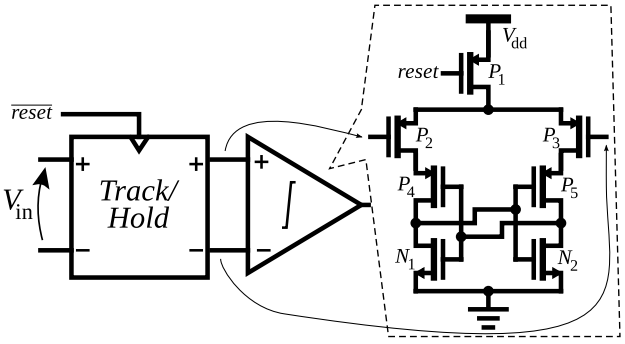

Figure 4: 1-bit ADC, made up of a TH and a comparator. The TH CM level sets the comparator input pair operating point and overall circuit characteristics

Hence, the designer has to carefully choose the CM amplitude and, what is probably more stringent, to ensure it remains stable to meet comparator requirement for the operating point. The problem has generally been downplayed, or ignored, in most of the recent published works on ADCs. The characterization is generally accomplished in a well-controlled environment, with close to ideal input sources and surrounding circuitry (e.g. a power-hungry amplifier with programmable CM to generate the required CM levels [4], or even a transformer [3]). The whole picture gets more complicated when the ADC is used whith not so well controlled input signals, specially in terms of CM levels.

3.2. TH Topology Derivation

From (2) the CM voltage of a differential signal is the arithmetic average of the differential inputs. Fig. 5 presents a very simple TH circuit with differential inputs (which can be made single-ended, by tying $V_{\text{in}-}$ to ground), and its associated waveforms. For the sake of clarity, for all plots in this section, we consider the $\overline{reset}$ signal to be permanently set low, and the circuits being in track phase. That means the output CM voltage also follows the input CM voltage.

For illustrating the point, in Fig. 5, the CM deliberately droops with time, while maintaining the same differential magnitude. The output CM voltage needs to stand stable independent of the variation in the input voltages (differential and CM). For V_{cm} to remain stable across the whole operating range of the TH we require a summing compensating CM voltage V_{com}, at every sampling cycle. An implementation of

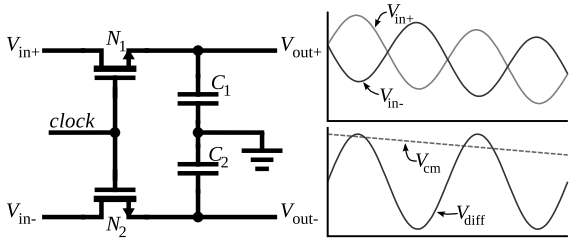

Figure 5: Simple TH for differential signals

the compensation scheme with ideal circuit element is shown in Fig. 6, with V_{com} inserted between C_1 and C_2.

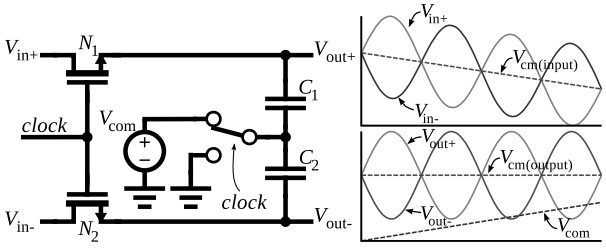

Figure 6: CM-adjustable TH

So, at every cycle, V_{com} is given by

$$V_{\text{com}} = V_{\text{cmS}} - \frac{V_{\text{in}+}}{2} - \frac{V_{\text{in}-}}{2} \tag{3}$$

where V_{cmS} is the desired CM voltage. The V_{com} voltage is a function of the sampled input, and thereof, is different for every TH cycle. Note that this leads to a differential output, even if the input is single-ended.

3.3. TH Circuit Implementation

In this section, we present the CMOS circuit implementation of the CM compensated TH in Fig. 6. The circuit is shown in Fig. 7, and is composed of a two-phase non-overlapping reset generator (shown separately in Fig. 8), transmission gates (TG), nMOS transistors and capacitors. The circuit works as follows. Initially, the reset phase ϕ_1 is high. Therefore, the capacitors C_3 and C_4 pre-charge to the voltages $V_{\text{cmS}} - V_{\text{in}+}$ and $V_{\text{cmS}} - V_{\text{in}-}$, respectively, through the the transmission gates TG_1, TG_2 and TG_4. The charges accumulated on capacitors C_3 and C_4 are given by (4) and (5), respectively.

$$Q_3 = C_3\,(V_{\text{cmS}} - V_{\text{in}+}) \tag{4}$$

$$Q_4 = C_4\,(V_{\text{cmS}} - V_{\text{in}-}) \tag{5}$$

Concurrently, the transistor N_5 ties the bottom plates of C_1 and C_2 to ground. Therefore, these capacitors track the input voltages $V_{\text{in}+}$ and $V_{\text{in}-}$. Note that the transistors N_1 and N_2 present a bootstrapping circuit (to be described later), in order to increase linearity.

In the next reset phase ϕ_2, N_5 turns off, disconnecting the node B from the ground. Also, the transmission gates TG_1 and TG_2 are turned off, while transistors N_3 and N_4 force the

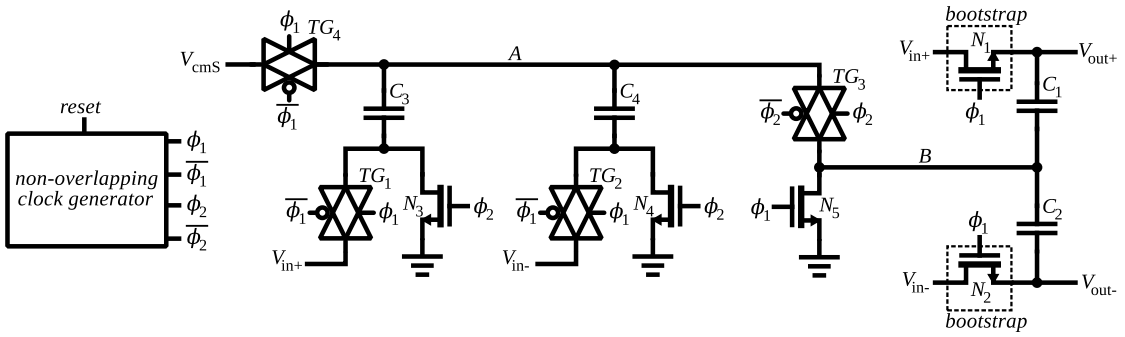

Figure 7: Proposed CM-adjustable CMOS circuit

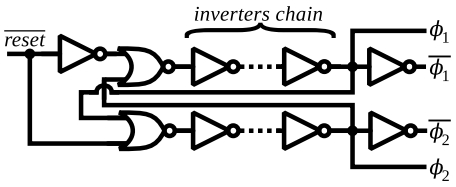

Figure 8: Non-overlapping reset signals generator

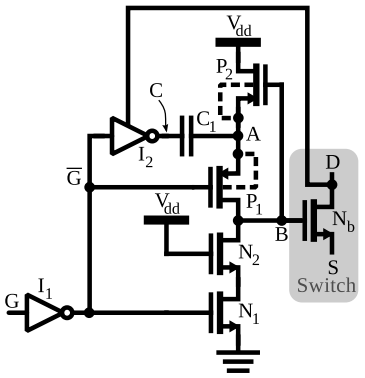

Figure 9: Proposed energy-efficient bootstrapping switch

voltages on the bottom plates of C_3 and C_4 to ground. TG_4 is also turned off, disconnecting node A from the voltage source V_{cmS}. On the other hand, TG_3 ties node B to node A. After this process, both $V_{\text{out+}}$ and $V_{\text{out-}}$ nodes experience an offset equal to the voltage on the node A, that we will derive next.

Since both the bottom plates of C_3 and C_4 are now tied together, we may consider them as a single capacitor with a total capacitance value of $C_3 + C_4$. Assuming $C_3 = C_4 = C$, the equivalent capacitance is $2C$. The voltage on node A is found solving

$$Q_{\text{tot}} = 2.C.V_{\text{A}} \tag{6}$$

where Q_{tot} is the total charge stored previously, during track cycle. We find the total charge summing Q_3 and Q_4, as

$$C_3\,(V_{\text{cmS}} - V_{\text{in+}}) + C_4\,(V_{\text{cmS}} - V_{\text{in-}}) = 2.C.V_{\text{A}}. \tag{7}$$

Setting $C_3 = C_4 = C$, leads to

$$V_{\text{A}} = V_{\text{cmS}} - \frac{V_{\text{in+}}}{2} - \frac{V_{\text{in-}}}{2}. \tag{8}$$

The voltage V_A is the same as in (3).

3.4. Bootstrapping Switch

The proposed switch is shown in Fig. 9. Differently from conventional implementations, the circuit has few components and does not need non-overlapped control phases. The inverter I_1 only works as a buffer and might be removed depending on the application. N_{b} is the bootstrapped nMOS switch, controlled by the voltage on node B, which has the same phase of the input G.

When G is at logic "0", the node $\overline{G}$ is at V_{dd}, turning transistor N_1 on, which in turn ties the output B to ground. When B is "0", the switch N_{b} is off. Concurrently, the inverter I_2 ties the bottom plate of capacitor C_1 to ground. The pMOS P_1 is kept off meanwhile, while P_2 charges C_1 to V_{dd}. Eventually, the circuit receives a logic "1" on its input, changing the voltage on $\overline{G}$ to zero. This turns off the transistor N_1, at the same time that the transistor P_1 is turned on, connecting the nodes A and B. The transistor N_2 avoids the drain-source voltage of N_1 to be higher than V_{dd}. As the voltage on node B raises towards V_{dd}, the transistor P_2 turns off, leaving the node A in high-impedance, since there is no direct current path to any of the supply terminals. The "0" on the input of the inverter I_2 forces the node C to V_{D}, which is the voltage on the drain of the bootstrapping transistor N_{b}, supplying I_2. Since A is in high-impedance, its voltage is increased to $V_{\text{dd}} + V_{\text{D}}$, because of the bootstrapping effect of capacitor C_1, and propagated through P_1 to the node B. Therefore, when the circuit input G is "1", the voltage at the gate of N_{b} is $V_{\text{dd}} + V_{\text{D}}$. Otherwise, if G is "0", the voltage at the gate of N_{b} is zero.

The circuit does not exhibit static current. The capacitor C_1 is never totally discharged and, for every cycle, it drains only the current necessary to replace the charge lost to the gate capacitance of N_{b} on the previous cycle and lost due to leakage. We simulated the bootstrapping circuit alone working at 5MHz (the maximum rating for the ADC) with minimum transistor sizes and C_1=125fF (metal-insulator-metal capacitor of 8μm × 8μm), and it consumes less than 100nW when driving a 2μm/90nm n-MOS.

3.5. TH Simulation Results

In order to confirm analytical derivations provided before, we simulated the TH circuit applying two different input sig-

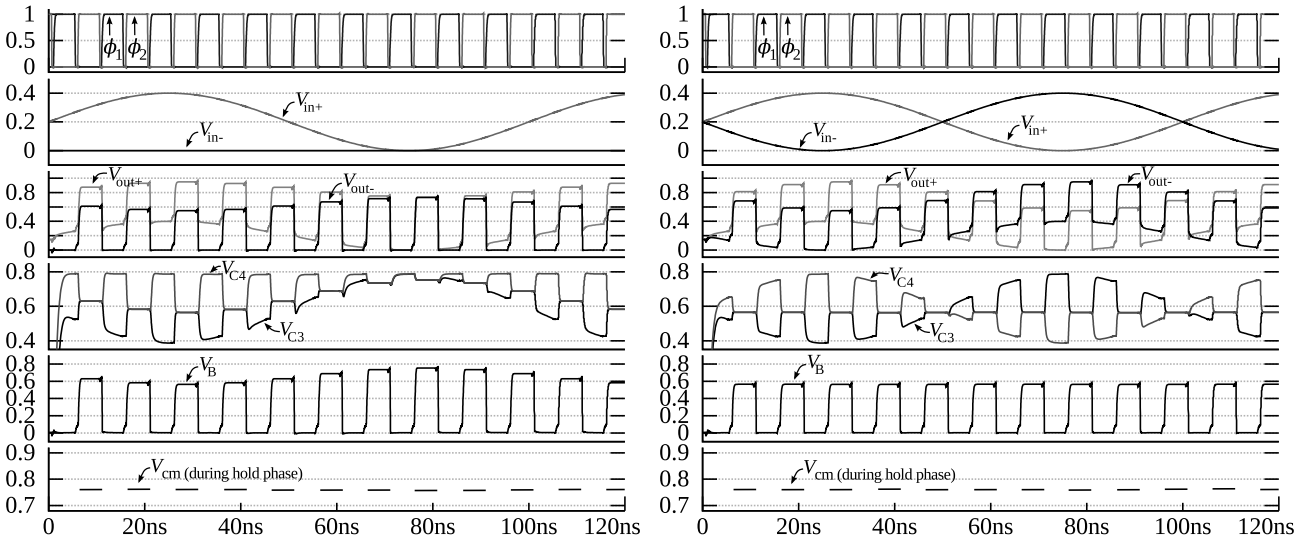

Figure 10: Simulation results for single-ended input/differential output, and differential input (CM=0.2)/differential output (CM=0.8).

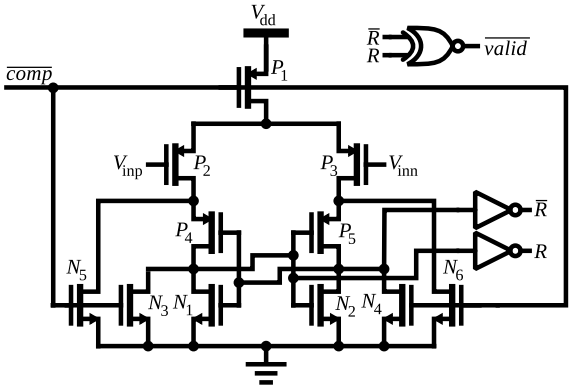

Figure 11: Dynamic regenerative comparator

nals: a single-ended signal, where the input V_{in-} is tied to ground, with a 0.4V sinusoid with 0.2V offset on the other terminal, and a differential 0.4V peek-to-peek sinusoid with 0.2V CM voltage. In both cases, the circuit is required to have a 0.8V CM output, setting V_{cmS} to this amplitude. The waveforms are shown in Fig. 10, for both cases. In the bottom part of the figure, we show the common-mode output level during the hold phase, which is very close to the desired 0.8V (approximately 0.76V and 0.77V for single-ended and differential, respectively). Also, we plot the voltage across capacitors C_3 and C_4, V_{C3} and V_{C4} and the voltage on node B, V_B, and input and output, as well.

4. ADC Circuit Implementation

In this section, we describe the working principle and the underlying design details of each one of the blocks inside the ADC.

4.1. Comparator

From the energy point of view, the comparator must consume very little or no power while not performing a comparison. The other requirements include a minimum offset, since the charge sharing SAR is much more sensitive to this non-ideality, as it manifests as non-linearity. Moreover, the noise will limit the size and power consumption of the comparator.

Different from other charge sharing designs ([1, 8, 9]), we decided against the inclusion of calibration feature for this ADC. The relative low data-rate (5 MSps) chosen as a design parameter enables us to accept larger devices on the comparator in order to increase the matching and, consequently, reduce offset. Trading off speed and matching, we get a standard deviation in the offset voltage σ_{offset} in the order of hundreds of micro volts. Fig. 11 shows the differential latched comparator topology, together with the comparator controller block.

4.2. Custom Controller

Most of the SAR ADCs reported to-date employ standard cell CMOS design methodology to implement the digital controller block. Some recent designs report the controller contribution to be responsible to roughly 50% of the overall ADC power [1, 10]. To significantly reduce energy, we design a custom controller for charge sharing ADC, based on [11]. It relies on true single phase clock (TSPC) latch, with embedded combinatorial logic. Moreover, we exploit the CMOS inherent parasitics to retain the control signals.

The proposed full-custom controller is composed of N slices (where N is the number of bits) and a comparator controller. For our 8-bit implementation, the schematic is shown in Fig. 12. In the figure we also show the other blocks of the complete ADC and their connections to the controller.

The controller was fully designed at transistor-level, and is based on the true single phase clock (TSPC) latch implementation. At the right side of Fig. 12 we show the circuit schematic of the logic slices. The arrangement of transistors N_1-N_6 and P_1-P_4 forms a TSPC latch with modified pull-up P_1-P_2 and pull-down N_2-N_5 combinatorial structures. Also, N_2 and N_3 parallel nMOS combination is added on the pull-

down network working towards comparison completion detection, allowing to discharge $\overline{next\_prep}$ exclusively after cp or cn are set.

The latch section feeds a differential regenerative stage that processes and keeps the comparison result, generating cp and cn control signal for every bit. This section of the circuit is triggered by the $\overline{valid}$ falling edge, implying a successful comparison. The complementary R and $\overline{R}$ signals come from the comparator, indicating the actual comparison result. The positive feedback provided in cp and cn nodes (transistors N_8 and N_9) avoids fluctuations on these nodes, that would exist because of the nodes high impedance in the following comparisons. The feedback arrangement does not drain static current. Every slice also generates the required signals responsible for triggering the subsequent slices.

The comparisons are properly required through the comparator controller circuit also shown in Fig. 12. The circuit drains no static current and has been implemented with custom logic. The ADC is made asynchronous improving the circuit presented in [11], thus no clock signal with a frequency multiple of the sampling frequency f_S is needed.

4.3. DAC

The DAC is made of 8 capacitors with binary-weighted values of capacitance, that are pre-charged to the reference voltage in the beginning of conversion cycle. During the conversion, the charges from these capacitances are added or subtracted to/from the sampled signal, following the binary search algorithm.

For this design, the capacitors mismatch is dominant over thermal noise, so unitary capacitors were dimensioned with differential non-linearity (DNL) constrained to $\sigma_{\mathrm{DNL}} < 0.2.V_{\mathrm{LSB}}$.

While the $\overline{reset}$ signal is low, the DAC capacitors C_7-C_0 are tied to V_{ref} through the switches on the bottom and top plates. The binary weighted relation is also kept for the n-MOS switches width. This weighting keeps the ADC immune to non-linearity caused by the charge injected into DAC capacitors while they are turning off. Since the injected charge from the transistor gate is a direct function of its area, it is beneficial to inject a charge proportional to the value of each capacitor, leading to the same voltage increase on every capacitor. It has the same effect of a constant offset on V_{ref} for every conversion, and it is naturally a linear process.

Different from the charge redistribution technique, once connected to the sampled input signal, capacitors are not disconnected until the end of conversion. Since there is no transistor turn-off during this period, there is also no charge-injection from cp and cn switches.

5. ADC Simulation Results

In order to estimate the ADC effective resolution and linearity performance, we simulated it in Cadence® Spectre® circuit simulator for different input cases:

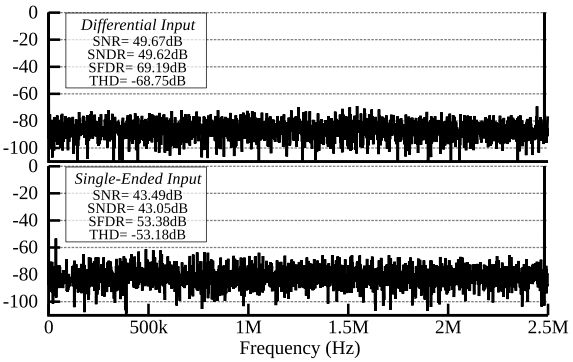

Figure 13: FFT plots at nearly Nyquist without and with transient noise

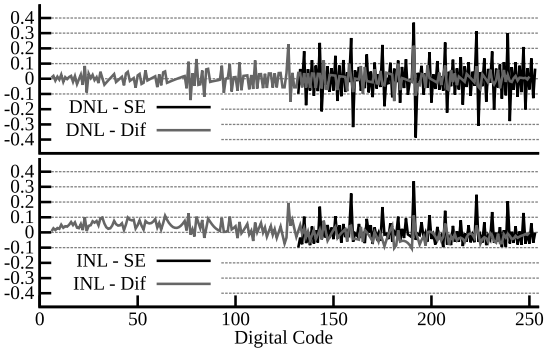

Figure 14: DNL and INL at nearly Nyquist

Single-Ended: a 480mV 2.48MHz input sinusoid is applied at the positive input, with 250mV DC offset; the negative input is tied to ground; the desired CM voltage is set to 250mV at the configurable TH;

Unmatched Differential: a 960mV 2.48MHz differential sinusoid with 500mV of CM (unmatched to 250mV CM required by the ADC) is applied to the ADC; the desired CM voltage is set to 250mV at the configurable TH.

Fig. 13 shows the FFT for both cases. When sampling an unmatched differential signal, the effective number of bits (ENOB) is 7.95-bit. However, when simulated with the single-ended input, the ADC presents a 6.86-effective number of bits. This may seem as a large performance degradation at the first glance, but the single-ended signal presents half the dynamic range of the differential signal. Thus, the input signal has also half the amplitude, which will decrease the signal-to-noise ratio (SNR) by a factor of two (or -6dB), leading to a 1-bit effective resolution loss, ideally.

The static performance of the ADC is shown through the DNL and integral non-linearity (INL) plots in Fig 14 for the same inputs. For the single-ended input, only digital codes in the larger half of the range occur, and DNL and INL plots make sense for the upper half interval only.

Consuming 13.25μW when sampling at 5MSps, the ADC has its power distributed among blocks as follows: DAC precharge 56.41%; TH (including input source current) 25.04%; digital controller 6.12%; comparator 12.43%. Fig 15 plots the energy dissipation in every sub-circuit during a complete

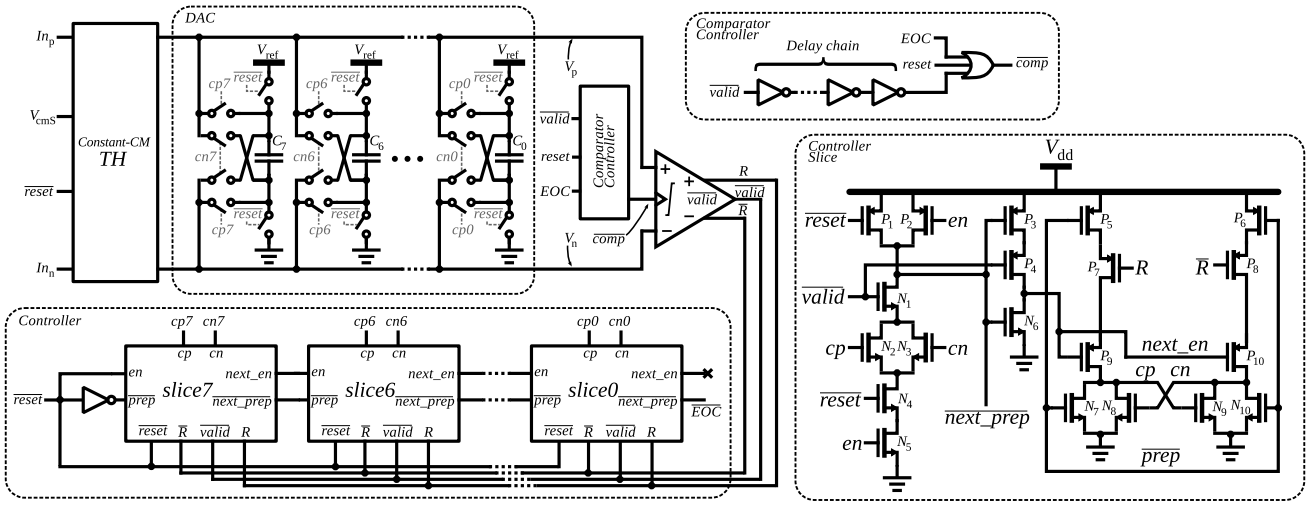

Figure 12: ADC schematic showing the SAR controller implementation

Table 1: Comparison with state-of-the-art ADCs

Parameter	[1]	[8]	[12]	[13]	[14]	[15]	[16]	[10]	[17]	This work [1]	This work [2]
Technology	90nm	90nm	180nm	90nm	40nm	180nm	65nm	90nm	65nm	90nm	90nm
Bits	9	9	8-9	6	8	10	5-10	10	8	8	8
ENOB	8.23	8.75	6.91	5.15	7.5	9.3	8.84	7.8	7.8	7.95	6.86
Samples/s	50M	40M	4.1k	1.5M	1.1M	100k	20k	1M	10M	5M	5M
Power	700μW	820μW	850nW	7μW	1.2μW	1.3μW	206nW	1.9μW	69μW	13.25μW	13.25μW
FOM($\frac{J}{conv.step}$)	65f	54f	1.72p	140f	6.3f	21f	22.4f	4.4f	30f	10.71f	22.81f

[1] with unmatched differential input [2] with single-ended input

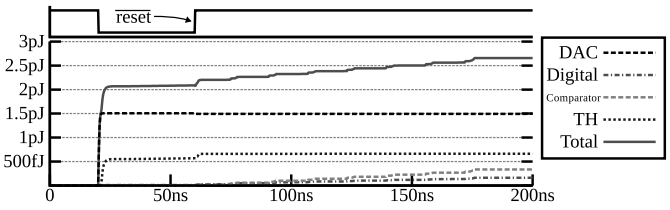

Figure 15: Energy consumption for a complete conversion

conversion cycle.

A commonly used figure of merit (FOM) relates power (P), sampling frequency (f_S) and ENOB as

$$\text{FOM} = \frac{P}{2^{\text{ENOB}} f_S}. \tag{9}$$

The proposed ADC achieves a FOM of 10.71fJ/conversion step sampling a unmatched differential input, and 22.81fJ/conversion step when sampling a SE input. Our design is compared to other state-of-the-art ADCs in Table 1.

6. Conclusion

In this paper we presented an ADC with the ability to process signals coming from a wide range of input sources, consuming only 13.25μW at 5MSps. Its design was only possible due to the novel ultra-low energy TH with auto-adjustable output CM voltage. The TH circuit has the ability to maintain a stable output CM voltage independent of the input CM, or the input being single-ended. The circuit analytical derivation, its implementation in CMOS, and corresponding simulations were presented. The use of the presented TH circuit avoids complicated coupling schemes between mismatched signals, including transformers and purpose-specific amplifiers. For the sake of comparison, the commercial single-ended to differential ADC driver referenced in [4] drains 4.8mA from a 5V supply, which leads to a power consumption that is more than 1800 times the total power consumption of our whole ADC working at full conversion speed.

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5 DISCUSSÃO

Neste trabalho, propomos técnicas de redução de consumo em conversores analógico-digitais por meio de inovações tanto em nível topológico como em nível de circuito.

A adaptação da técnica de escalonamento de tensão (já bastante conhecida no projeto de circuitos digitais) para os circuitos do ADC, apresentada no Capítulo 3, possibilita uma economia de energia de mais de 50% para o controlador digital. Isto decorre do fato de que a potência de chaveamento em circuitos digitais é reduzida com um fator quadrático à tensão de alimentação digital, e as potências de curto-circuito e de fuga são também significantemente reduzidas com o escalonamento desta tensão, porém seguem modelos mais complexos(RABAEY, 2009). Como foram empregadas tensões diferentes de alimentação analógica e digital e, por consequência, conversores de nível entre os domínios, o ADC não sofre com acréscimo de suscetibilidade ao ruído na parte analógica. No entanto, o emprego dessa técnica reduziu a frequência máxima de operação do ADC para 5MSps e requer fontes diferentes de alimentação para os domínios analógico e digital. Ainda no mesmo capítulo, apresentamos uma técnica de pré-carga iterativa que também possibilita redução no consumo de potência, ao preço de um número maior de fontes de alimentação e mais ciclos de relógio para uma conversão. Uma topologia de *track-and-hold*, que não sofre de redução de gama dinâmica como em (CRANINCKX; PLAS, 2007), também é apresentada.

No Capítulo 4, outras técnicas são apresentadas no projeto de um novo ADC por compartilhamento de carga. Um circuito de *track-and-hold* flexível em termos de sinal de entrada é empregado, oferecendo a habilidade de amostrar sinais *single-ended* ou diferenciais e convertê-los para um sinal diferencial com tensão de modo comum ajustável. Esse circuito facilita a instanciação do ADC em um sistema, uma vez que

evita a necessidade de circuitos de casamento entre o sinal de entrada e o ADC. Esse *track-and-hold* também apresenta um novo circuito de *bootstrapping* para as chaves, que ajuda o ADC a obter maior linearidade ao longo da gama dinâmica de entrada.

Neste trabalho também foram apresentadas três arquiteturas de circuito de controle digital para conversores SAR-CS. A primeira, apresentada no Capítulo 3, foi desenhada seguindo metodologia de *standard-cells*. A segunda, apresentada no Apêndice A e posteriormente usada no ADC apresentada no Apêndice B, foi desenhada em nível de transistores e otimizada para redução de potência. Ambas as topologias são síncronas, ou seja, têm o seu funcionamento baseado em um sinal de relógio. A terceira arquitetura, apresentada no Capítulo 4, é assíncrona e não necessita de sinal de relógio. O algoritmo é guiado por sinais inerentes ao ADC.

6 CONCLUSÃO

Este trabalho apresentou técnicas de redução de consumo em conversores analógico-digitais por aproximações sucessivas e compartilhamento de carga. Esta topologia é menos explorada que a sua similar por redistribuição de carga e as técnicas propostas ajudam a torná-la uma topologia mais competitiva em aplicações com restrições de potência limitantes. Para melhorar a eficiência energética destes ADCs, recorremos a inovações em nível arquitetural e nos sub-blocos.

As inovações propostas neste trabalho incluem três topologias de controlador digital para conversores SAR por compartilhamento de carga. Uma delas foi desenhada seguindo metodologia de *standard-cells*, enquanto as outras foram desenhadas a nível de transistores. Também apresentamos melhorias no circuito de *track-and-hold*, incluindo a amostragem com multiplexador analógico e dois circuitos de chave com *charge-pump*. Além disso, apresentamos uma metodologia e o circuito de *track-and-hold* correspondente para conversão de sinais *single-ended* em diferenciais. Este *track-and-hold* é também capaz de estabilizar a tensão de modo comum de saída, quando amostrando sinais já diferenciais. Um método de pré-carga iterativa do conversor digital-analógico também é descrito.

Por fim, foram apresentados três projetos de ADCs completos que recorrem a essas técnicas, cujos desempenhos encontram-se no estado-da-arte.

6.1 Sugestão de trabalho futuro

Todas as técnicas apresentadas aqui necessitam ser validadas em protótipos de circuito integrado, para garantir que nenhum aspecto importante de projeto foi desconsiderado durante a concepção destas mesmas técnicas. Mais, a técnica de pré-carga iterativa dos capacitores do DAC, apresentada no Capítulo 3, necessita de um circuito

que gere as tensões intermediárias internamente ao *chip* e que seja econômica em termos de potência.

APÊNDICE A ARTIGO III: A NOVEL ENERGY EFFICIENT DIGITAL CONTROLLER FOR CHARGE SHARING SUCCESSIVE APPROXIMATION ADC

RABUSKE, T. G.; RABUSKE, F. A.; RODRIGUES, C. R. A novel energy efficient digital controller for charge sharing successive approximation ADC. In: IEEE LATIN AMERICAN SYMPOSIUM ON CIRCUITS AND SYSTEMS (LASCAS), 2011. Bogotá, Colômbia. **Anais...** doi:10.1109/LASCAS.2011.5750295. 23-25 fev. 2011.

A Novel Energy Efficient Digital Controller for Charge Sharing Successive Approximation ADC

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***Abstract*—Successive approximation analog-to-digital converters are very attractive to power-constrained applications due to the topology inherent energy efficiency. This converter architecture most often relies on digital controller circuit to guide the conversion algorithm, and this controller is reported to have an important impact on the overall power consumption, sometimes demanding roughly half the total energy of a given ADC. Therefore, the design of an efficient controller must be of main concern in an ultra-low power ADC. In this paper we present a novel full-custom controller, based on true single phase clock latch, and provide simulation results. The proposed implementation achieves an extreme power reduction using only 13.4% of the energy of a standard cells implementation. We also propose a figure of merit (FOM) to controllers, and use it to compare our topology to a range of state-of-the art ADCs. According to this FOM, the proposed controller exhibits the smallest amount of energy per processed bit currently reported for SAR ADCs.**

I. Introduction

Ultra-low power consumption is a requirement for a wide range of integrated circuits including, but not limited to, sensor networks, medical aids and almost every battery-powered device. Moreover, the persisting reduction on the technologies minimum transistor channel length inversely increase the energy performance of digital circuits, due do decreased value of capacitance at the circuit nodes, extending the feasibility of the digital domain to signal processing, storing and controlling. However, the analog domain features more closely most of the physical events on nature. This context raises the need for interface circuits between both domains, so-called analog-to-digital converters (ADCs).

For low data rates, the successive approximation register (SAR) topology is a befitting solution to energy-efficient ADCs, due to its reduced amount of active analog circuitry, and logarithm dependence on resolution. The architecture converts a continuous analog waveform into a discrete digital representation running a binary search algorithm on a closed loop between the logic and a digital-to-analog converter (DAC). Fig. 1 shows the SAR topology. The most popular implementation of SAR ADC is called charge redistribution SAR, upon the DAC architecture it relies on.

The authors in [1] present a new SAR architecture, called charge sharing. It relies on a novel DAC operation principle, instead the usual charge redistribution. Among the advantages

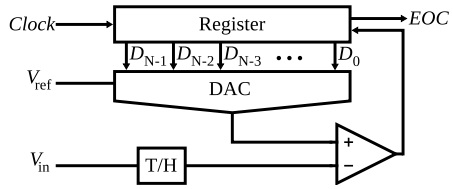

Fig. 1. SAR Topology Blocks Diagram

of this method is no need of neither low output impedance operational amplifiers on the input nor on the reference signal, reducing indirectly the power consumption. The architecture is explained on Section II.

To further reduce power consumption of charge sharing architecture, improvements must be made on each block of the ADC. This paper focus on increasing the logic controller efficiency. Some references report the controller to be responsible for around half of the total energy in a SAR ADC[1]–[3]. Hence, an extremely efficient control block has been designed, with full-custom methodology based on true single phase clock (TSPC) latches with combinational logic embedded. Moreover, we exploit the inherent circuit parasitics to store control signals.

To provide a proof-of-concept, we have designed a controller based on standard cells in a 180nm mature technology, and the proposed improved circuit in the same 180nm and in a 90nm later technology. The circuits were implemented employing higher threshold voltages V_T option on both n-MOS and p-MOS transistors, and this design choice is supported by our low-energy objective. Higher V_T leads to smaller short-circuit currents inherent to CMOS gates, with the price of a slower circuit operation. The implementations details are provided throughout Sections III and IV.

In Section V we present the simulations results. We also propose a figure of merit to compare SAR controllers efficiency, and plot the results of some leading edge ultra-low power converters to put our achievements into perspective. Section VI concludes this work.

II. Charge Sharing ADC

Similar to charge redistribution ADCs, the charge sharing based architecture requires a controller, a voltage comparator, and a DAC. However, due to its working principle, it also

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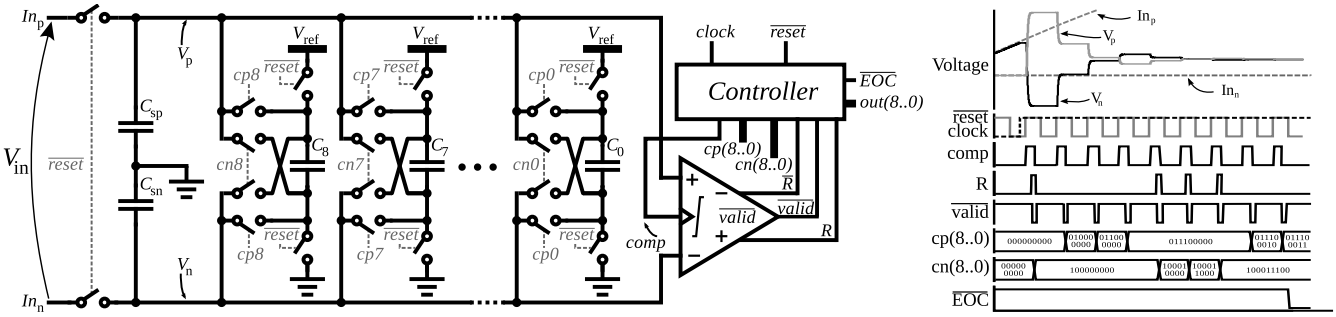

Fig. 2. Charge Sharing ADC blocks diagram and illustrative waveforms

requires a track and hold (T/H) circuitry, as the sampled signal cannot be held on the DAC capacitances. The topology is depicted in Fig. 2.

A conversion takes place on the falling edge of the $\overline{\text{reset}}$ input. While this input is low, the T/H circuit is tracking the input, whereas the DAC is being precharged. For the 9-bit converter described here, the DAC consists of 9 capacitors with binary-weighted values of charge. During the precharge cycle, these capacitances are tied to the reference voltage V_{ref}, and disconnected from T/H capacitors and from each other. When $\overline{\text{reset}}$ is returned to 1, the input signal tracked on T/H is held steady, and DAC is disconnected from V_{ref}.

Next, the SAR circuit starts performing the binary search algorithm, adding or subtracting charge to or from the sampling capacitors. On the next rising edge of the clock, comparator is initiated to compare voltages V_p and V_n. The comparison result is the most significant bit (MSB) of actual conversion. Subsequently, some charge must be added or subtracted on these nodes, in order to make the voltage difference (error voltage) between V_p and V_n smaller. If, for instance, V_p is evaluated larger than V_n, we remove an MSB-equivalent (one half) amount of charge from sampling capacitors, by turning on control signal *cn*8. Therefore, capacitor C_8 would be connected anti-parallel to the series arrange of C_{sp} and C_{sn}. If, on the other hand, V_p was smaller than V_n, the same amount of charge would be added placing C_8 in parallel to the sampling capacitances, by turning the control signal *cp*8 on. The process is repeated for the other bits, adding or subtracting charge to/from the sampled charge from V_{in}. At the end, *cn*(8...0) represents the desired 9-bit output.

III. Standard Cells Approach

The authors in [4] proposed a power efficient controller, based on standard cells. We have redesigned this controller towards energy optimization, but yet keeping the standard cells methodology. Also, our proposed controller is synchronous to a clock signal, unlike the cited paper. Along this section we explain the details of the gates-level implementation, since it is used as a reference model to our novel custom approach.

The controller relies on two registers, where their widths are equal to the ADC number of bits. A few combinational gates fulfill the circuit schematic, that is shown in Fig. 3.

The controller guides the conversion as follows: After reset ($\overline{reset}$ signal is released back to high logic level), the *clock*

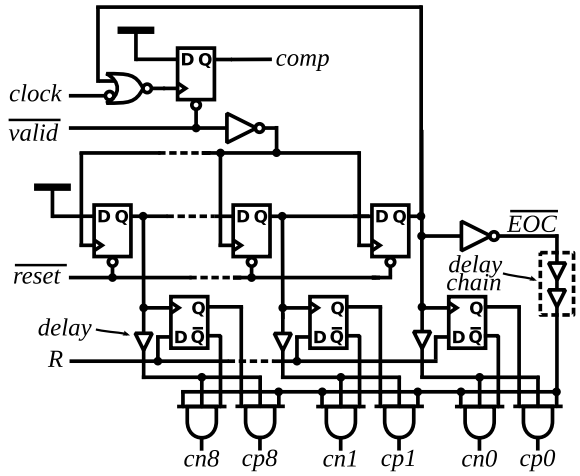

Fig. 3. Standard cells proposed circuit

positive edge triggers *comp* signal, requesting a comparison from the comparator. After a successful comparison result, the $\overline{valid}$ signal is pulled down by the comparator, and it leads to a pair of parallel logic tasks. First, the *comp* signal is reset to zero. Second, $\overline{valid}$ is inverted and the result feeds the clock of the top shift-register. This causes the shift-register to be shifted right and the most significant bit (MSB) is set to 1. After, one of the flip-flops on the lower chain retains the comparator result *R*. This must happen before the comparator output is reset to initial state and, depending on the standard cells library, a small delay is required in order to assure the flip-flop setup time. Two 3-input AND-gates assure that *cp* and *cn* signals are updated and kept for the proper period of time, avoiding them to be on during the reset and DAC precharge cycle. Moreover, delay cells were added along some logic paths, to avoid overlapping on control signals, that would lead to overall ADC non-linearities.

In order to decrease the power consumption, the controller was manually designed in gate level, and this approach proved to have better results than with a logic synthesizer software. We implemented this circuit in a 180nm technology, and the simulation results are exhibited in Section V.

IV. Full-Custom Approach

The proposed full-custom controller is composed of *N* slices (where *N* is the number of bits) and a comparator controller. For our 9-bit implementation, the blocks diagram is shown

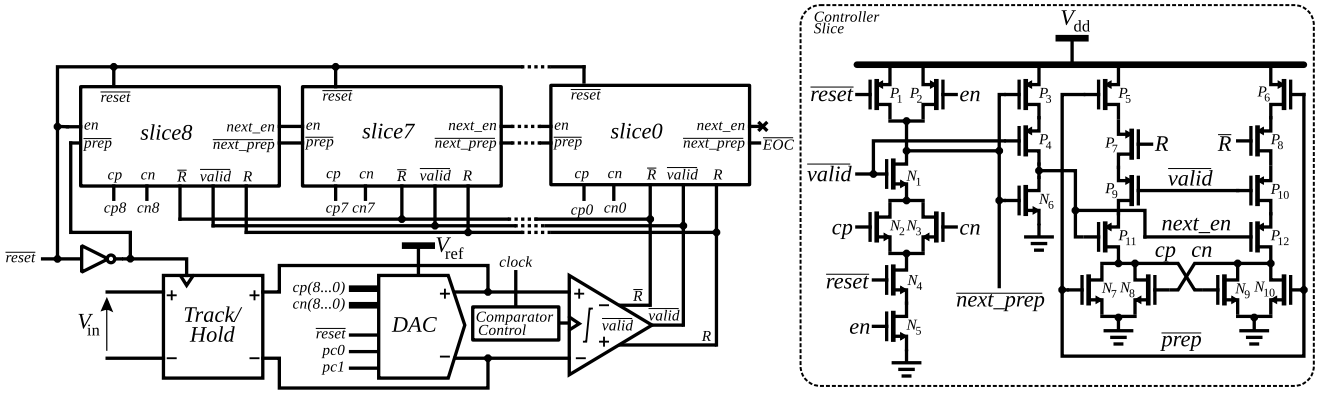

Fig. 4. Logic blocks diagram and custom controller slice circuit schematic

in Fig. 4. In the figure we also show the other blocks of a complete ADC and their connections to the controller.

The controller was fully designed at transistor-level, and is based on the true single phase clock (TSPC) latch implementation. At the right side of Fig. 4 we show the circuit schematic of the logic slices. The arrangement of transistors N_1-N_6 and P_1-P_4 forms a TSPC latch with modified pull-up P_1-P_2 and pull-down N_2-N_5 combinatorial structures. Also, N_2 and N_3 parallel n-MOS combination is added on the pull-down network working towards comparison completion detection, allowing to discharge $\overline{next\_prep}$ exclusively after cp or cn are set.

The latch section feeds a differential regenerative stage that processes and keeps the comparison result, generating cp and cn control signal for every bit. This section of the circuit is triggered by the $\overline{valid}$ falling edge, implying a successful comparison. The complimentary R and $\overline{R}$ signals come from the comparator, indicating the actual comparison result. The positive feedback provided in cp and cn nodes (transistors N_8 and N_9) avoids fluctuations on these nodes, that would exist because of the nodes high impedance in the following comparisons. The feedback arrangement does not drain static current. Every slice also generates the required signals responsible to trigger the subsequent slices.

The comparisons are properly required through the circuit shown in Fig. 5, based on the clock signal. The simple proposed circuit avoid comparisons during the reset phase. Moreover, comparisons are not done when the converter is idle. The imposed limitations avoid worthless comparisons throughout the conversion cycle.

The proposed circuit has been simulated in the same 180nm technology referred before, in order to fairly compare performance of both standard-cells and full-custom architectures. Also, we had designed the full-custom circuit in a modern 90nm channel length technology to compare simulation results to state-of-the-art designs.

V. Simulation Results

We have performed simulations with both standard cells and full-custom architectures in order to extract performance parameters. In both cases, the simulations were performed in transistors level, using a commercial Spice simulator.

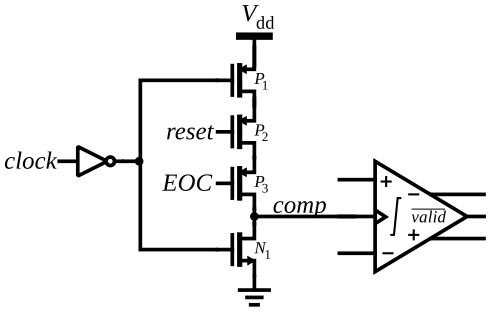

Fig. 5. Comparator activation circuit

Both controller topologies were tested inside a validated charge-sharing ADC. The employment of a well-proven ADC as the simulation environment avoids wrong assumptions regarding the operation, that would mislead to erroneous performance metrics. Both approaches show exactly the same logic behavior as the validated ADC golden model controller. The equivalence persists over all extensive analyses, under all covered situations. The parasitics were not accounted for any case.

Table I summarizes the results for both topologies. We show the controller average power consumption for a 1MSps sampling rate, and the energy needed for the full conversion cycle as well. Our novel full-custom circuit performs the same functionality using just 13.4% of the energy consumed by the standard cells version in the same technology.

Another indirect improvement of our novel approach is the reduced number of transistors in the controller block, that is more than 4 times smaller than employing standard-cells. A consequence of using reduced number of transistors in the controller is a reduction on propagation delays along the logic paths, yielding to a faster circuit operation. Moreover, it leads to a diminished simulation time, when using circuit-level analysis. In Table I we show the simulation time in transistors-level normalized to a full conversion cycle.

In order to reliably compare performance parameters to other designs, we introduce a figure of merit (FOM) for SAR logic controllers.

The contribution of a controller on the energy consumption of a given SAR ADC can be characterized as in (1), where α is the fraction of total ADC power drained by the controller,

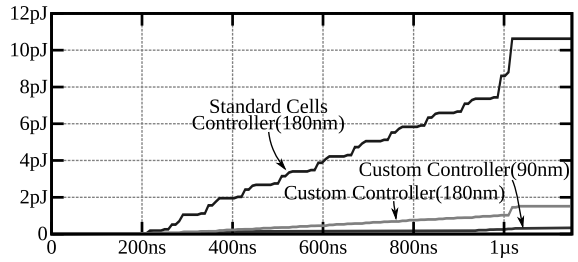

Fig. 6. Energy versus time plot for both logic approaches, for one 9-bit conversion.

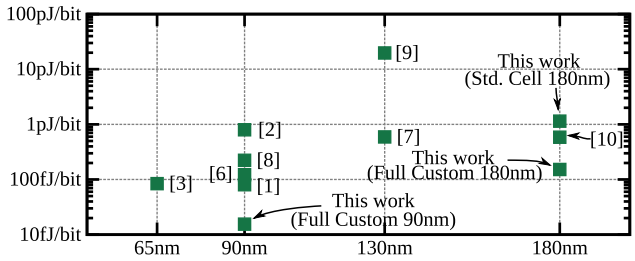

Fig. 7. Energy per bit of controllers in state-of-the-art ADC as a function of technology node

TABLE I
COMPARING STANDARD CELLS (SC) AND FULL CUSTOM (FC) PROPOSED CIRCUITS

Parameter	SC(180nm)	FC(180nm)	FC(90nm)
Power consumption@1MSps	10.2μW	1.37μW	140nW
Energy per 9-bit cycle	10.2pJ	1.37pJ	140fJ
Transistors	852	208	208
Simulation time per cycle	2min 36sec	32sec	32sec

and E_{ADC} is the energy needed per conversion sample.

$$E_{\text{controller}} = \alpha . E_{\text{ADC}} \tag{1}$$

If the static power, ofter related to leakage current, is neglected, E_{ADC} is given by (2), where P is the total ADC power and F_s is the sampling rate.

$$E_{\text{ADC}} = \frac{P}{F_s} \tag{2}$$

The energy of a CMOS digital circuit is a direct function of the switching activity, needed to charge or discharge the load capacitances. Therefore, once again neglecting leakage currents, the controller total dissipated energy for a complete conversion of N bits is a linear function of N. Based on this relation, we propose a figure of merit for SAR controllers, that relates the total controller energy normalized for the N number of bits of a given conversion. So, the energy per bit is given by (3), expressed in Joules per bit.

$$\text{FOM}_{\text{controller}} = \frac{E_{\text{controller}}}{N} \tag{3}$$

To put both approaches in perspective to other state-of-the-art similar designs, we show in Fig. 7 a plot of FOM for logic controllers in some recent papers, as a function of technology node. All the designs plotted does not count on digital calibration circuitry, that would probably increase the controller power consumption. The figure relates the proposed FOM for a range of 6 to 12-bit state-of-the art calibration-less SAR converters.

VI. CONCLUSIONS

Throughout this paper we have presented the concept and design of a novel controller architecture for charge sharing successive approximation ADCs. Also, a standard-cells implementation of a logic-equivalent controller is proposed to provide a reference energy value. An energy reduction of more than 7 times is achieved in the custom controller over the standard-cells controller. In order to provide reliable comparisons to leading edge ultra-low power SAR ADCs, we derived a figure of merit specific to SAR controllers. We contrasted our simulation results using this FOM to other state-of-the-art designs in the field of ultra-low power ADCs. When comparing our FOM results to the reference papers, we proved to have the most energy efficient SAR logic controller currently reported.

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APÊNDICE B ARTIGO IV: AN ENERGY-EFFICIENT 1MSps 7μW 11.9fJ/CONVERSION STEP 7pJ/SAMPLE 10-BIT SAR ADC IN 90nm

RABUSKE, T. G.; RODRIGUES, C. R.; NOOSHABADI, S. An energy-efficient 1MSps 7μW 11.9 fJ/conversion step 7pJ/sample 10-bit SAR ADC in 90nm. In: IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS (ISCAS), 2011. Rio de Janeiro. **Anais..** doi:10.1109/ISCAS.2011.5937551. 15-18 maio 2011.

An Energy-Efficient 1MSps 7μW 11.9fJ/conversion step 7pJ/sample 10-bit SAR ADC in 90nm

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***Abstract*—Current trends constantly increase the need for ultra-low power solutions for embedded and portable hardware. One circuit component required in a wide range of devices is the analog-to-digital converter (ADC). In this paper we propose an extremely energy-efficient successive approximation register (SAR) ADC, in which we have overcome the limitations of conventional approaches through topological improvements. Further advances include the implementation of a custom controller and a novel bootstrapped track and hold (T/H) circuitry. Statistical simulations indicate an ADC with a figure of merit (FOM) of 11.9 fJ per conversion step, and an effective number of bits (ENOB) of 9.2, operating close to Nyquist frequency, sampling at 1 Msps. To put it into perspective, consuming only 7 pJ/sample, this ADC is able to work at its maximum speed for more than 40 years with the total energy of a single alkaline AA battery.**

I. Introduction

A tight power budget is present in an ever increasing range of applications. New trends and emerging technologies often focus on miniaturization and portability, bringing devices which are mostly battery-powered. Therefore, in order to increase battery lifetime, every block in a system in this environment must consume the minimum possible energy.

One required circuit for a wide range of low-power applications is the analog-to-digital converter (ADC). Among the diversity of available topologies, the successive approximation register (SAR) is well-known for its energy efficiency. It is very attractive in applications which demand low data-rates, with tight power constraints, mainly due to the logarithmic dependence of architecture on the resolution.

Based on a feedback loop, the SAR converter converges iteratively to the final digital word, comparing the value of a digital-to-analog converter (DAC) to a sampled representation of the input signal, captured with a track and hold (T/H) circuit. The conversion cycle is guided by the binary search algorithm.

Conventional SAR ADCs rely on the charge redistribution (CR) method, so-called due to the DAC topology they employ. In that approach, the capacitive DAC is also used as tracking circuit, and at every step, one of the binary-weighted capacitors is tied to ground or reference terminal, leading the error voltage to diminish towards zero.

In the inspiring work in [1], authors present a method to implement capacitive SAR based on charge sharing (CS), rather than charge redistribution. As an advantage, the DAC is totally precharged once in the beginning of a conversion cycle, instead of per bit active interactions with the supply lines. Still, the settling requirements for DAC can be relaxed during design cycle, and most importantly, avoiding any power-hungry opamp buffering the reference signal. Misleadingly, this opamp is often not accounted for in the energy measurement of a given converter, which could be significant.

In this paper we implement a 10-bit charge sharing ADC, with topological improvements over the reference paper in [1]. Its operation is described in Section II. Furthermore, we have improved the inner circuit blocks. A modified T/H circuitry is proposed, employing bootstrapped switches to achieve the linearity required for the 10-bit ADC. In this paper we have significantly decreased the contribution of digital controller to the overall energy by taking an extremely efficient custom approach to logic design based on true single phase clock (TSPC) latches with embedded combinational logic and taking advantage of inherent parasitics to retain control signals. The complete description of each circuit block, with additional information on their implementation is presented in Section III. In order to validate the ADC and extract the reliable circuit parameters, we carried out statistical simulations. The simulation environment and procedures with the achieved results are expounded in Section IV. Conclusions are drawn in Section V.

II. Operation Principle

Similar to charge redistribution ADCs, the charge sharing based architecture requires a controller, a voltage comparator, and a DAC. However, due to its working principle, it also requires a track and hold circuitry, as the sampled signal cannot be held on the DAC capacitances. The topology is depicted in Fig. 1.

A conversion takes place on the falling edge of the $\overline{\text{reset}}$ input. While this input is low, the T/H circuit is tracking the input, whereas the DAC is being precharged. For the 10-bit converter described here, the DAC consists of 10 capacitors with binary-weighted values of charge. During the precharge cycle, these capacitances are tied to reference voltage V_{ref}, and disconnected from T/H capacitors and each other. When $\overline{\text{reset}}$

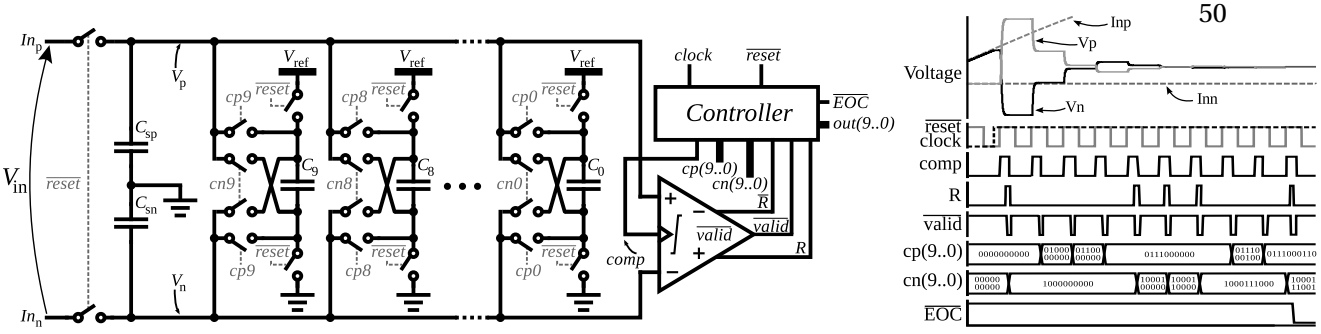

Fig. 1. ADC blocks diagram and illustrative waveforms

is returned to high logic level, the input signal tracked on T/H is held steady, and DAC is disconnected from V_{ref}.

Next, the SAR circuit starts performing the binary search algorithm adding or subtracting charge to or from the sampling capacitors. On the next rising edge of the clock, comparator is initiated to compare voltages V_p and V_n. The comparison result is the most significant bit (MSB) of actual conversion. Subsequently, some charge must be added or subtracted on these nodes, in order to make the voltage difference (error voltage) between V_p and V_n smaller. If, for instance, V_p is evaluated larger than V_n, we remove an MSB-equivalent (one half) amount of charge from sampling capacitors, by turning on control signal *cn*9. Therefore, capacitor C_9 would be connected anti-parallel to the series arrange of C_{sp} and C_{sn}. If, on the other hand, V_p was smaller than V_n, the same amount of charge would be added C_9 by being placed in parallel to the sampling capacitances, by turning the control signal *cp*9 on. The process progressively repeats for the other bits, adding or subtracting charge to/from the sampled charge from V_{in}. At the end, *cn*(9...0) represents the desired 10-bit output.

III. Circuits

In this section, we describe the working principle and the underlying design details of each one of the blocks inside the ADC.

A. Track and Hold

The power consumption of T/H circuit must be compatible to a low-energy design. Despite of the fact that some complex T/H topologies had been explored for charge sharing ADC ([1]–[3]), a very efficient approach is the simple arrangement of MOS switch and capacitor, shown in Fig. 2. Apart from the increased energy efficiency and reduced complexity, this circuit does not reduce the signal to noise ratio (SNR) during charge processing because it does not divide the input sampled voltage by a factor of 2, as is the case in [1]. The employment of this simple circuit means no current is drawn from the input signal when the ADC is not effectively tracking the input. This is different from the cited approaches, where there is always one set of capacitors sampling the input and, therefore, consuming power. To avoid the use of a low-impedance buffer on the input, the tracking time can be adjusted to march the input signal strength, by changing the time the signal $\overline{reset}$ is kept low.

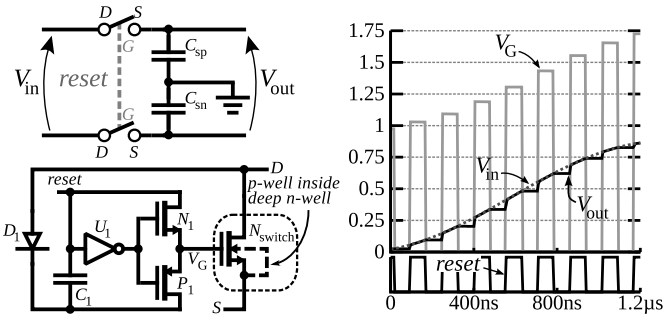

Fig. 2. Charge pump proposed switch

The 10-bit resolution chosen for this ADC imposes stringent linearity constraints on the T/H, as the overall ADC linearity is dependent on the T/H linearity. Therefore, in order to meet the fundamental linearity constraints for 10-bit resolution, we have employed a novel bootstrapped switch, based on [4], as shown in Fig. 2.

When signal *reset* is low, capacitor C_1 is precharged to the drain voltage V_D minus diode D_1 forward-biased voltage drop. Because of inverter U_1, n-MOS N_1 is turned on, transferring the zero voltage signal *reset* to the gate of N_{switch}, therefore, turning this switch off. If, on the other hand, *reset* signal is high, the inverter U_1 outputs zero voltage, turning P_1 on. As a result, P_1 delivers the sum of previously charged C_1 and *reset* node voltages ($V_{C_1} + V_{reset}$). The process is shown in Fig. 2. In order to avoid channel modulation effect and its impact on linearity, we have employed p-well inside a deep n-well for N_{switch} and tied its bulk and source together.

Simulations of the T/H circuitry, with the bootstrapping through the simple arrangement of MOS switch and capacitor, show that it presents a signal to noise and distortion ratio (SNDR) of around 74 dB. This corresponds to around 12 effective bits, giving the design some safety margin.

B. DAC

The DAC consists of 10 capacitors, that are precharged to binary-weighted values of charge in the beginning of conversion cycle. During the conversion, these charge values are added or subtracted to/from the sampled signal, in order to realize binary search algorithm. The circuit, with charge sharing switches *cn*(9...0) and *cp*(9...0) omitted, is shown in Fig. 3.

For this specific design, the capacitors mismatch is dominant over thermal noise, so unitary capacitor were dimensioned to

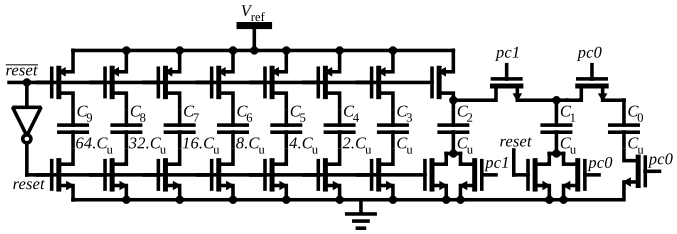

Fig. 3. DAC Circuit Schematic

fulfill linearity constraints. However, for the 10-bit accuracy keeping $\sigma_{\text{DNL}} < 0.2$, the unit capacitance is smaller than the minimum size metal-metal capacitor design rule for the technology. To overcome this limitation, we kept the charge proportionality on the least significant bits (LSBs) by first precharging C_2 to V_{ref} and than redistributing its charge to C_1 and C_0, iteratively. This sharing on LSBs happens concurrently to conversion, and does not require extra clock periods.

While the $\overline{\text{reset}}$ signal is low, the DAC remaining capacitors $C_9 - C_3$ are tied to V_{ref} through n-MOS and p-MOS transistors on the bottom and top plates, respectively. The binary weighted relation is also kept for the transistors width. Doing so, the charge-injection on the DAC capacitors, when these transistors are turned off, does not lead to non-linearities in the ADC. Since the injected charge from the transistor gate is a direct function of its area, it is beneficial to inject a charge proportional to the value of each capacitor, leading to the same voltage increase on every capacitor. It has the same effect of a constant offset on V_{ref} for every conversion, and it is naturally a linear process.

The charge sharing switches ($cn(9...0)$ and $cp(9...0)$), are implemented using transmission gates, to decrease their resistance over the full signal range. Different from the charge redistribution technique, once connected to the sampled input signal, capacitors are not disconnected until the end of conversion. Since there is no transistor turn-off during this period, there is also no charge-injection from cp and cn transistors.

C. Comparator

From the energy point of view, the comparator must consume very little or no power while not performing a comparison. The other requirements include a minimum offset, since the charge sharing SAR is much more sensitive to this non-ideality, as it manifests as non-linearity. Moreover, the noise will limit the size and power consumption of the comparator.

Different from other charge sharing designs ([1]–[3]), we decided against the inclusion of calibration feature for this ADC. The relative low data-rate chosen as a design parameter enables us to accept larger devices on the comparator in order to increase the matching and, consequently, reduce offset. Trading off speed and matching, we get an standard deviation in the offset voltage σ_{offset} in the micro volts range. Fig. 4 shows the differential latched comparator topology, together with the comparator controller block.

D. Custom Controller

Most of the SAR ADCs reported to-date the employ standard cell CMOS design methodology to implement the digital

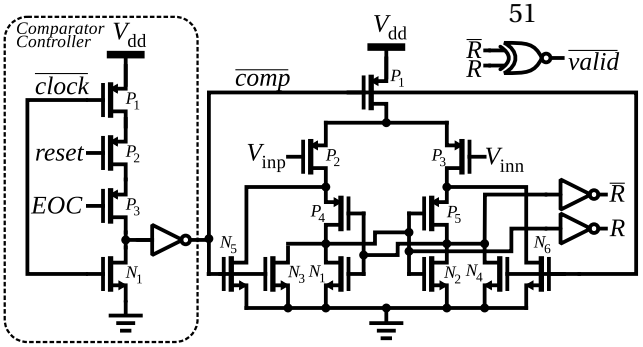

Fig. 4. Comparator circuit

controller block. Some recent designs report the controller contribution to be responsible to roughly 50% of the overall ADC power [1], [5]. To significantly reduce energy, we propose a novel custom controller for charge sharing ADC. It relies on true single phase clock (TSPC) latch, with embedded combinatorial logic. Moreover, we exploit the CMOS inherent parasitics to retain the control signals. Full-custom logic controller has already been used in SAR ADCs, like in [6].

The controller is composed of 10 identical slices, as shown in Fig. 5. The circuit drains no static current and has been implemented with high threshold low leakage transistors. Also notice that even though the proposed ADC is synchronous, the controller does not depend on the clock signal. Therefore, the same circuit may be employed without any adaption in an asynchronous ADC. In that case, the only modifications should be made to the comparator, changing the way it is activated; based on the clock signal for our design, or based on certain delay after a valid comparison for the asynchronous alternative.

IV. Simulation Results

In order to compensate for the absence of a prototype chip and extract reliable results, we have employed extensive Monte-Carlo (MC) simulations. This was only feasible due to the reduced number of transistors in the controller logic block, when compared to standard logic approach employed in other designs. Using the full-custom controller the time required to run a 512 points transient analysis with transient noise was around 2.5 hours on an 8-core processor machine. For every run (30 random seeds) in the Monte Carlo simulation, the important parameters were extracted, and their mean and standard deviation calculated. Average effective number of bits (ENOB) and its standard deviation for different sinusoidal inputs along the frequency range of the converter are plotted in Fig. 6.

Unfortunately, the converter has some performance degradation in higher range of frequencies. The linearity loss is caused by the track and hold circuit, that is not able to respond well on low duty-cycles. Fig. 7 shows an FFT plot for the ADC for a 41 kHz 1 V peak to peak signal.

Regarding the power consumption, sampling at 1 MSps, the converter consumes 7 μW from a 1 V supply source. The power distribution among the blocks is as follows; comparator 2.4%, controller 2%, T/H circuit 1.4%, DAC precharge 94.2%.

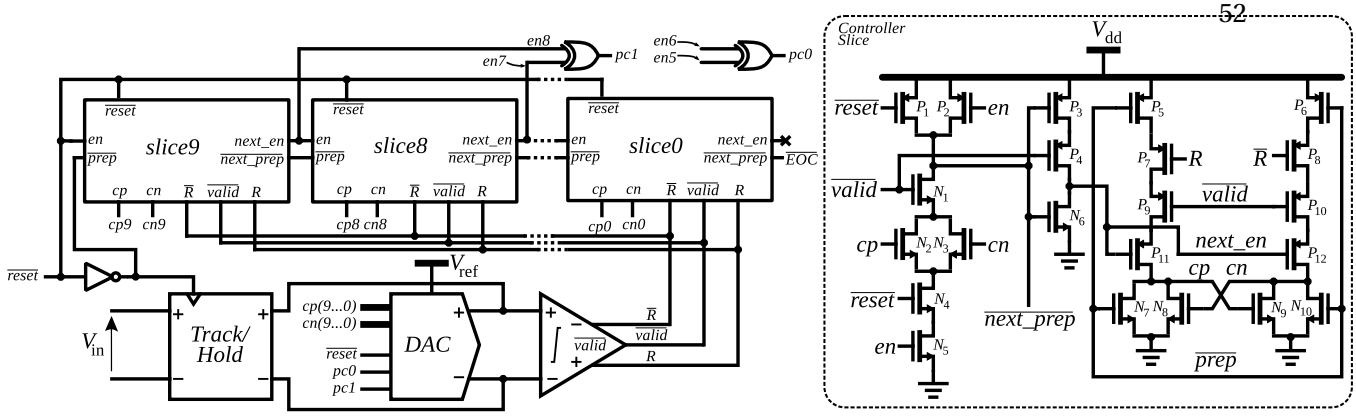

Fig. 5. Logic blocks diagram and custom controller slice circuit schematic

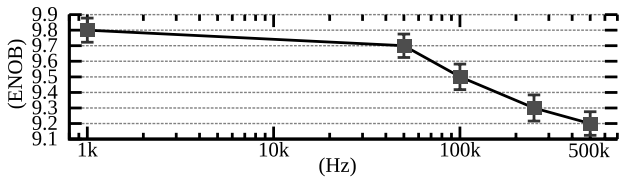

Fig. 6. ENOB mean and standard deviation as a function of input frequency

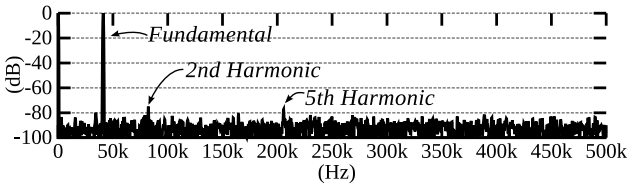

Fig. 7. FFT Plot with harmonics for a 41 kHz input signal

It is important to consider that parasitics were not accounted in the simulation, and the power consumption may increase slightly in the physical design. Fig. 8 shows the energy dissipated by each one of the circuit blocks during a complete conversion cycle, within 1 μs. The energy needed to precharge the DAC by far surpasses the other blocks energy.

A commonly used figure of merit (FOM), is defined as,

$$\text{FOM} = \frac{P}{2^{\text{ENOB}} F_s} \tag{1}$$

where P is total power and F_s the sampling frequency. Using (1), the proposed ADC achieved a FOM of 11.9 fJ/conv. step, with the 9.2-bit ENOB at nearly Nyquist frequency. We compare our design to other state-of-the art ADCs in Table I.

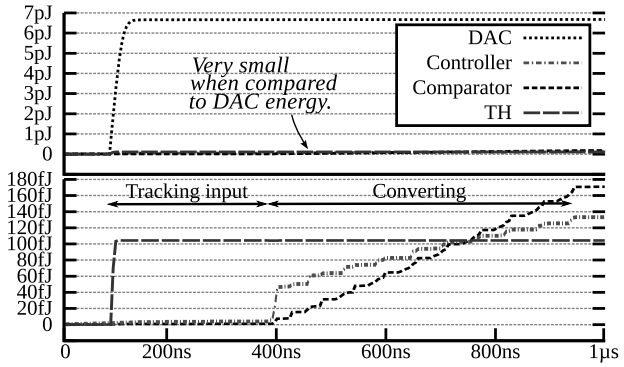

Fig. 8. Energy versus time for each circuit block in the ADC

TABLE I
COMPARISON WITH STATE-OF-THE-ART DESIGNS

Parameter	[1]	[2]	[5]	[6]	This work
Technology	90nm	90nm	65nm	90nm	90nm
Bits	9	9	10	8	10
ENOB	7.8	8.23	8.75	7.8	9.2
Samples/s	50M	40M	1M	10M	1M
Power(μW)	700	820	1.9	69	7
FOM($\frac{J}{conv.step}$)	65f	54f	4.4f	30f	11.9f

V. Conclusions

In this paper, we successfully designed a state-of-the art ADC with extreme energy efficiency. The results place this design in the leading edge of ultra-low energy ADCs.

To illustrate the power scale, we compare the energy necessary for a single conversion of the ADC to the amount of energy available in a conventional AA alkaline battery [7]. Working at full 1 MSps speed, the converter is theoretically able to work for 40 years with 9000 Joules.

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APÊNDICE C ARTIGO V: A TRACK AND HOLD FOR SINGLE-ENDED OR DIFFERENTIAL INPUT WITH ADJUSTABLE OUTPUT COMMON MODE

RABUSKE, T. G.; RODRIGUES, C. R.; NOOSHABADI, S. A track and hold for single-ended or differential input with adjustable output common mode. IEEE INTERNATIONAL MIDWEST SYMPOSIUM ON CIRCUITS AND SYSTEMS (MWSCAS), 2011. Seul, Coréia do Sul. **Anais...** doi:10.1109/MWSCAS.2011.6026456. 7-10 ago. 2011.

A Track and Hold for Single-Ended or Differential Input with Adjustable Output Common Mode

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***Abstract*—A novel differential output track and hold (TH) circuit with configurable common-mode output voltage is presented. Its structure avoids the coupling circuits required when dealing with different common-mode levels in differential signals. Another novelty of the proposed design is its ability to track single-ended signals, and convert the output to a steady differential voltage, with a programmable common-mode level. The solution employs switched capacitors arrangement that is compatible with standard CMOS technology. Circuit simulations in a 90nm technology for both single-ended and differential input confirm the ability of convert and stabilize the output common mode (CM) levels. The main drawback is a small loss of output linearity (4.81dB and 2.72dB for single-ended and differential input, respectively).**

I. Introduction

Track-and-Hold (TH), or Sample-and-Hold (SH) is a circuit element with the ability to track the magnitude of a continuously varying signal and momentarily capture it as a constant value. It is employed in a wide range of electronic circuits. The name Track and Hold is more befitting, as it better describes the real operation: the input signal is followed (tracked) by the output, until the TH receives a command to freeze the latter. When done, the TH starts tracking the input signal again.

A TH is one of the main building blocks in modern Analog-to-Digital (ADC) design, which are circuits that transform a signal from the real-world analog domain to its digital domain approximation. There are several architectures devised for this purpose, and most require a stable input signal during the process of conversion, a requirement that is fulfilled by the TH.

There are different schemes to perform track and hold on a voltage signal, from simple capacitor-switch arrangement to complex wide-bandwidth track and hold amplifiers (THA), employing either CMOS [1], Silicon-Germanium (SiGe) [2], [3] or Indium Phosphide (InP) [4] fabrication technologies.

Additionally, in the construction of an ADC three different structures exist: fully-differential input, pseudo-differential input and single-ended input [5]. The input signal source (e.g. sensor) and the ADC structure must be consistent, bringing severe limitations on the choice of ADC in a given application. Performing the signal processing of the sampled signal differentially (i.e. the blocks after the TH) presents some advantages over the single-ended processing, including increased noise rejection and dynamic range. However, most sensors and transducers only produce a single-ended output or a differential output with an incompatible common-mode (CM) voltage with that of the succeeding signal processing block. Traditionally, in order to match the signal types, designers have been relying on more complex coupling circuits, that may include electromagnetic transformers [6] or power-hungry programmable amplifiers [7].

We present a novel TH circuit that is able to maintain a desired stable CM voltage at its output, independent from the changes at the input CM voltage. This is a significant circuit design advantage when the TH is connected to a circuit block (e.g. comparator) that requires a stable CM voltage for its proper operation. Another advantage of this circuits it that it readily performs track and hold on both single-ended and differential voltage inputs, yet producing differential output around the desired output CM voltage.

The mathematical model and derivation of the circuit is presented in Section III. The circuit-level implementation is described in Section IV, with the simulation results presented in Section V. The paper is concluded in Section VI.

II. TH Background

Fig. 1 presents two operation phases of the clock signal. In the first, the tracking phase, the circuit works like a closed switch, passing the input signal to the output, ideally not affecting it. During the hold phase, the magnitude of the input in the preceding instant is kept steady until the next tracking phase. Also, during hold phase the circuit block that feeds from TH processes the sampled signal. An ideal TH has a zero output impedance, and an infinite input impedance.

In differential signaling, there are two quantities of primary interest (See Fig. 2). The first is the differential amplitude itself, that is given by;

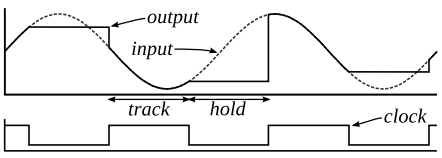

Fig. 1. Working principle of a TH.

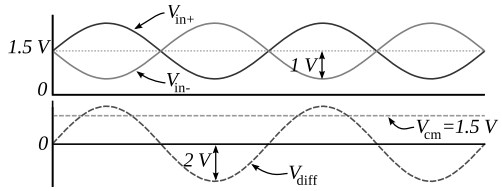

Fig. 2. Decomposition of differential and common-mode levels in a differential signal.

$$V_{\text{diff}} = V_{\text{in+}} - V_{\text{in-}} \tag{1}$$

where $V_{\text{in+}}$ and $V_{\text{in-}}$ are the inputs.

The other quantity is the common-mode voltage, the DC offset of the signal, or in other words, the mean amplitude of $V_{\text{in+}}$ and $V_{\text{in-}}$, as given by;

$$V_{\text{cm}} = \frac{V_{\text{in+}} + V_{\text{in-}}}{2} \tag{2}$$

The CM voltage sets the operating point of the circuits. As an example, Fig. 3 shows the case where the TH feeds a comparator directly (e.g. a 1-bit ADC). In this circuit CM voltage of the TH sets the transconductance of the transistors from the differential pair at the comparator input. This parameter determines some of the performance metrics of the comparator, such as speed, offset and noise susceptibility [8], [9] and therefore should remain stable when the comparator is working.

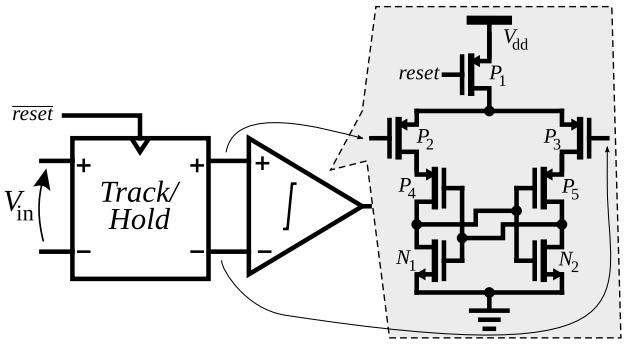

Fig. 3. 1-bit ADC, made up of a TH and a comparator. The TH CM level sets the comparator input pair operating point and overall circuit characteristics.

Hence, designer has to carefully choose the CM amplitude and, what is probably harder, to ensure it remains stable to meet comparator requirement for the operating point. The problem has generally been downplayed or ignored in most recent published work on ADC, where it is characterized within a well-controlled environment, with close to ideal input sources and surrounding circuitry (e.g. a power-hungry amplifier with programmable CM to generate the required CM levels [7], or even a transformer [6]). The whole picture gets even more complicated when ADC needs to fit in a more realistic environment, where the input comes from a signal not well controlled, specially in terms of CM levels.

III. Topology Derivation

We know from (2) that the CM voltage of a differential signal is the arithmetic average of the differential inputs. Let us take a very simple TH circuit for differential inputs, that is shown with the proper waveforms in Fig. 4. Despite this circuit being differential, it may perform track and hold on a single-ended signal, only tieing V_{in-} to ground. In this case, the output is also single-ended. For the sake of clarity, in all the plots inside this section, we consider the clock signal to be permanently in high logic level, and the circuits being in track phase. That means the output CM voltage also follows the input CM voltage.

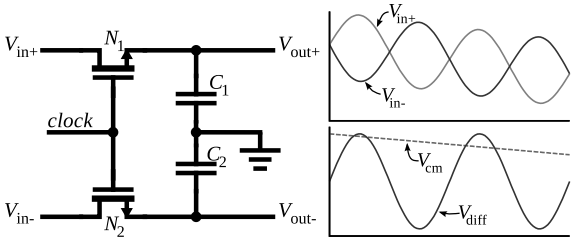

Fig. 4. Simple TH for differential signals.

For illustrating the point, in the figure, the CM is deliberately degraded with time, while maintaining the same the differential magnitude. For the correct operation generally the output CM voltage needs to be kept stable independent of the variation in the input voltages (differential and CM). For V_{cm} to remain stable across the whole operating range of the TH we require a summing compensating CM voltage V_{com}, at every sampling cycle. An implementation of the compensation scheme with an ideal circuit element is shown in Fig. 5, with V_{com} inserted between C_1 and C_2.

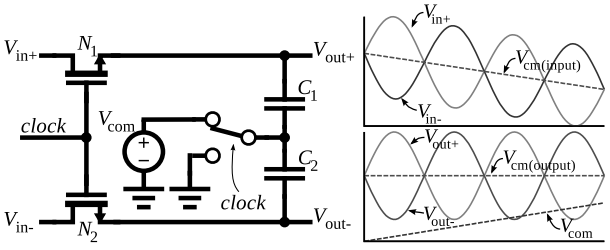

Fig. 5. CM-adjustable TH.

So, at every cycle, V_{com} is given by;

$$V_{\text{com}} = V_{\text{cmS}} - \frac{V_{\text{in+}}}{2} - \frac{V_{\text{in-}}}{2} \tag{3}$$

where V_{cmS} is the desired CM voltage. The V_{com} voltage is a function of the sampled input, and thereof, is different for every track and hold cycle. Note that this leads to a differential output, even if the input is single-ended, a much desired property.

IV. Implementation

In this section, we present the CMOS circuit implementation of the concept introduced in Section III. The circuit is shown in

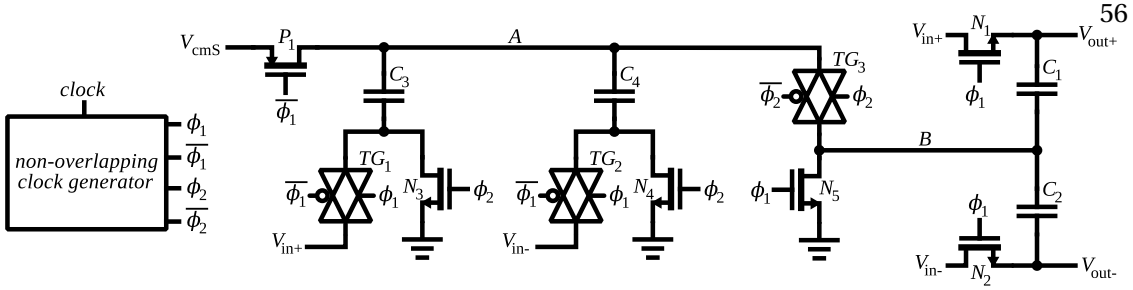

Fig. 6. Proposed CM-adjustable CMOS circuit.

Fig. 6, and is composed of a two-phase non-overlapping clock generator (shown separately in Fig. 7), three transmission gates and a set of pMOS and nMOS transistors and capacitors. The circuit works as follow. Initially, the clock phase ϕ_1 is high. Therefore, the capacitors C_3 and C_4 precharge to the voltages $V_{\text{cmS}} - V_{\text{in+}}$ and $V_{\text{cmS}} - V_{\text{in-}}$, respectively, through the pMOS P_1 and the transmission gates (TG) TG_1 and TG_2. The charges accumulated on each capacitor are, respectively, given by (4) and (5).

$$Q_3 = C_3 \left(V_{\text{cmS}} - V_{\text{in+}}\right) \tag{4}$$

$$Q_3 = C_4 \left(V_{\text{cmS}} - V_{\text{in-}}\right) \tag{5}$$

Concurrently, the transistor N_5 ties the bottom plates of C_1 and C_2 to the ground. Therefore, these capacitors track the input voltages $V_{\text{in+}}$ and $V_{\text{in-}}$. Note that these transistors can be effortlessly replaced by transmission gates or bootstrapped switches, in order to increase linearity, similar to the techniques applied to conventional TH circuits. We have decided to keep the TH design as simple as possible, employing simple N-switches, and therefore, focus on the impact of the conversion circuit.

In the next clock phase ϕ_2, N_5 turns off, disconnecting the node B from ground. Also, the transmission gates TG_1 and TG_2 are turned off, while transistors N_3 and N_4 force the voltages on the bottom plates of C_3 and C_4 to ground. Transistor P_1 is also turned off, disconnecting node A from the voltage source V_{cmS}. On the other hand, TG_3 ties node B to node A. Assuming that the impedance seen on the output nodes $V_{\text{out+}}$ and $V_{\text{out-}}$ is sufficiently high (i.e. the TH does not feed any current-starving load), both $V_{\text{out+}}$ and $V_{\text{out-}}$ nodes experience an offset equal to the voltage on the node A, that we will derive next.

Since both the bottom plates of C_3 and C_4 are now tied together, we may consider them as a single capacitor with a total capacitance value of $C_3 + C_4$. Assuming $C_3 = C_4 = C$, the equivalent capacitance is $2C$. The voltage on node A is found solving;

$$Q_{\text{tot}} = 2.C.V_{\text{A}} \tag{6}$$

where Q_{tot} is the total charge stored previously, during track cycle. We find the total charge summing Q_3 and Q_4, as;

$$C_3 \left(V_{\text{cmS}} - V_{\text{in+}}\right) + C_4 \left(V_{\text{cmS}} - V_{\text{in-}}\right) = 2.C.V_{\text{A}} \tag{7}$$

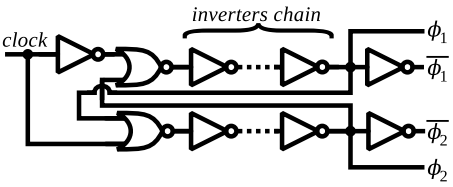

Fig. 7. Non-overlapping clock signals generator.

Setting $C_3 = C_4 = C$, leads to

$$V_{\text{A}} = V_{\text{cmS}} - \frac{V_{\text{in+}}}{2} - \frac{V_{\text{in-}}}{2}. \tag{8}$$

The voltage V_A is the same as in (3).

V. Simulation Results

In order to confirm analytical derivations provided before, we simulate the proposed circuit with a commercial state-of-the-art circuit simulator. The circuit is designed in a recent 90nm technology, with the devices sizes shown in Table I.

We simulated the circuit applying two different input signals: a single-ended signal, where the input $V_{\text{in-}}$ is tied to ground, with a 0.4V sinusoid with 0.2V offset on the other terminal, and a differential 0.4V peek-to-peek sinusoid with 0.2V CM voltage. In both cases, the circuit is required to have a 0.8V CM output, setting V_{cmS} to this amplitude. The waveforms are shown in Fig. 8, for both cases. In the bottom part of the figure, we show the common-mode output level during the hold phase, which is very close to the desired 0.8V (approximately 0.76V and 0.77V for single-ended and differential, respectively). Also, we plot the voltage across capacitors C_3 and C_4, V_{C3} and V_{C4} and the voltage on node B, V_{B}, and input and output, as well.

TABLE I
Component sizes

Device	Size
N_1	W=5μm, L=90nm
N_2	W=5μm, L=90nm
N_3	W=2.5μm, L=90nm
N_4	W=2.5μm, L=90nm
N_5	W=5μm, L=90nm
P_1	W=5μm, L=90nm
TG_1	W_{n}=3.5μm, W_{p}=3.5μm, L=90nm
TG_2	W_{n}=3.5μm, W_{p}=3.5μm, L=90nm
TG_3	W_{n}=3.5μm, W_{p}=3.5μm, L=90nm
C_1	C=1pF
C_2	C=1pF
C_3	C=500fF
C_4	C=500fF

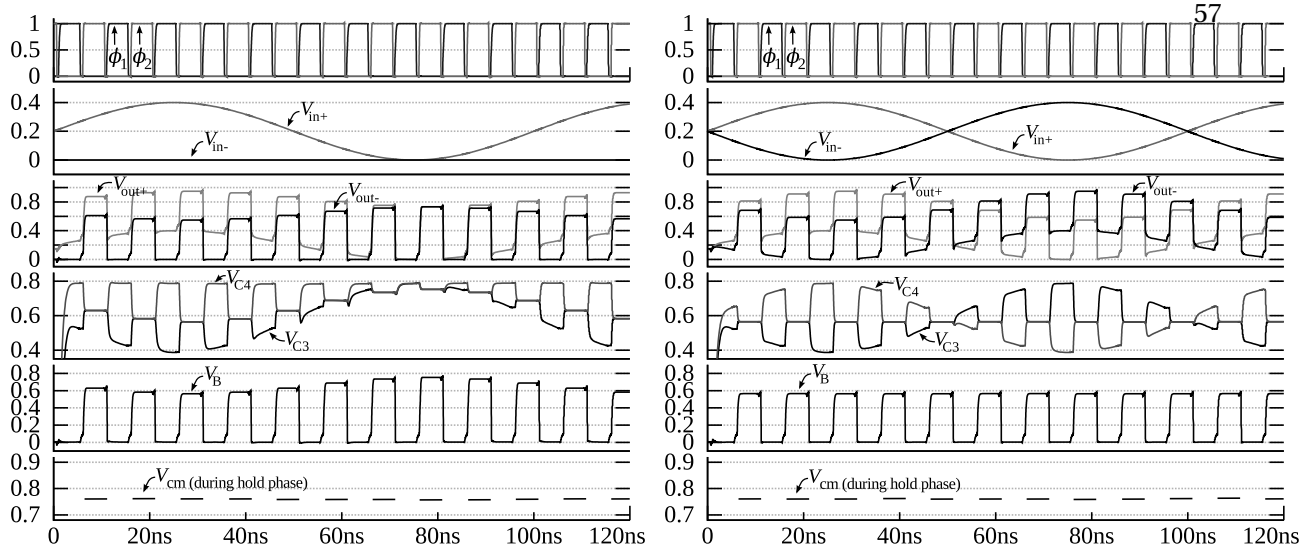

Fig. 8. Simulation results for single-ended input/differential output, and differential input (CM=0.2)/differential output (CM=0.8).

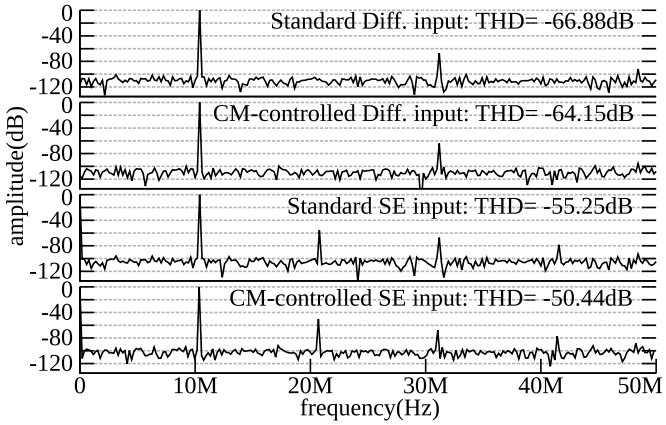

Fig. 9. FFTs of the simulated outputs.

Moreover, in order to estimate output linearity of the proposed circuit, we compare its simulated results with that of a simple TH circuit in Fig. 4. The components sizes are given in Table I for N_1, N_2, C_1 and C_2. We performed an FFT on four different combinations of circuit configurations and input types, in order to measure the linearity of both circuits.

The FFTs with the total harmonic distortion (THD) for two circuits are shown in Fig. 9. The relatively high levels of harmonic distortion in both circuits are caused by the non-linearity imposed by using simple nMOS transistors as switches in TH circuits. This can eliminated by employing transmission gates or bootstrapped switches. However, comparing the linearity of two circuits we note that our CM-stabilized exhibit an small degradation in THD. When converting a single-ended input signal into a differential output signal with 0.8V CM level, our circuit presents a loss of 4.81dB in THD when compared to the simple TH circuit with a single-ended output. For the case differential input with 0.2V CM, our circuit provides a 0.8V CM differential output, presenting a small loss in the THD (-2.73dB), when compared to the circuit of Fig. 4 where the output follows input CM. In both cases, we sacrifice a small amount of linearity in order to achieve the desired property; stabilized output CM, and the ability to convert a single ended input to a differential output.

VI. Conclusion

In this paper, we have presented a novel TH design with the ability to maintain a stable output CM voltage independent of the input CM. The circuit analytical derivation, its implementation in CMOS, and corresponding simulations were presented. The employment of the presented circuit avoids complicated coupling schemes between different signal types, including transformers and purpose-specific amplifiers. Further, it allows a conversion from a single-ended signal to a differential output. Through simulations, we have estimated the THD impact on the output to be -4.81dB and -2.73dB.

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ANEXO A EMAIL DE ACEITAÇÃO DO ARTIGO II

COURTOIS, B. **Your submission MEJ-D-11-00508** [mensagem pessoal]. Mensagem recebida por <taimurgibran@gmail.com> em 6 jan. 2012.

Gmail by Google

Taimur Gibran Rabuske <taimurgibran@gmail.com>

Your submission MEJ-D-11-00508

Bernard Courtois <Bernard.Courtois@imag.fr> **Fri, Jan 6, 2012 at 6:05 AM**
To: taimurgibran@gmail.com
Cc: Bernard.Courtois@imag.fr, saeid@mtu.edu

Ms. Ref. No.: MEJ-D-11-00508
Title: A 5MSps 13.25珐 8-bit SAR ADC with Single Ended or Differential Input
Microelectronics Journal

Dear Taimur,

I am pleased to inform you that your submission entitled
"A 5MSps 13.25珐 8-bit SAR ADC with Single Ended or Differential Input" has been accepted for publication in the Microelectronics Journal.

Attached you will find comments from the reviewers. When you submit the final version of your paper, you must provide a summary, as a separate sheet, of how you addressed these comments in the revised version, or of the reasons why you consider better not to take them into account.

To submit the final version, please go to http://ees.elsevier.com/mej/ and login as an Author.
Your username is: taimurgibran
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On your Main Menu page is a folder entitled "Submissions Needing Revision". You will find your submission record there.

Yours sincerely,

Bernard Courtois
Editor-in-Chief
Microelectronics Journal

Reviewers' comments:

Reviewer #1: Paper describing a very interesting work and with original contributions.
Minor typos and errors in the document writing.

Reviewer #2: This paper describes in detail the design of an ultra low power consumption and energy (13.25uW) analog to digital converter at a moderate bit rate (5MSps). The challenge of the work is related to the track and hold (TH) circuit design. The approach is to maintain a common mode voltage at the output of the TH block, and the ultra low power design technique. Most of the transducer circuit generates a single ended output or a differential output with an incompatible common mode voltage. The novel approach is very useful for the integration of sensor in wireless applications.

ANEXO B OUTRAS PUBLICAÇÕES DURANTE O MESTRADO

RABUSKE, T. G.; PINHEIRO, R. B.; FERNANDES, J.; RODRIGUES, C. R. PyCO: A Parallel Genetic Algorithm Optimization Tool for Analog Circuits. In: IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS (ISCAS), 2012. Seul, Coréia do Sul. **Anais...** Manuscrito aceito para publicação. 20-23 maio 2012.

CORREIA, D.; ALBA, M. D.; MARTINS, M. A; RABUSKE, T. G.; RODRIGUES, C.; FERNANDES, J. R. An IR-UWB Transmitter with Digital Pulse Duration Control. In: IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS (ISCAS), 2012. Seul, Coréia do Sul. **Anais...** Manuscrito aceito para publicação. 20-23 maio 2012.

RABUSKE, T. G.; FERNANDES, J. R.; NOOSHABADI, S.; RODRIGUES, C. R. A 749nW 1MSps 8-bit SAR ADC at 0.5V Employing Boosted Switches. Manuscrito não publicado.

RABUSKE, T. G.; RABUSKE, F. A.; FERNANDES, J. R.; RODRIGUES, C. R. A 4-bit 1.5GSps 4.2mW Comparator-Based Binary Search ADC in 90nm. Manuscrito não publicado.

PINHEIRO, R. B.; RABUSKE, T. G.; RODRIGUES, C. R. Distributed Version Control as a Tool to Increase Productivity in Analog and Mixed-Signal Design. In: IBERCHIP WORKSHOP, 2011. Bogotá, Colômbia. **Anais...** 23-25 fev. 2011.

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